A Study on the Fluorine Effect of Direct Contact Process in High-Doped Boron Phosphorus Silicate Glass (BPSG)

Hyung-Joon Kim^{1,2}, Pyungho Choi², Kwangsoo Kim², and Byoungdeog Choi^{2,*}

Abstract—The effect of fluorine ions, which can be reacted with boron in high-doped BPSG, is investigated on the contact sidewall wiggling profile in semiconductor process. In the semiconductor device, there are many contacts on p^+/n^+ source and drain region. However these types of wiggling profile is only observed at the n⁺ contact region. As a result, we find that the type of plug implantation dopant can affect the sidewall wiggling profile of contact. By optimizing the proper fluorine gas flow rate, both the straight sidewall profile and the desired electrical characteristics can be obtained. In this paper, we propose a fundamental approach to improve the contact sidewall wiggling profile phenomena, which mostly appear in high-doped BPSG on nextgeneration DRAM products.

Index Terms—BPSG, contact, fluorine, ion implanttation

I. INTRODUCTION

As semiconductor device design rule dimensions gradually shrank, the device contact and metal line space also decreased. In order to increase the gap-fill margin of interlayer dielectrics between conducting lines, high doped Boron Phosphorus Silicate Glass (BPSG) layer was applied [1]. The concentration of boron and phosphorus in the BPSG layer can change the reflow property of this layer and the etching rate for chemical etchants [2, 3]. Therefore the plug ion implantation dopant species and chemical etchants used in the direct contact (DC) process which is formed at transistor source/drain region can change the properties of the high doped BPSG layer [4]. Failure to properly understand these properties can cause contact related failures, especially short failure between contacts.

In this study, we proposed the solution and root cause of the sidewall wiggling profile of contacts during the DC process and discussed the effects of the interaction between fluorine gas and the BPSG layer. We also revealed the effect of n^+/p^+ plug ion dopant species with fluorine ions. Fig. 1 shows the failure analysis image of the contact-to-contact short in a DRAM product.

II. EXPERIMENTAL DETAILS

In this work, 8 inch p-type Si (100) wafers were used as the starting substrates. As interlayer dielectrics, 450nm thick BPSG film which contained 7.0wt% boron and 3.2wt% phosphorus was deposited on the Si substrates by



(a) Failure analysis [Top view]
(b) Failure analysis image
Fig. 1. Failure by n⁺ contact wiggling profile.

Manuscript received Dec. 21, 2012; accepted Sep. 6, 2013

¹ Yield Enhancement Team, Memory Division, Samsung Electronics Co. San#16 Banwol-Dong, Hwasung-City, Gyeonggi-Do, 445-701, Republic of Korea

² College of Information and Communication Engineering, Sungkyunkwan University, Suwon, 440-746, Republic of Korea E-mail : bdchoi@skku.edu

chemical vapor deposition (CVD) after standard Si cleaning. After deposition, the 100nm size direct contacts were formed by the dry etch process after photolithography patterning for n^+/p^+ contacts. After forming the contacts, As⁺ plug ion implantation for the n⁺ contact and BF_2^+ plug ion implantation for the p⁺ contact were utilized to make a source and drain junction of metal oxide semiconductor field effect transistor (MOSFET). In order to remove the residual by-product and clean the damaged Si surface in the contacts after dry etch process, the Si treatment process using fluorine gas was performed. The flowchart of key processes for DRAM direct contact is summarized in Table 1. We experimented with these specimens using various quantities of fluorine in order to check the profile of contacts (Table 2). Next, the effect of dopant species was evaluated by exchanging the ion implantation process (Table 3). For the specimens that were utilized with Tables 2 and 3 conditions, scanning electron microscope (SEM) and transmission electron microscopy (TEM)

	Table 1.	. Flowcha	rt of key	processes	for DR	AM (direct	contact
--	----------	-----------	-----------	-----------	--------	------	--------	---------

Photolithography and etching for p+ contact formation $p+(BF_2^+)$ plug implantation (Energy: 35KeV, Dose: 4×10^{15} /cm ²)
PR Ashing/Strip
Photolithography and etching for n+ contact formation
n+(As ⁺) plug implantation (Energy: 40KeV, Dose: 3×10 ¹⁵ /cm ²) PR Ashing/Strip
Rapid thermal nitridation (RTN) anneal for activation of implanted ions
Si treatment for removing the residual by-product in the contacts
Post cleaning by SC1 and barrier metal pre cleaning by HF Contact barrier metal (Ti 60Å/TiN 80Å) deposition at 650 °C

Contact filling with tungsten(550 Å) by chemical vapor deposition

* SC1 cleaning (NH₄OH:H₂O₂:H₂O = 1:1:5)

Table 2. Si	treatment	test condition
-------------	-----------	----------------

Specimen	NF ₃ (sccm)	O ₂ (sccm)	Time (sec)	Remark
#1	15	180	SKIP	
#2	15	180	15	
#3	15	180	25	Control group
#4	15	180	35	
#5	4	30	20	

	D 1		•			4 * . *
' abla '	111110	1010	1 100 10	ontotion	toot	a a m d t t a m
I SIMP 1	PIIIO	14 11 1	11111	ининин	1001	1.
rance.	I IUG	IUII	mm _U	antanon	icor	contantion
			-			

Specimen	Group / Contact	$DC p^+$ contact	DC n ⁺ contact
#6	Control group	$49BF_2^+$	75As^+
#7	Test group	$75As^+$	$49BF_2^+$

were carried out to make a comparison with the contact profile of each condition. The electrical characteristics of resistance for contacts were also measured by Agilent 4156C precision semiconductor parameter analyzer.

III. RESULTS AND DISCUSSION

3.1 Contact Profile Analysis for Each Condition

After forming the direct contacts, the contact profiles for the Si treatment conditions before the barrier metal deposition step were as follows: when the Si treatment step was skipped [Fig. 2(a)], the n^+ contact profile was dramatically improved. This profile of skip condition was different from that of the previous control group condition [Fig. 2(b)]. In this experiment, we could confirm that the bad n⁺ profile was a result of the interaction between the BPSG layer and the fluorine gas used in the Si treatment step. Based on these results shown in Figs. 2(a) and (b) for the fluorine effect, the n^+ contact profile in Fig. 2(c) also had a good profile, as we expected, when the fluorine flow $(NF_3 \text{ gas})$ was decreased from 15 to 4sccm. But the p^+ contact in Fig. 2(d) always had a good profile even though the flow rate of fluorine was high enough to make a bad profile in n⁺ contact during the experiment. It means clearly that the different dopants of n^+/p^+ plug ion implantation affect the interaction between the BPSG layer and the fluorine gas in the contacts. In order to confirm such a phenomenon, the p^+ contact was applied to the n^+ plug ion implantation scheme (As⁺) such as in Table 3. As a result, the p^+ contact also had a bad profile [Fig. 3(b)]. Therefore we could find that ion dopant played an important role in contact profile. The mechanism of these results would be covered in the chapter. 3.3.

3.2 Electrical Characteristics for Each Condition

Since all semiconductor devices have contacts and all contacts have contact resistance, it is important to characterize such contacts. If not properly minimized, it can make a significant contribution to the device series resistance [5]. Even if a contact has good profile through any process condition, high contact resistance is meaningless in the point of view of overall contact process integration. In this work, we analyzed the



Fig. 2. n^+/p^+ contact profile for Si treatment time and NF₃ flow condition



(a) Specimen $\#6 p^+$ contact

Fig. 3. p^+ contact profile for the type of dopants.

electrical characteristics of each condition after checking the profiles. We utilized the commonly used contact string pattern which consisted of one thousand contacts. After measuring total resistance, the value of resistance was divided by the number of contacts to get each contact resistance. When we measured the improved profile which the Si treatment step was skipped, the resistance of the n⁺ contact was 30% higher than that of the control group because of the residual polymer of the Si sub-interface. This high resistance of the n^+ contact could not be applied to device products. Also the n^+ contact resistance was gradually decreased according to the increase of Si treatment time because of the effective by-product and damaged Si surface removal and the contact area increase with the time [6]. The measured Si open sizes for n+ contacts are 80, 102 and 112nm for specimen (a), (b) and (c) in Fig. 2, respectively. The improved group that had less NF₃ flow (15 \rightarrow 4sccm) Si treatment condition, not only had a good DC profile but also had good electrical characteristics compared with the previous control group. For the resistance of p^+

contact, there was no big difference between each condition such as good profiles over all test conditions.

3.3 Failure Analysis and Mechanism

Based on the experimental results, the failure mechanism was established for the n^+ contact. Fig. 5(a) shows the failure mechanism of n^+ contact. The fluorine ions that were injected into the contacts during Si treatment process reacted with the boron in the etching damaged BPSG layer area. Also the boron ions could be easily escaped from the Si-O bonds of oxide broken by ion implantation. This reaction resulted in stable BF₃ products and diffused out from the n^+ contact hole [7, 8]. It also resulted in numerous pores in the BPSG layer like the TEM inset image in Fig. 5(a). The etching rate of these damaged pore layers could be abruptly increased by the next HF cleaning process [9, 10]. This mechanism can be supported by another test in Fig. 6. We checked the n⁺ contact profile as a function of delay time from the Si treatment to post HF cleaning process. The wiggling



Fig. 4. Electrical property of n^+/p^+ contacts for Si treatment condition.



Fig. 5. Schematic failure mechanism for n^+/p^+ contacts during Si treatment process. Inset image of Fig. 5(a) is the analyzed pores in BPSG layer by TEM.

profiles were found over 130min. of delay time even though these profiles could be easily formed in n^+ contacts. It means that the wiggling process needs the critical time to form the pore through chemical reaction. The more interaction between fluorine ions and boron increase, the more wiggling contact profile occurred. Thus, a wiggling profile such as Fig. 2(b) could be easily formed on the n^+ contact. In contrast, for the p^+ contact shown in Fig. 5(b), the 10^{15} /cm² dose level BF₂⁺ dopants were injected into the contact during the plug ion implantation and then the secondary scattered $\mathrm{BF_2^+}$ ions were also injected into the sidewall. These BF_2^+ ions could be reacted with fluorine ions injected into the p^+ contact during the Si treatment and could be transformed into the stable form (covalent bonding) of $BF_3[11]$. As a result, for the p^+ contact, the boron in the BPSG layer was not greatly consumed producing BF₃ and these contact sidewalls did not have porous layers. The next



Fig. 6. Effect of post cleaning delay time on n^+ contact wiggling.

cleaning process never resulted in any wiggling p^+ contact profile different from the n^+ contact. [Fig. 2(d)]

IV. CONCLUSIONS

A new method for the Si treatment process step was proposed in this study in order to solve the contact-tocontact short failure by wiggling profile. Previously, the boron and phosphorus dopants of BPSG or the post HF cleaning recipe was only changed to prevent these failures. In that case, these failures could occur again in any other device products because the fundamental problem remained unsolved. We proved that the contact sidewall became porous because of the interaction between boron and fluorine, and the subsequent HF cleaning step accelerated the etching rate of the porous layer. Finally this irregularly etched layer became a wiggling bad profile contact. Therefore we proposed a lower flow of NF₃ gas in order to suppress this failure. This solution successfully resulted in not only a straight profile sidewall contact but also good electrical properties. Besides, we also proposed a new failure mechanism in direct n^+/p^+ contacts that used different kinds of plug ion implantation dopants.

The newly proposed mechanisms can fundamentally prevent the contact failure related profile according to high-doped BPSG in next-generation devices.

ACKNOWLEDGMENTS

This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2009-0083540)

REFERENCES

- M. Fanciulli, E. Bonera, E. Carollo, L. Zanotti, "EPR and UV-Raman study of BPSG thin films: structure and defects," *Microelectronic Engineering*, Vol.55, pp.65-71, 2001.
- [2] Jagadeesha T, Louis Kim, Wei Ti Lee, and Thammaiah Gowda, "Development of new BPSG process to reduce boron concentration range in BPSG SACVD processes," *International Journal* of Engineering Science and Technology, Vol.3, No.1, pp.156-161, Jan., 2011.
- [3] R. Fuller, H. Evans, C. Gamlen, B. Czagas, M. Morrison, D. Decrosta, and R. Lowry, "The Effect of Deposition Conditions on the Radiation Tolerance of BPSG Films," *IEEE Transactions on Nuclear Science*, Vol.43, No.6, pp.2565-2571, Dec., 1996.
- [4] Mary Tiemessen, Ping Wang, Paul Oakey, Lisa Liu, Stephen Schauer and Carl Bowen, "Fluorine Induced Formation of Intermetal Dielectric Defects," *IEEE/SEM1 Advanced Semiconductor Manufacturing Conference*, pp.303-307, 1996.
- [5] Yuan Taur, Jack Yuan-Chen Sun, Dan Moy, L. K. Wang, Bijan Davari, Tephen P. Klepner, and Chung-Yu Ting, "Source-Drain Contact Resistance in CMOS with Self-Aligned TiSi," *IEEE Transaction on Electron Devices*, Vol.34, No.3, pp575-580, 1987.
- [6] B. E. E. Kastenmeier, P. J. Matsuo, and G. S. Oehrlein, "Remote plasma etching of silicon nitride and silicon dioxide using NF₃/O₂ gas mixtures," *Journal of Vacuum Science and Technology A*, Vol.16, No.4, pp.2047-2056, 1998.
- [7] S.Y. Lee, J.B. Yoon, Samsung Internal Technical Report, 2002 [in Korean].
- [8] K. H. Lau and D. L. Hildenbrand, "Thermochemical studies of the BF₂ radical," *Journal of Chemical Physics*, Vol.72, No.9,

pp.4928-4931, May., 1980.

- [9] Arvind Sankaran and Mark J. Kushner, "Fluorocarbon plasma etching and profile evolution of porous low-dielectric-constant silica," *Applied Physics Letters*, Vol.82, No.12, pp.1824-1826, Mar., 2003.
- [10] R. Charavel and J. P. Raskin, "Etch Rate Modification of SiO₂ by Ion Damage," *Electrochemical and Solid-State Letters*, Vol. 9, No. 7, pp.G245-G247, 2006.
- [11] T.W. Graham Solomons and Craig B. Fryhle: Organic Chemistry (John Wiley & Sons, NJ, 2009) 10th ed., p. 39.



Hyung-Joon Kim received the Master degree in Hanyang University in 2001, and he has been working at Samsung Electronics from 2001. He has been working toward the Ph. D degree at Sungkyunkwan University since 2010. His current research

interests include DRAM and CMOS Image Sensors characterization and reliability analysis.



Pyungho Choi received the Master degree in Sungkyunkwan University in 2012. Since 2012, he has been working toward the Ph. D degree at Sungkyunkwan University. His current research is focused on Electrical characteristic analysis of

solar cell device.



Kwangsoo Kim received the Master degree in Hanyang University in 2004, and he has been working at Samsung Electronics from 2004. He has also been working toward the Ph. D degree at Sungkyunkwan University since 2011. His current

research is focused on Electrical characteristic analysis of MOSFET.



Byoungdeog Choi received the B.S. and M.S. degrees in physics from Kyung Hee University, Seoul, S.Korea in 1988 and 1990, respectively,and the M.S. and Ph.D. degrees in electrical engineering from Arizona State University,

Tempe, Arizona in 1998 and 2001, respectively. He spent 6 years at Samsung in S. Korea. In 2008, he joined School of Information and Communication Engineering, Sungkyunkwan University in S. Korea, where he is currently an professor. His research involves MOS devices, defects insemiconductor, carrier lifetime measurement, and gateoxide integrity.