http://dx.doi.org/10.5573/JSTS.2013.13.6.622 JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.13, NO.6, DECEMBER, 2013

Performance Investigation of Insulated Shallow Extension Silicon On Nothing (ISE-SON) MOSFET for Low Volatge Digital Applications

Vandana Kumari[1], Manoj Saxena[2], R. S. Gupta[3], and Mridula Gupta[1,*]

Abstract—**The circuit level implementation of nanoscale Insulated Shallow Extension Silicon On Nothing (ISE-SON) MOSFET has been investigated and compared with the other conventional devices i.e. Insulated Shallow Extension (ISE) and Silicon On Nothing (SON) using the ATLAS 3D device simulator. It can be observed that ISE-SON based inverter shows better performance in terms of Voltage Transfer Characteristics, noise margin, switching current, inverter gain and propagation delay. The reliability issues of the various devices in terms of supply voltage, temperature and channel length variation has also been studied in the present work. Logic circuits (such as NAND and NOR gate) and ring oscillator are also implemented using different architectures to illustrate the capabilities of ISE-SON architecture for high speed logic circuits as compared to other devices. Results also illustrates that ISE-SON is much more temperature resistant than SON and ISE MOSFET. Hence, ISE-SON enables more aggressive device scaling for low-voltage applications.**

Index Terms—**Insulated shallow extension, silicon on nothing, inverter, ATLAS 3D, logic gates, temperature**

Manuscript received Dec. 13, 2012; accepted Aug. 11, 2013

[1]Semiconductor Device Research Laboratory, Department of Electronics Science, University of Delhi, South Campus, New Delhi, India
[2]Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi, New Delhi, India
[3]Department of Electronics and Communication Engineering, Maharaja Agrasen Institute of Technology, Rohini, Delhi, India
E-mail : Mridula@south.du.ac.in

I. INTRODUCTION

CMOS technology has been widely used for digital switching element in semiconductor memories and system on chip (SOC) applications due to its low cost, large noise margin, easily manufacturing process and overall reliability [1]. CMOS is also commonly used to develop random access memory (RAM), micro-processors, digital signal processors (DSP), and image sensors. However, with continuous device scaling, one of the major challenges for large scale integrated circuits i.e. the leakage current in individual devices, results in excessive power loss and heat generation. Therefore, to keep the advantages of technology scaling, it is essential to find solutions to minimize the leakage current and lower sub-threshold slope.

Recently, we proposed a new device architecture called Insulated Shallow Extension Silicon On Nothing (ISE-SON) MOSFET that combines the advantages of Silicon On Nothing (SON) [2] and Insulated Shallow Extension (ISE) MOSFET [3] showing superior device performance as compared to other devices for DC as well as the analog applications even at the higher temperatures [4, 5]. The advantage of ISE-SON over the conventional ISE and SON is because of the dielectric isolation provided by the dielectric pillars and the buried oxide layer except the uppermost part of the channel at which the inversion layer is formed. The insulating layers effectively suppressed the field penetration from drain to source region and thereby showing reduction in Channel Length Modulation (CLM) and Hot Carrier Effect (HCE) [6]. Previously [4, 5] we have already demonstrated that,

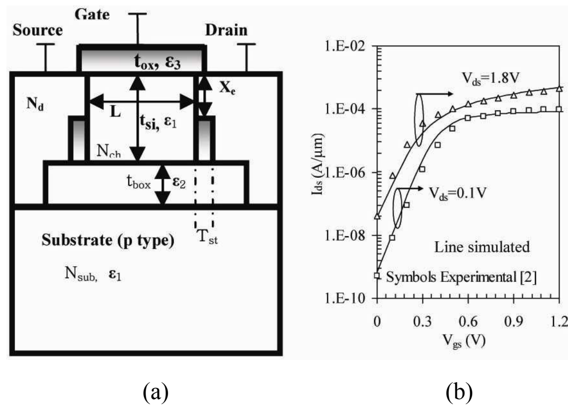


Fig. 1. (a) Schematic cross sectional view of the ISE-SON MOSFET, where ε_1 (11.9), ε_2 (1) and ε_3 (3.9) are the permittivity of channel, buried oxide layer and side pillars respectively, T_{st} (10 nm) is the thickness of the side pillar, N_{ch} (1×10^{17} cm^{-3}) and N_{sub} (2×10^{18} cm^{-3}) are the doping concentration in the channel and the substrate region respectively, (b) Transfer characteristics of SON MOSFET in semi logarithmic scale at different drain biases [2].

ISE-SON architecture shows enhanced immunity against the HCE as compared to ISE and SON because of suppressed electron temperature at the drain side. The reduction in electron temperature at the drain side is only because of the presence of side pillars. The gate and substrate leakage current are also suppressed in case of ISE-SON architecture as compared to other devices [7]. Although, the suitability of the ISE-SON for analog applications has been discussed in detailed [4, 5] but suitability for low-voltage digital application is still not discussed. Thus to explore the advantage of the ISE-SON (as shown in Fig. 1(a)) over ISE and SON for low voltage digital applications, dynamic and transient behaviour of CMOS inverter [8] has been discussed in this work using ATLAS 3D mixed mode simulation [9]. Inspite of this various reliability issues such as process and temperature variability has been discussed *in section IV*. Application of the non-classical device architecture is also extended to explore its usage for implementing the universal logic gate (i.e. NAND and NOR gate) and ring oscillator.

II. FABRICATION FEASIBILITY

The fabrication feasibility of the ISE-SON architecture is not discussed in the literature till date. Thus, the proposed fabrication flow of the non-classical device (i.e. ISE-SON) based on the process steps of ISE and SON architecture is also discussed in this work. The process flow of the ISE-SON architecture is initiated by the conventional STI isolated wafer. Thereafter epitaxy of SiGe layer can be performed followed by the Si cap layer (serve as the active channel layer). SiGe layer can be used for transferring the continuity of the lattice from the bulk to the silicon cap layer. After epitaxy, conventional CMOS process flow can be carried out until the spacer layer formation. Thereafter trenches in the S/D regions can be formed using anisotropic plasma etching to provide the access to SiGe. The SiGe layer is then selectively etched out which forms a tunnel underneath the Si cap layer (channel). The tunnel layer (SON) isolates the channel region attached to the gate from the substrate region. The gate and the active channel region is supported at both the ends by STI. Furthermore, a passivation of internal wall of tunnel with a thin RTO oxide is useful for preventing the tunnel from being refilled with silicon when rebuilding the S/D extension by epitaxy [10]. After the spacer layer formation, the depressions in the S/D region can be formed using anisotropic plasma etching which determines the depth of dielectric pockets (DP). Thereafter, second pair of nitride spacers can be formed on the vertical sidewalls of the depressions. Further, PECVD oxide layer shall be deposited prior to the second nitride layer. This provides a protection to the bottom of the depression and upper nitride space layer from being further etched during the buried spacer formation. The uncovered part of PECVD oxide is removed after buried spacer formation (i.e. the dielectric pocket). After dielectric pocket formation, the selective epitaxy was carried out to fulfill the depression in the S/D regions [3].

The proposed fabrication process scheme of ISE-SON architecture discussed above requires some additional steps as compared to the SON architecture to form the insulating layers at the side walls of the channel. However, on the basis of the fabrication techniques described for SON [10] and ISE [3] MOSFET architectures separately, the possibility of fabricating ISE-SON MOSFET seems possible. In addition, the analytical modeling scheme proposed earlier for ISE-SON architecture [5] also helps in understanding the device physics of the non-classical architecture and laying down design guidelines for the sub-100-nm device

design. In addition, the various advantages of ISE-SON architecture in terms of the DC and digital performance metrics have also been discussed *in section IV* to prove the superiority of ISE-SON as compared to SON at an expense of fabrication complexity of the device architecture.

III. Calibration and Simulation Details

Due to non-availability of any experimental results of ISE-SON architecture, the simulation results were calibrated with the available experimental results for n-type SON [2] (as shown in Fig. 1(b)) and then same models are used to simulate the various device architectures. Various models invoked during simulation are parallel and transverse field dependent (FLDMOB) and concentration dependent mobility (CONMOB) model along with the Shockley– Read–Hall (SRH for fixed carrier lifetime) recombination model for minority carrier recombination. Mobility models i.e. transverse and parallel field dependent mobility model available in the ATLAS are adjusted to get the best fit with the experiment results. The best fit curve is obtained at acc.sf=0.5 and inv.sf=0.5. acc.sf (inv.sf) specify the accumulation (inversion) saturation factor which describes the ratio of the majority carrier concentrate on in the accumulation (inversion) layer before and after bending of conductivity and valence bands. To account the "non-local" effects such as velocity overshoot and impact ionization which have significant impact on the device performance at the shorter gate lengths hydrodynamic model is used. Hydrodynamic transport model adds continuity equations for the carrier temperatures, and treats mobilities and impact ionization coefficients as functions of the carrier temperatures rather than functions of the local electric field. The default values of hydrodynamic model for carrier electrons and holes have been used in the simulation [9]. The calibrated parameters are then fed into our ATLAS 3D device simulator to get the accurate results. However, the device degradation due to self heating is not accounted in the present work.

IV. Results And Discussions

For fair comparison among various devices i.e. ISE-SON, ISE, SON and bulk as shown in Figs. 1(a) and 2(a)-(d), same structural parameters are taken into consideration. Thereafter, threshold voltage for both P-MOS and N-MOS is optimized (V_{th}=0.25V @ V_{ds}=0.5V both P-MOS and N-MOS) for different architectures by tuning the metal gate work-function in the range of 4.4eV to 4.9eV. The other device parameters are kept constant. The various physical device parameters which are used during simulation of the device architectures are listed in Table 1.

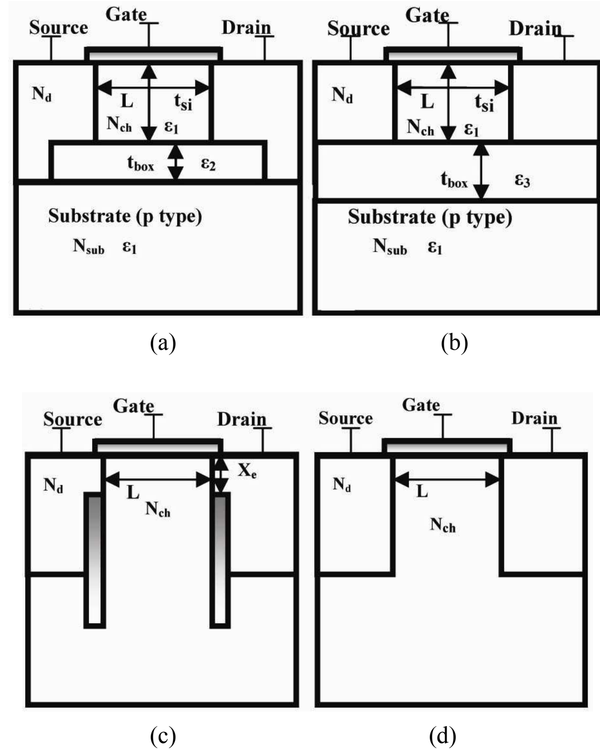


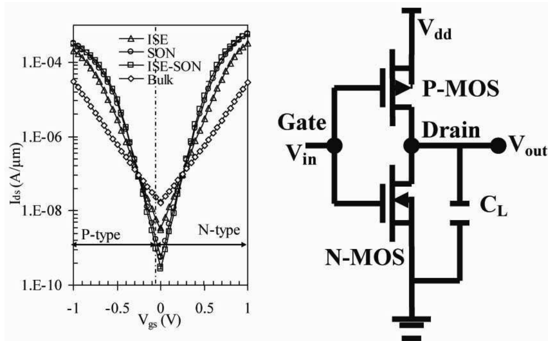
Fig. 2. Schematic cross section view of the (a) Silicon On Nothing, (b) Silicon On Insulator, (c) Insulated shallow Extension, (d) bulk MOSFET.

It can be clearly observed from Fig. 2(e) that, I_p and I_n @ V_{gs}=0V are same for all the devices. However, the off state leakage current (I_{off}) is tremendously high in bulk MOSFET architecture as compared to ISE, SON and ISE-SON MOSFET. This is only because of the enhanced Short Channel Effect (SCEs) in bulk MOSFET as compared to other devices in which the insulating layers are used to suppress the SCEs.

Table 2 shows that, ISE-SON architecture exhibits higher I_{on}/I_{off} ratio followed by SON, SOI, and bulk MOSFET. This is because of the tremendously suppressed leakage current in ISESON architecture as

Table 1. List of parameters used for simulating various devices i.e. ISESON, SON, SOI ISE and Bulk MOSFET

	ISESON	SON	SOI	ISE	Bulk
Channel Thickness (t_{si})	10 nm	10 nm	10 nm	--	--
Buried Oxide Thickness (t_{box})	10 nm	10 nm	50 nm	--	--
Shallow Extension Depth (X_e)	5 nm	--	--	5 nm	--
Shallow Extension Thickness (T_{st})	10 nm	--	--	10 nm	--
Channel Doping (N_{ch})	1×10^{17} cm^{-3}	1×10^{17} cm^{-3}	1×10^{17} cm^{-3}	1×10^{17} cm^{-3}	1×10^{17} cm^{-3}
Substrate Doping (N_{sub})	2×10^{18} cm^{-3}	2×10^{18} cm^{-3}	2×10^{18} cm^{-3}	N_{ch}=N_{sub}	N_{ch}= N_{sub}
Permittivity of channel (ε_1)	11.9	11.9	11.9	11.9	11.9
Permittivity of buried oxide (ε_2)	1	1	3.9	--	--
Permittivity of side pillars (ε_1)	3.9	--	--	3.9	--



(e) (f)

Fig. 2. (e) I_{ds}-V_{gs} characteristics of N-MOS and P-MOS for all the devices under consideration for V_{ds}=1.0 V, L=32 nm, t_{ch}=10 nm, $N_{ch}=1\times10^{17}$ cm^{-3}, $N_{sub}=2\times10^{18}$ cm^{-3}, for ISE and ISE-SON, T_{st}=10 nm, X_e=5 nm; for SON and ISE-SON, t_{box}=10 nm, (f) Basic CMOS inverter using driver (N-MOS) and load (P-MOS).

Table 2. Simulated electrical parameters of various device architectures i.e. ISESON, SON, ISE and Bulk MOSFET optimized at the same V_{th} (0.25 V); L=32 nm, t_{box}=10 nm, t_{st}=10 nm, X_e=5 nm, I_{on} @ V_{gs}=1 V and R_{on} @ V_{gs}=1 V

	DIBL (mV/V)	I_{on}/I_{off}	S (mV/decade)	R_{on} (mΩ)
ISESON	200	2.0×10^6	100	1.8
SON	275	1.0×10^6	113	1.7
ISE	400	9.6×10^4	171	2.9
Bulk	520	1.6×10^3	220	35

discussed above and thereby showing fast digital performance as compared to other devices. The sub-threshold slope (S) of the ISE-SON architecture is also lower that the other devices. The on-state resistance of ISE-SON architecture is marginally higher than the SON MOSFET because of comparatively lower on-state current. Also, the achieved Drain Induced Barrier Lowering (DIBL) is lower in ISE-SON architecture thereby showing immunity against the drain bias variation. Thus there are several advantages of ISE-SON architecture as compared to SON in respect to the DC characteristics and these are: (a) ISE-SON architecture exhibits 52% lower leakage as compared to SON, (b) ISE-SON architecture shows nearly 50% higher I_{on}/I_{off} ratio as compared to SON, (c) sub-threshold slope of ISE-SON architecture is approximately 13% lower than the SON MOSFET, (d) 27% reduction in DIBL is observed in ISE-SON architecture as compared to SON MOSFET.

Inspite of these advantages, the on-state current of ISE-SON architecture is marginally lower (5%) than the SON MOSFET.

1. CMOS Inverter Characteristics

This section assesses the digital performance of different devices using circuit level simulation. The CMOS inverter circuit having load (P-MOS) and driver MOSFET (N-MOS) (as shown in Fig. 2(f)) is used to investigate the static and dynamic performance of different architectures using ATLAS 3D mixed mode simulation [9]. Various others logic circuits have also been investigated along with the inverter circuit. The various models used in the circuit simulation are same as the device level simulation models used during the calibration. Ideally, the output of the CMOS inverter circuit (i.e. the Voltage Transfer Characteristics VTCs) is either "Zero" or "One" i.e. high or Low in which only one of the transistor is conducting state at one time. However, in real devices transition region exists between "High" level and "Low" level. During the transition period, both the transistors are in conducting state and the current flows from input to ground leading to power dissipation. For fast digital performance, inverter circuit should exhibit narrow transition zone.

Fig. 3(a) illustrates that VTC of SON based inverter is

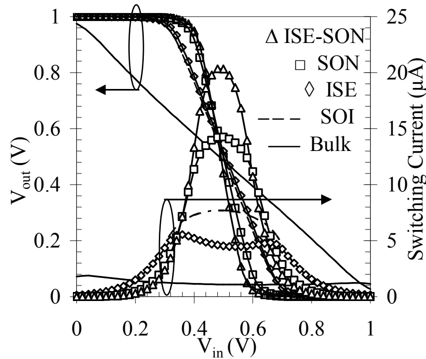


Fig. 3. (a) Variation of Voltage Transfer Characteristics (VTC) and switching current with input voltage for different devices for T=300K, V_{dd}=1.0 V, C_L=1 fF.

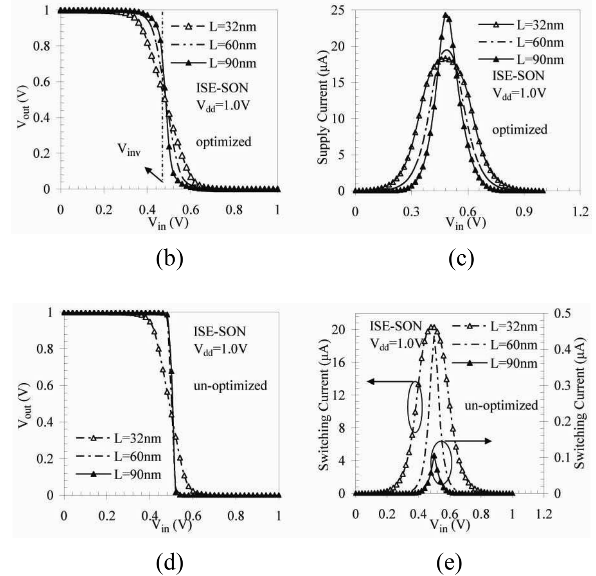


Fig. 3. Impact of channel length variation on (b) Voltage Transfer Characteristics, (c) switching current for optimized ISESON at different channel length, (d) VTC curve, (e) switching current for un-optimized ISE-SON at different channel length; T=300K, C_L=1 fF.

steeper than that of ISE and SOI architecture hence more preferable for digital applications. By using ISE-SON architecture to implement the inverter circuit, VTC becomes much more steeper due to improved sub-threshold performance [11]. The current drawn from the power supply during the high-to-low transition or vice versa, reaches its peak value with V_{in}=V_{inv} (V_{inv} is the point at which V_{in} and V_{out} are equal (as shown in Fig. 3(a)).

The sharpness in the peak of the switching current is a strong function of transition slope of VTC curve. The sharper peak in case of ISE-SON reflects narrow transition zone of VTC. The transition zone ΔV_{in} (i.e. the value of input voltage during which output makes a transition from 90% to 10% of final value (V_{outmax}) (i.e. V_{in} @ V_{outmax} (90%)-V_{in} @ V_{outmax} (10%))) is 0.14V for ISE-SON architecture however it is 0.18V for SON, 0.3Vfor ISE, 0.32 for SOI and 0.82V for bulk. The switching current of bulk MOSFET is almost flat thereby showing linear VTC which is due to high sub-threshold slope (S) and off state current (I_{off}) as shown in Fig. 2(b) Although, the maximum supply (switching) current is higher in case of ISE-SON as compared to other devices but it remains almost zero when either P-MOS or N-MOS is conducting i.e. either P-MOS or N-MOS which is mainly responsible for static power dissipation.

As the channel length decreases, sub-threshold slope of the device increases and hence the slope of VTC curve become less steeper (i.e. degrades) as shown in Figs. 3(b) and (d). However, the V_{inv} point remains same in Fig. 3(b) because threshold voltage (V_{th}) is optimized (i.e. V_{th}=0.25 V @ V_{ds}=0.5 V at different gate lengths). Similarly, as channel length decreases, peak value of the switching current decreases (in case of optimized device as shown in Fig. 3(c)) due to the reduction in saturation current level, however it increases in case of un-optimized device (shown in Fig. 3(e)) due to the enhancement in saturation current level. Thus we can get the lower power dissipation at lower gate lengths in optimized ISE-SON at different channel length. At higher device lengths, the transition zone gets sharper and switching current falls very sharply leading to steeper VTC curve The sharper peak (at higher device length) also reflects reduced CLM effect. Hence it can be easily concluded that, as we scale down the device dimensions, threshold voltage decreases and hence power dissipation increases along with the enhancement in the switching speed (given by g_m/C_{gg}). Thus there is a trade-off between switching speed and power dissipation.

As shown in Figs. 4(a) and (b), the adjustment of channel doping for the device optimization in bulk architecture shows superior device performance as compared to the metal gate work-function as shown in Fig. 2(f). As the channel length increases, drain current decreases (both I_{on} and I_{off}). However the reduction in drain current with channel length is significantly lower in ISE-SON (35%) architecture as compared to the bulk MOSFET (52%) thereby showing immunity against the

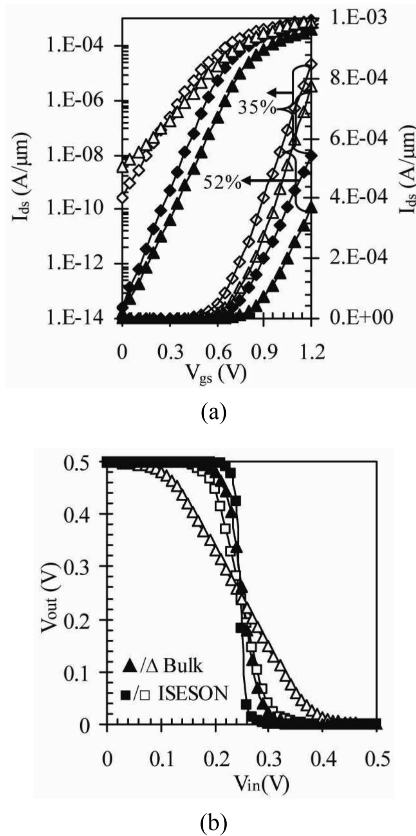


Fig. 4. Impact of channel length on (a) drain current (I_{ds}-V_{gs}), (b) inverter transfer characteristics for bulk and ISESON architecture optimized at the same threshold voltage of 0.25 V @ V_{ds}=0.5 V by varying the channel doping; Solid symbols: L=60 nm and hollow symbols: L=32 nm, □/■ for ISE-SON, Δ/▲ for bulk MOSFET.

channel length scaling. As the channel doping increases, leakage current of the device decreases, however this will also decrease the on-state current of the device and hence trans-conductance. Fig. 4(b) illustrates the impact of channel doping and the channel length on the performance of inverter characteristics. As the channel length increase, VTC curve becomes more steeper because of the reduction in sub-threshold slope. Further, because of the lower leakage current in bulk MOSFET (due to the enhancement in channel doping and reduction in metal gate work-function), the inverter transfer characteristics is also improved in Fig. 4(b) as compared to Fig. 3(a).

2. Immunity Against Process Variation in ISE-SON Architecture

The variation in the position of the Dielectric Pocket

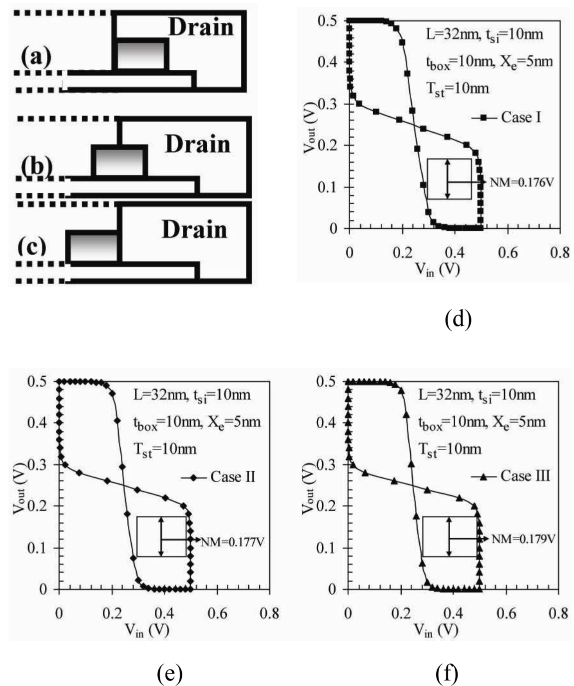
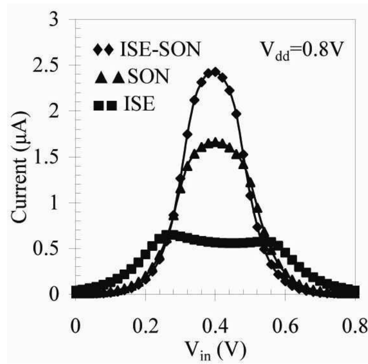


Fig. 5. Half cross-section view of the ISE-SON (a) DP inside the S/D region i.e. Case I, (b) DP at the middle of the channel and the S/D region i.e. Case II, (c) DP in the channel region at the S/D regions i.e. Case III. Impact of process variation on the Voltage Transfer Characteristics VTC (in butterfly shaped) of the ISE-SON, (d) Case I, (e) Case II, (f) Case III; T=300K, V_{dd}=0.5 V, C_L=1 fF.

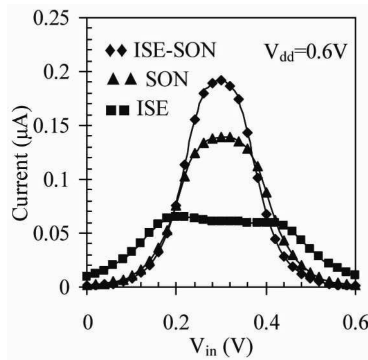
(DP) (as shown in Figs. 5(a)-(c)) is a serious issue while fabricating a un-conventional device architecture. Thus the tolerance of the inverter performance against the variation in the Dielectric Pocket position due to process variation or other factors is also studied The variation in the Dielectric Pocket position may negatively (or positively) affect the speed, stability of traditional CMOS inverter. As shown in Figs. 5(d)-(f), almost similar characteristics (noise margin) can be achieved in all the three cases (slightly improved in case III) with the variation in Dielectric Pocket position towards the channel region. The marginal improvement in VTC curve (or noise margin) is attributed to the fact that as the Dielectric Pocket shifts towards the channel, the effective channel thickness decreases thereby showing (marginally) improvement in VTCs due to enhance gate control.

3. Impact of Supply Voltage Scaling (V_{dd})

This sub-section addresses the impact of voltage



(a)



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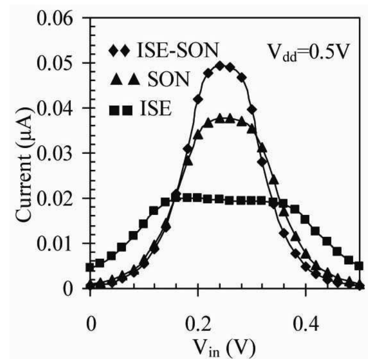
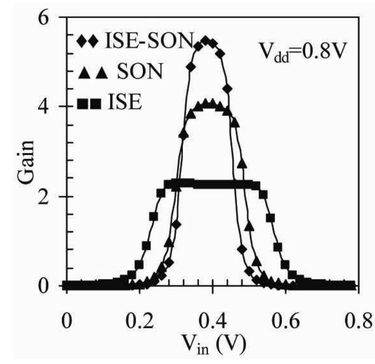
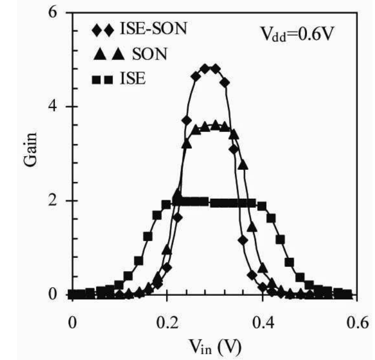


(c)

Fig. 6. Variation of switching current with input voltage of different architectures i.e. ISE-SON, SON and ISE for different supply voltage (a) V_{dd}=0.8 V, (b) V_{dd}=0.6 V, (c) V_{dd}=0.5 V for T=300K, L=32 nm, C_L=1 fF.



(a)



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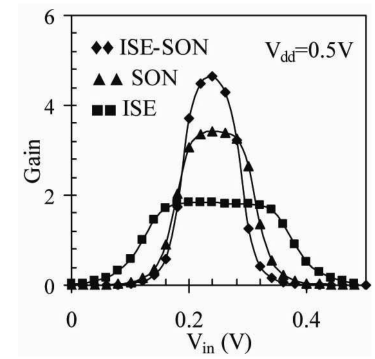


(c)

Fig. 7. Effect of supply voltage variation on the inverter gain of different architectures i.e. ISE-SON, SON and ISE (a) V_{dd}=0.8 V, (b) V_{dd}=0.6 V, (c) V_{dd}=0.5 V for T=300K, L=32 nm, C_L=1 fF.

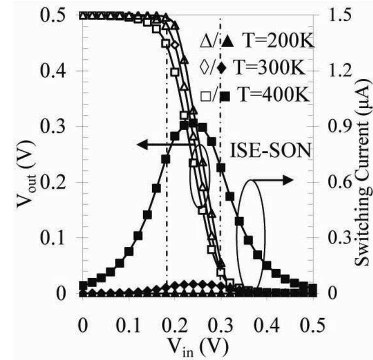
scaling on switching current for a CMOS inverter. According to Figs. 6(a)-(c), as V_{dd} decreases, maximum value of switching current decreases and the peak gets broadened due to change in threshold voltage with the applied drain bias (V_{dd}). As we scale the supply voltage V_{dd}, power dissipation also decreases due to reduction in switching current. The wide peak of switching current also reflects that high-to-low transition in the transfer characteristic occurs between large ranges of V_{in} (i.e. very large transition zone) and this is maximum in case of ISE followed by SON and ISE-SON for supply voltage even as low as 0.5V.

Power dissipation deteriorates with increase in supply voltage and it also affects the inverter gain which is calculated by taking the slope of the VTC curve ($-\partial V_{out}/\partial V_{in}$) [12-14]. According to Figs. 7(a)-(c), ISE-

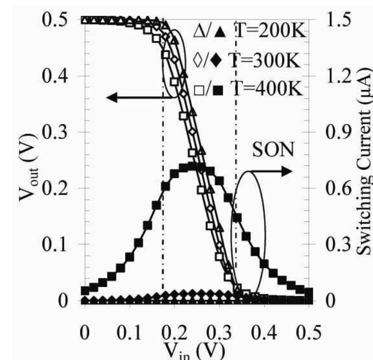
SON has the highest inverter gain in the transition region even for supply voltage down to 0.5V as compared to other architectures due to the higher device gain. Figure also shows that the degradation in inverter gain with V_{dd} scaling is 14% in ISE-SON however it is 16% in SON and 20% in ISE based inverter. This is mainly because of the reduced charge sharing between source and drain region in ISE-SON thereby showing immunity against the supply voltage scaling as compared to other devices.

3. Impact of Temperature Variation

Figs. 8(a)-(c) illustrate the impact of temperature variation on the performance of inverter circuit. As the operating temperature increases, VTC performance degrades (i.e. the width of the transition zone of the device increases) due to the enhancement in the leakage current and sub-threshold slope of the devices. With increases in temperature, maximum value of switching current as well as power dissipation also increases. In ISE-SON, transition region is smaller (ΔV_{in}) and hence showing faster switching speed. The immunity of ISE-SON against temperature variation is attributed to the presence of dielectric pillars (i.e. ISE) layer which increases the heat dissipation capability of the device [15, 16]. The percentage change in the maximum value of switching current is also lower in ISE-SON as compared to SON and ISE thereby showing lesser dependence of power dissipation on operating temperature. This is due to the fact that the degradation in sub-threshold performance with operating temperature is lower in ISE-SON [5] as compared to other devices.



(a)



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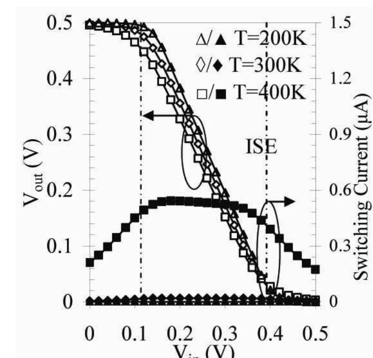

(c)

Fig. 8. Effect of temperature variation on the VTCs and supply voltage of different devices i.e. (a) ISE-SON, (b) SON, (c) ISE MOSFET respectively for V_{dd}=0.5 V, C_L=1 fF, L=32 nm.

5. Noise Margin

For high performance circuit operation, noise margin should be as high as possible [17, 18] so that the output signal will not be corrupted by the noise voltage present at the input level. Noise margin generally represents the robustness of the digital circuit in noisy environment and are describe as: 1) low state noise margin (NM_L) and 2) high state noise margin (NM_H).

NM_L is defined as the difference in maximum of low input voltage (V_{IL}) recognized by the input terminal and the maximum low output voltage (V_{OL}) at the output terminal [8].

$NM_L = V_{IL} - V_{OL}$

Similarly NM_H is defined as the difference in minimum high output voltage (V_{OH}) at the output terminal and the minimum high input voltage (V_{IH}) recognized by the input terminal [8].

$NM_H = V_{OH} - V_{IH}$

Thus the observed high noise margin (NM_H) and low noise margin (NM_L) of ISE-SON architecture are 0.246

and 0.22 respectively. It can be observed that similar trend can be observed for low noise margin or high noise margin. Thus the variation of low noise margin is plotted in Fig. 9, to demonstrate the immunity against the noise present at the input terminal.

As shown in Fig. 9, noise margin (i.e. low state noise margin NM_L) of ISE-SON is higher than that of the ISE and SON due to better high to low transition of the transfer curve as shown in Fig. 3(a). As channel length decreases, NM_L decreases but, the percentage change in noise margin with channel length is smaller in ISE-SON (19%) as compared to ISE (40%) and SON (29%). This is because the enhancement in sub-threshold slope and leakage current with the reduction in channel length is more pronounced in ISE and SON as compared to ISE-SON MOSFET. This results in improvement of noise margin immunity towards channel length scaling. Similar trend can be observed for the high state noise margin (NM_H) discussed in next section.

It can be also observed that noise margin (i.e. low state noise margin NM_L) of ISE-SON is higher than other devices even at lower drive voltage (V_{dd}) and the reduction in noise margin with V_{dd} scaling is also small in ISE-SON (30%) as compared to ISE (38%) and SON (36%). The immunity against supply voltage variation in ISE-SON with respect to other devices is mainly attributed to the lower carrier injection into channel region from the source side with V_{dd} (due to the reduce electrostatic coupling between S/D regions through the SON layer and side pillars) that results in (a) leakage current reduction and (b) suppression of DIBL.

The effect of supply voltage variation ($\pm$ 5%) (due to parameter variation such as tolerance of the voltage regulator) on noise margin i.e. at 0.45V, 0.5V and 0.55V is also shown in Fig. 9. The percentage change in noise margin with supply voltage ($\pm$ 5%) is significantly lower in ISE-SON (7%) as compared to ISE (34%) and SON (25%). This is due to fact that as the V_{dd} increases, S/D depletion region penetrates into the channel in ISE and SON. However in ISE-SON, due to the presence of side pillars and buried oxide layer, depletion region penetration into the channel region is less and hence shows more tolerance towards supply voltage variation as compared to SON and ISE.

Fig. 10 illustrates that the percentage degradation in noise margin (i.e. high state noise margin NM_H) with operating temperature is negligible in ISE-SON (3%) and SON (18%) as compared to ISE (53%). The reason behind this is that the impact of temperature variation on the R_{on} is less in ISE-SON as compared to SON and ISE architecture which we clearly observed from the table in inset of Fig. 10.

It can be observed that, as the operating temperature increases on-state resistance of the device increases. However, the enhancement in R_{on} with temperature is lower in ISE-SON followed by SON and ISE MOSFET. Hence it can be concluded that ISE-SON architecture has better immunity towards temperature variation as compared to SON and ISE MOSFET and can be easily operated at high temperature without much degradation in device performance.

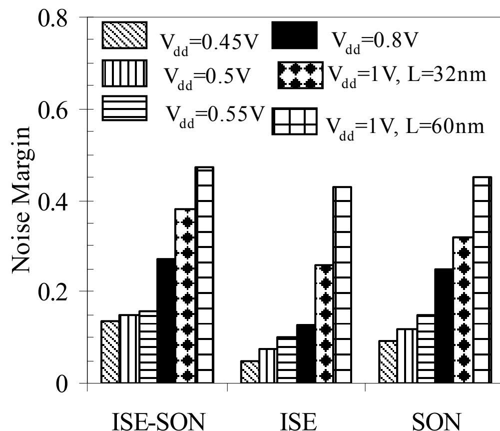

Fig. 9. Comparative study of noise figure (NM_L) for different channel lengths and supply voltage, C_L=1 fF, L=32 nm.

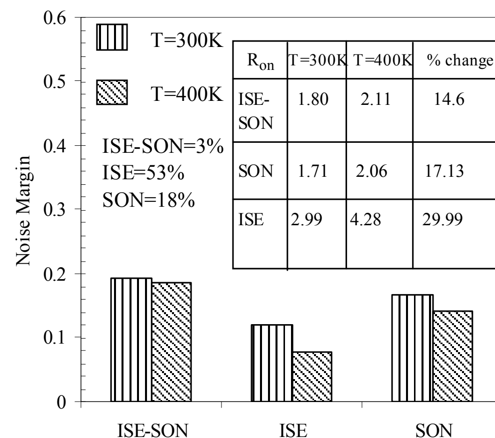

Fig. 10. Noise margin (NM_H) of the devices at different operating temperatures. Inset, Value of R_{on} (mΩ) at two different temperatures, for V_{ds}=0.5 V, V_{gs}=1.0 V, C_L=1 fF, L=32 nm.

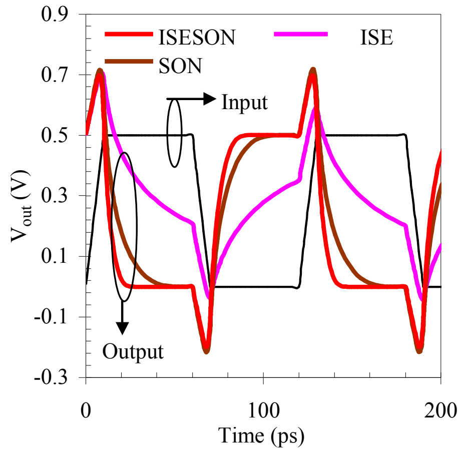

Fig. 11. Comparative study of transient response for different devices; V_{dd}=0.5 V, T=300K, L=32 nm, C_L=1 fF.

6. Transient Analysis

The switching characteristics of CMOS inverter are described in terms of the estimation of rise time and fall time values. Transient analysis is used to study the propagation delay of the circuit which is measured as the time difference between input transition (50%) and the 50% output level [19].

The overshoot in the output, as shown in Fig. 11, caused by the gate-drain capacitances and have a negative impact on the performance of the device and it can be clearly observed that the overshoot peak is maximum in case of SON followed by ISE and ISE-SON. The propagation delay of ISE-SON is 8.55ps which is 54% lower than the SON, and 81.3% from ISE. The lower propagation delay in ISE-SON is due to the reduction in parasitic capacitances and enhancement in the saturation current of the device. The higher propagation delay of the ISE based inverter is due to (a) smaller trans-conductance (g_m) and drive current and (b) lower output resistance as compared to SON and ISE-SON [5]. Unlike SON and ISE-SON, the capacitor does not discharge completely in ISE due to the high sub-threshold slope and lower output resistance (R_{out}) of the device. Thus, ISE-SON can be used for fast switching applications as compared to ISE, and SON architecture.

7. NAND and NOR Gate

Logic circuits such as NOR and NAND gate have been build using three different architectures are studied in this section to illustrate the capabilities of ISE-SON for reconfigurable logic systems. Figs. 12(a) and (b) shows that high-to-low or low-to-high propagation time deteriorated in case of ISE based NOR and NAND respectively gate as compared to SON based logic gates. The transient response of ISE-SON based logic gates is superior in comparison to other devices.

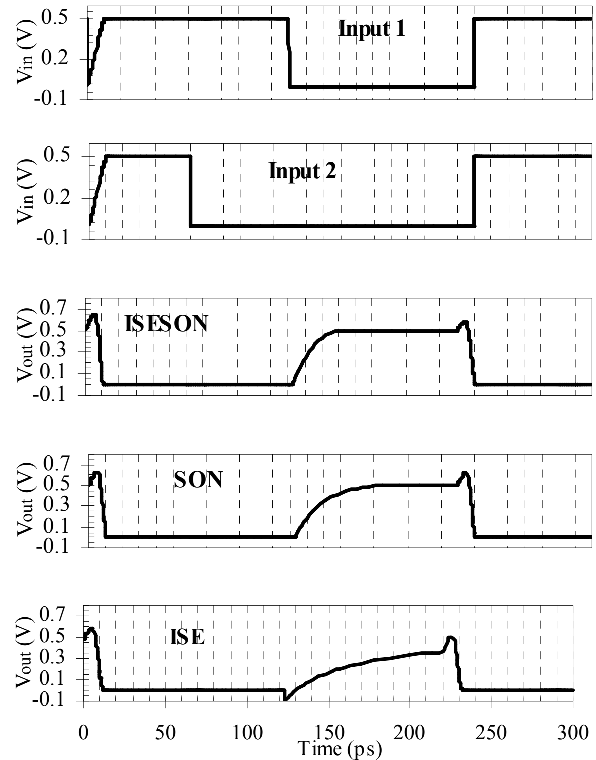

Fig. 12. (a) The simulated comparison of the timing diagram for NOR gate logic for T=300K, V_{dd}=0.5 V, L=32 nm, C_L=1 fF.

This is mainly because of the (a) high device gain (g_m/g_d) (b) lower leakage current and (c) improved sub-threshold slope (S) resulting in a reduction of charging and discharging time when connected to the load capacitor (C_L). The poor performance of the ISE based NOR and NAND gate is potentially due to the increased parasitic capacitance between the S/D regions and the substrate.

8. Ring Oscillator

Fig. 13 shows the output response of 3-stage ring oscillator commonly employed for measurement of circuit delay. From Fig. 13, it can be easily seen that ISE based oscillator provides maximum delay followed by

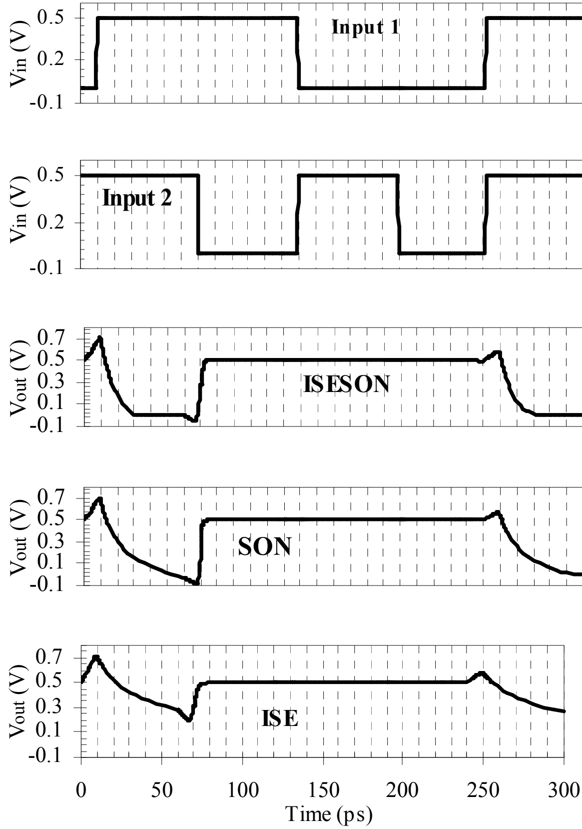

Fig. 12. (b) The simulated comparison of the timing diagram for NAND logic gate for T=300K, V_{dd}=0.5V, L=32 nm, C_L=1fF.

SON and ISE-SON based oscillator and hence, reducing the frequency of oscillation. The frequency of oscillation is given by $1/2n\tau$ where n is the number of inverter and τ is the delay between input and output cycle. The calculated frequency of oscillation for ISE-SON based oscillator is 5.99 GHz whereas it is 3.7 GHz for SON architecture. The improvement in ISE-SON based output is due to reduced input resistance and enhanced output resistance (R_{out}) as compared to other two devices [5]. The output of the ISE does not go completely to on state (i.e. 0.5V) due to the increased sub-threshold slope and leakage current (I_{off}) of the device (for both N-MOS and P-MOS) and hence cannot be used as a ring oscillator as compared to other devices.

The advantages of ISE-SON architecture as compared to SON MOSFET in terms of digital performance metrics are: (a) propagation delay of the ISE-SON based circuit is 54% lower than the SON MOSFET, (b) 13% higher noise margin in ISE-SON architecture is observed as compared to SON, (c) frequency of oscillation of ISE-

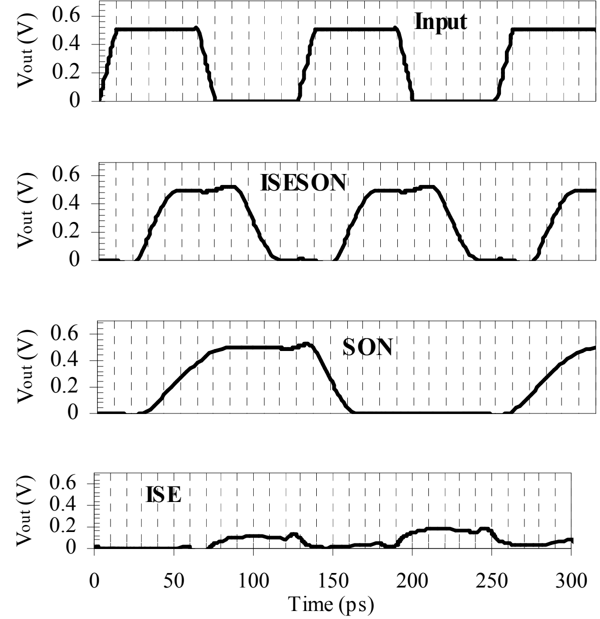

Fig. 13. The simulated comparison of 3-stage ring oscillator response for different architecture for V_{dd}=0.5 V, T=300K, L=32 nm, C_L=1fF.

SON based ring oscillator is 38% higher than the SON architecture, (d) reduction in noise margin with channel length scaling is lower in ISE-SON architecture i.e. 19% in ISE-SON and 29% in SON MOSFET, (e) the impact of temperature variation on noise margin is also marginal in ISE-SON architecture i.e. 7% as compared to SON MOSFET.

Thus the improvement in various dc and digital performance merits of the ISESON architecture discussed above justifies the structural modification in the conventional SON architecture having simpler proven fabrication process steps.

IV. CONCLUSIONS

In this paper, the dynamic and transient performance of CMOS inverter for different devices has been investigated using ATLAS 3D device simulator. ISE-SON shows better tolerance towards parametric variation for digital applications. The paper also looks into the temperature dependence of VTC of the inverter, supply voltage scaling, and noise margin which play a vital role in designing small sized VLSI circuits. It can be also observed that ISE-SON has potential to boost the speed of the device due to smaller propagation delay and also

more reliable as compared to other architectures. The advantage of ISE-SON in terms of the performance of logic circuits such as NAND, NOR and ring oscillator has been also studied in the present work. The improved performance of ISE-SON based inverter is due to the 1) smaller sub-threshold slope (S) and leakage current (I_{off}) 2) DIBL and 3) thin body minimizes the current leakage from source-to-drain as well as the substrate. Thus the paper demonstrates advantage of ISE-SON based CMOS inverter for low voltage digital application as compared to its counterparts. The ISE-SON architecture also shows better electrical performance at high operating temperature because of its lower leakage current.

ACKNOWLEDGMENTS

One of the authors (Vandana Kumari) would like to thanks University Grant Commission (UGC), Government of India, for financially supporting this research work.

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Vandana Kumari was born in New Delhi, India, in 1986. She received the B.Sc. (Gen) and M.Sc. degrees in Electronics from the University of Delhi, Delhi, India in 2006 and 2009, respectively. She is currently pursuing the Ph.D. degree in Electronics at the Semiconductor Device Research Laboratory, Department of Electronics Science, University of Delhi, and South Campus. Her current research interests are in the area of modeling and simulation of Insulated Shallow Extension, Silicon on Nothing and III-V compound semiconductor based MOSFETs. She has authored 22 papers in various international journals and conferences.

Manoj Saxena was born in New Delhi, India, on August 14, 1977. He received the B.Sc. (with honors), M. Sc., and Ph.D. degrees from the University of Delhi, New Delhi, in 1998, 2000, and 2006, respectively, all in electronics. He joined Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi in 2000 and presently he is Associate Professor. He has authored/coauthored 170 technical papers in international journals and conferences. His current research interests are in the areas of analytical modeling, design, and simulation of Optically controlled MESFET/MOSFET, silicon-on-nothing, insulated-shallow-extension, cylindrical gate MOSFET and Tunnel FET.

R. S. Gupta received the B.Sc. and M.Sc. degrees from Agra University, Agra, India, in 1963 and 1966, respectively, and the Ph.D. degree in electronic engineering from the Institute of Technology, Banaras Hindu University, Varanasi, India, in 1970. He has authored or coauthored more than 600 papers in various international and national journals and conference proceedings and supervised 46 Ph. D students. Currently he is Professor and Head in Department of ECE, Maharaja Agrasen Institute of Technology (GGIP University, Delhi). His current interests and activities include modeling and simulations of HEMTs, and advance MOSFET device designs.

Mridula Gupta received the B.Sc. degree in physics, the M.Sc. degree in electronics, the M.Tech. degree in microwave electronics, and the Ph.D. degree in optoelectronics from the University of Delhi, Delhi, India, in 1984, 1986, 1988, and 1998, respectively. Since 1989, she has been with the Department of Electronic Science, University of Delhi South Campus, New Delhi, India, where she was previously a Lecturer and is currently an Professor and with the Semiconductor Devices Research Laboratory. She has authored or coauthored more than 330 publications in international and national journals and conference proceedings. Her current research interests include modeling and simulation of MOSFETs, MESFETs, and HEMTs, for microwave applications.