Linearity of Hetero-Gate-Dielectric Tunneling Field-Effect Transistors

Hyun Kook Lee and Woo Young Choi

Abstract—**Linearity characteristics of hetero-gate-dielectric tunneling field-effect transistors (HG TFETs) have been compared with those of high-*k*-only and SiO_2-only TFETs in terms of IIP3 and P1dB. It has been observed that the optimized HG TFETs have higher IIP3 and P1dB than high-*k*-only and SiO_2-only TFETs. It is because HG TFETs show higher transconductance (g_m) and current drivability than SiO_2-only TFETs and g_m less sensitive to gate voltage than high-*k*-only TFETs.**

Index Terms—**Low power, linearity, tunneling field-effect transistor (TFET)**

I. INTRODUCTION

The progress of wireless communication technology has led to the rapid development of radio frequency (RF) devices. When there are more than two input frequencies, nonlinear RF devices generate high-order harmonics and intermodulation distortions. Thus, semiconductor devices for RF applications should maintain high linearity in order to suppress unwanted signals which have interfering frequencies which generate intermodulation distortions and high-order harmonics near the operating frequency [1]. Because linearity analysis requires complex circuitry at system level [2], device-level investigation will be more appropriate. In addition, due to the burgeoning demand for portable mobile devices, low-standby power consumption becomes one of the most important requirements. In order to save standby power consumption, it is necessary to lower supply voltage and subthreshold swing (SS). Thus, a tunneling FET (TFET) has been considered as one of the most promising low-power devices [3]. The earlier TFET studies focused on on-current boosting by introducing various materials and device structures [4-7].

Previously, we proposed hetero-gate-dielectric (HG) TFETs [4] and their RF performance and circuit applicability was discussed [8, 9].

This manuscript is contributed to the linearity of HG TFETs. TFETs are very promising in RF applications because their linearity is better than that of MOSFETs [10]. In this paper, the design of HG TFETs will be optimized by adjusting the length of high-*k* material under the gate ($L_{high\text{-}k}$) in terms of the linearity. The linearity of the optimized HG TFETs will be compared with that of high-*k*-only and SiO_2-only TFETs. High-*k*-only TFETs use only high-*k* dielectric as gate insulator and SiO_2-only TFETs use only silicon oxide as gate insulator. Third-order intercept point (IP3) and 1-dB compression point (P1dB) were used to evaluate the linearity of each kind of a TFET. For the investigation of IP3 and P1dB, transconductance (g_m) and its second derivative (g_{m3}) have been extracted.

II. SIMULATION CONDITION

To compare the linearity of HG TFETs with high-*k*-only and SiO_2-only TFETs, two-dimensional device simulation has been performed by using Silvaco ATLAS [11]. A nonlocal band-to-band tunneling model has been used. Band gap narrowing, Fermi statistics, Shockley-

Manuscript received May. 7, 2013; accepted Jul. 12, 2013
A part of this work was presented in Korean Conference on Semiconductors, Gangwon-do in Korea, Feb. 2013
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Read-Hall (SRH) recombination and Lombardi mobility models have been used in this simulation. Gate leakage current and quantum effect have been ignored. An abrupt source/drain junction profile has been assumed as shown in the previous works [4, 9].

Fig. 1 shows structures of HG, high-k-only and SiO_2-only TFETs. Device parameters used in this simulation are summarized in Table 1. The gate work function of each TFET has been adjusted to obtain the same I_{off}.

III. Results and Discussion

In order to evaluate the linearity of HG, high-k-only and SiO_2-only TFETs, IP3 and P1dB have been used. The important parameters that determine IP3 and P1dB are g_m and its derivatives. They are used to define the extrapolated input power (IIP3) where the third-order intermodulation term at output and fundamental one are equal. The mathematical expression of IIP3 is given by [2]:

$$IIP3 = \frac{2g_{m1}}{3g_{m3}R_S} = \frac{4\left(\frac{\partial I_d}{\partial v_g}\right)}{R_S\left(\frac{\partial^3 I_d}{\partial v_g^3}\right)} \quad (1)$$

where R_s=50Ω. The relationship between g_m and the drain current (I_D) is defined as

$$g_{mn} = \frac{1}{n!}\frac{\partial^n I_d}{\partial v_g^n} \quad (2)$$

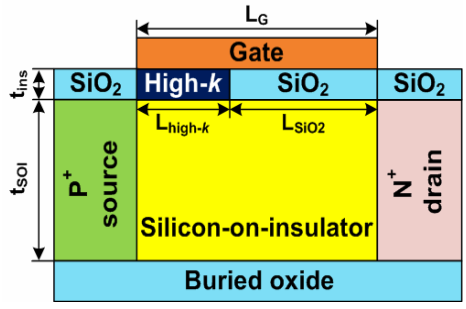
Previously, it has been reported that the linearity of transistors increases as g_m becomes less dependent on the gate voltage (V_G) variation, which leads to lower g_{m3} [12]. In order to make a g_m–V_G curve flat, I_D needs to rise linearly as V_G increases.

Transfer curves of HG, high-k-only and SiO_2-only TFETs are shown in Fig. 2(a). Compared with high-k-only and SiO_2-only TFETs, HG TFETs whose $L_{high\text{-}k}$ is 5 nm show higher on-current as shown in [4]. It is because a local minimum of conduction band edge (E_c) reduces the tunneling width (W_{TUN}) of HG TFETs. Also, HG TFETs are expected to show higher linearity if $L_{high\text{-}k}$ is optimized. Fig. 2(b) shows g_m-V_G curves of HG, high-k-only and SiO_2-only TFETs. HG TFETs show flatter g_m-V_G curves than high-k-only TFETs and higher g_m values than SiO_2-only TFETs. Higher g_m values and flatter g_m-V_G curves result in higher IIP3 value which indicates better linearity performance. For the optimization of HG TFETs in terms of linearity, the dependency of IIP3 and P1dB on $L_{high\text{-}k}$ needs to be investigated. They are extracted at maximum transconductance ($g_{m,max}$) condition except for the case of SiO_2-only TFETs. Because SiO_2-only TFETs have $g_{m,max}$ at high V_G around 4 V, their IIP3 and P1dB have been extracted at operating voltage: 2 V in this work.

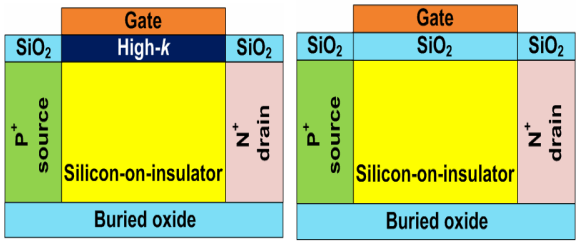
Fig. 3 shows the relationship between IIP3 and $L_{high\text{-}k}$. It is observed that HG TFETs show the highest IIP3

Table 1. Device parameters used for simulation

	HG TFET	High-k-only TFET	SiO_2-only TFET
L_G (nm)	50	50	50
t_{SOI} (nm)	30	30	30
t_{ins} (nm)	2	2	2
Source / drain doping conc. (cm^{-3})	10^{20}	10^{20}	10^{20}
Channel doping conc. (cm^{-3})	10^{15}	10^{15}	10^{15}
$L_{high\text{-}k}$ (nm)	5	50	X
k value of high-k dielectric	25	25	X

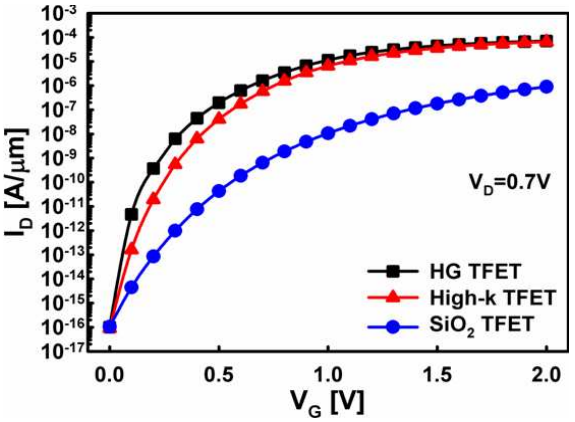


(a)

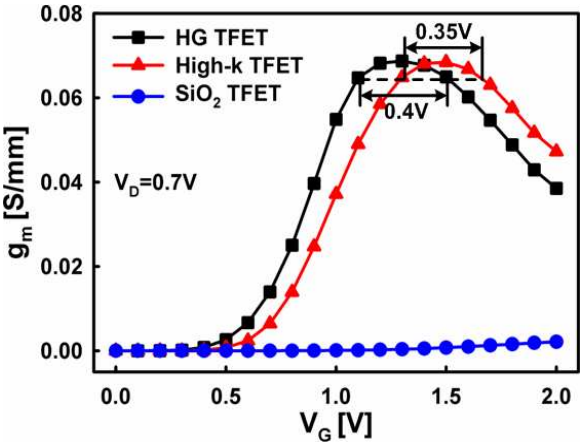


(b) (c)

Fig. 1. Schematic of an (a) HG, (b) high-k-only, (c) SiO_2-only TFET.



(a)



(b)

Fig. 2. (a) Transfer curves, (b) g_m–V_G curves of the HG, high-*k*-only and SiO_2-only TFETs.

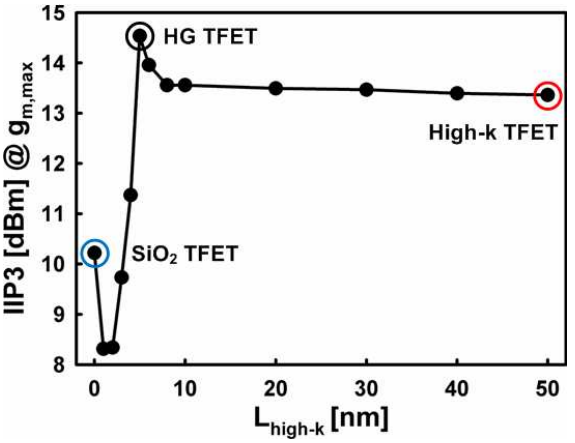


Fig. 3. IIP3 of HG TFETs as a function of L_{high-k}. IIP3 values have been extracted at the gate bias condition when g_m is maximum ($g_{m,max}$).

when L_{high-k} is ~5 nm. The optimized HG TFETs show ~30% higher IIP3 than high-*k*-only TFETs and >2x higher IIP3 than SiO_2–only TFETs. However, HG TFETs whose L_{high-k} is less than 4nm show lower IIP3 than SiO_2-only TFETs. It is because HG TFETs with low L_{high-k} show high g_{m3} though their g_m is higher than SiO_2-only TFETs. In case of optimized HG TFETs, W_{TUN} decreases abruptly around on set voltage and then it shows little change with the variation of V_G. On the other hand, W_{TUN} reduces continually at low L_{high-k} compared to optimized HG TFETs because a local minimum of E_c is shallow. As a result, HG TFETs with low L_{high-k} show sharper g_m-V_G curve which leads to higher g_{m3} value. Table 2 compares the linearity of the optimized HG TFETs with that of high-*k*-only and SiO_2-only TFETs in terms of IIP3 and P1dB. The optimized HG TFETs show higher linearity than high-*k*-only and SiO_2-only TFETs. It should be noted that the L_{high-k} value optimized in terms of linearity is the same as that optimized in terms of performance [4]. For more detailed analysis, the variation of IIP3 depending on L_{high-k} is shown in Fig. 4. HG TFETs whose L_{high-k} is 0 nm correspond to SiO_2-only TFETs and HG TFETs whose L_{high-k} is 50 nm correspond to high-*k*-only TFETs. It is well-known that IIP3 increases as g_m becomes higher and g_{m3} becomes lower. When L_{high-k} is 0 nm, both g_m and g_{m3} are small. Under this condition, linearity assessment is meaningless due to extremely

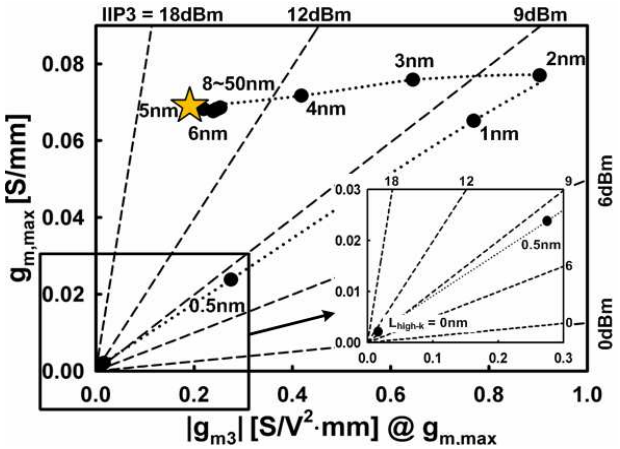


Fig. 4. Variation of the IIP3 value along with L_{high-k} as a function of g_m and g_{m3}. Optimized HG TFETs show higher linearity than high-k-only and SiO_2-only TFETs. A star represents the maximum IIP3 condition.

Table 2. Comparison of IIP3 and P1dB of the HG, high-*k*-only and SiO_2-only TFETs.at maximum transconductance ($g_{m,max}$)

Device type	HG TFET	High-*k*-only TFET	SiO_2-only TFET
IIP3 [dBm]	14.53	13.36	10.22
P1dB [dBm]	-4.64	-5.81	-8.95

small transconductance. As $L_{high\text{-}k}$ increases, both g_m and g_{m3} increase while IIP3 increases. When $L_{high\text{-}k}$ reaches 5 nm, the maximum IIP3 value is obtained and it is marked as a star in Fig. 4. As $L_{high\text{-}k}$ increases beyond 10 nm, IIP3 values are saturated to those of high-*k*-only TFETs. Higher IIP3 of HG TFETs is attributed to the gate controllability improved by high-*k* dielectric. It significantly reduces W_{TUN} and increases g_m of TFETs around the operation voltage. However, the sole increase of relative permittivity of high-*k* dielectric is not a solution to higher linearity because it increases g_{m3} as well as g_m. Thus, $L_{high\text{-}k}$ and the relative permittivity of high-*k* dielectric should be optimized in terms of both g_m and g_{m3}.

IV. CONCLUSIONS

The linearity of HG TFETs has been compared with the high-*k*-only and SiO_2-only TFETs. HG TFETs have been optimized in terms of the linearity with the variation of $L_{high\text{-}k}$. It has been found that the optimized HG TFETs have higher linearity than high-*k*-only and SiO_2-only TFETs because the optimized HG TFETs have higher g_m than SiO_2-only TFETs and flatter g_m–V_G curves than high-*k*-only TFETs. Also, it has been observed that HG TFETs have the same optimization condition in terms of both on-current and linearity. It is promising that HG TFETs will be used for wireless RF systems.

ACKNOWLEDGMENTS

This work was supported in part by the NRF of Korea funded by the MSIP under Grant 2013-027714 (Mid-Career Researcher Program), in part by the NIPA funded by the MSIP under Grant NIPA-2013-H0301-13-1007 (University ITRC Support Program), in part by the MOTIE/KSRC under Grant 10044842 (Future Semiconductor Device Technology Development Program) and in part by the Sogang University Research Grant of 2012.

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