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# Behavioral Current-Voltage Model with Intermediate States for Unipolar Resistive Memories

**Young Su Kim and Kyeong-Sik Min**

***Abstract*—In this paper, a behavioral current-voltage model with intermediate states is proposed for analog applications of unipolar resistive memories, where intermediate resistance values between SET and RESET state are used to store analog data. In this model, SET and RESET behaviors are unified into one equation by the blending function and the percentage volume fraction of each region is modeled by the Johnson-Mehl-Avrami (JMA) equation that can describe the time-dependent phase transformation of unipolar memory. The proposed model is verified by the measured results of $TiO_2$ unipolar memory and tested by the SPECTRE circuit simulation with CMOS read and write circuits for unipolar resistive memories. With the proposed model, we also show that the behavioral model that combines the blending equation and JMA kinetics can universally describe not only unipolar memories but also bipolar ones. This universal behavioral model can be useful in practical applications, where various kinds of both unipolar and bipolar memories are being intensively studied, regardless of polarity of resistive memories.**

***Index Terms*—Unipolar resistive memories, behavioral model, Johnson-Mehl-Avrami equation**

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## I. INTRODUCTION

Resistive memories have been developed for many years because they have been considered to be able to replace current DRAM and FLASH memories in future. Though underlying physics are still not fully understood, some behavioral models have been proposed for circuit simulators such as HSPICE and SPECTRE. Generally speaking, resistive memories can be categorized into two types that are bipolar and unipolar, respectively. For bipolar resistive memories, many behavioral models that are based on the state variable equations were developed [1-4]. However, very few models were proposed for unipolar resistive memories compared with bipolar ones [5-7]. The SPICE macromodel for unipolar memories that was proposed by Lee et al [5] cannot describe the intermediate resistance values between SET and RESET states accurately. If we try to consider intermediate states in the macromodel, many complicated sub-blocks such as comparators should be added to the model. This complicated macromodel with intermediate states needs a long simulation time and a large amount of main memory for the simulation.

As a different modeling approach, the behavioral unipolar memory model that was formulated by double-well potential function was developed [6]. Though the behavior model does not need any circuit block, it is described by very complex mathematical equations [6]. Moreover, the intermediate states between SET and RESET states that are very important in realizing analog memory applications such as neuromorphic systems were not considered in the behavioral model formulated by the double-well potential [6].

In this paper, we will propose a new behavioral

current-voltage model with intermediate states that is implemented by Verilog-A for unipolar memories [7]. The proposed model will be verified by the measurement results of $TiO_2$ unipolar memory [8] and tested by the SPECTRE circuit simulation with CMOS read and write circuits for unipolar memories. With the new behavioral model, we will extend the concept of combing the blending equation [9, 10] and Johnson-Mehl-Avrami (JMA) kinetic equation [11] to bipolar memories. Thus, in this paper, we will show that the proposed model can universally describe the current-voltage relationship of both unipolar and bipolar memories with intermediate states, regardless of polarity. The universal behavioral model can be more useful than unipolar-only or bipolar-only model in practical applications because both unipolar and bipolar resistive memories are being studied and developed for various analog and digital applications nowadays. In terms of materials and processing technologies of resistive memories, many scholars are still trying to find the best one for resistive memory applications regardless of polarity of memory charactersistics. For them, the universal behavioral model proposed in this paper can be used to compare and analyze the electrical characteristics and behaviors between various materials and processing technologies. Furthermore, the universal resistive memory model can help circuit engineers design various resistive memory circuits regardless of the polarity of memories.

## II. Behavioral Model with Intermediate States between SET and RESET for Unipolar Resistive Memories

To describe the current-voltage behavior in both SET and RESET regions of unipolar resistive memories, we assume the following blending equation that can merge two regional equations into a united expression as shown below [9, 10].

$$i(t) = f_{SET}(v(t)) \times \exp\left( (1 - C_{SET}) \cdot Ln\left( \frac{f_{RESET}(v(t))}{f_{SET}(v(t))} \right) \right) \quad (1)$$

Here $C_{SET}$ is a percentage volume fraction of SET region that varies between 0 and 1 [9]. In Eq. (1), $f_{SET}(v(t))$ means the current-voltage relationship in SET state and $f_{RESET}(v(t))$ means the current-voltage relationship in RESET state. v(t) and i(t) represent voltage and current of resistive memories, respectively. $f_{SET}(v(t))$ and $f_{RESET}(v(t))$ can be described by $a_1 \cdot \sinh(b_1 \cdot v(t))$ and $a_2 \cdot \sinh(b_1 \cdot v(t))$, respectively [12]. Here the parameters of $f_{SET}(v(t))$ and $f_{RESET}(v(t))$ that are used in this paper are $a_1$ = 5 [A], $b_1 = 10^{-3}$, $a_2 = 10^{-4}$ [A], and $b_2$ = 3, respectively. When $f_{SET}(v(t))$ and $f_{RESET}(v(t))$ seem very linear, we can use simple linear current-voltage relationships of $i(t) = v(t) / R_{SET}$ and $i(t) = v(t) / R_{RESET}$, respectively, for $f_{SET}(v(t))$ and $f_{RESET}(v(t))$. $R_{SET}$ and $R_{RESET}$ mean LOW resistance at SET state and HIGH resistance at RESET state, respectively.

In Eq. (1), when $C_{SET}$ is 1, the unipolar resistive memory is dominated by $f_{SET}(v(t))$, where the resistive memory is in SET state. On the contrary, when the resistive memory is in RESET state, it can be described by $f_{RESET}(v(t))$ because $C_{SET}$ in Eq. (1) is 0. Between SET and RESET, there can be some intermediate states, where $C_{SET}$ is larger than 0 but smaller than 1.

Let's assume that we apply a voltage or current pulse to $TiO_2$ unipolar resistive memory that is shown in Fig. 1(a), where TE and BE are the top and bottom electrode, respectively. As a current or voltage stress accumulates in $TiO_2$, the state variable that is represented by $C_{SET}$ in Eq. (1) starts to be changed with respect to time thereby the conductivity of unipolar resistive memory changes, too. Fig. 1(b) shows briefly the SET and RESET operation in unipolar memories. $I_{TH,RESET}$ and $V_{TH,RESET}$ are the threshold current and threshold voltage for SET-to-RESET transition, respectively. $I_{COMP}$ is the compliance current that limits a maximum allowable current through resistive memory. $V_{TH,SET}$ is the threshold voltage for RESET-to-SET transition in resistive memory. If the applied current exceeds $I_{TH,RESET}$, $C_{SET}$ becomes lower to 0. On the contrary, if the applied voltage of unipolar memory exceeds $V_{TH,SET}$, the state changes from RESET to SET.

It is known that the percentage volume fraction of SET region is changed with respect to time if the unipolar memory is applied by a voltage or current stress. The measurement by S. Song et al [13] indicates that phase transformation that happens in $TiO_2$ unipolar memories could be described by the Johnson-Mehl-Avrami (JMA)

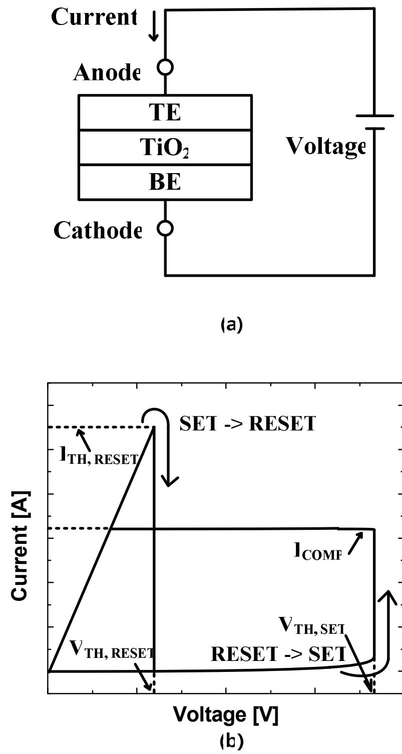


**Fig. 1.** (a) A cross-sectional view of $TiO_2$ unipolar resistive memories. TE and BE mean the top electrode and the bottom electrode, respectively, (b) Current-voltage relationship of SET and RESET operation in unipolar memories.

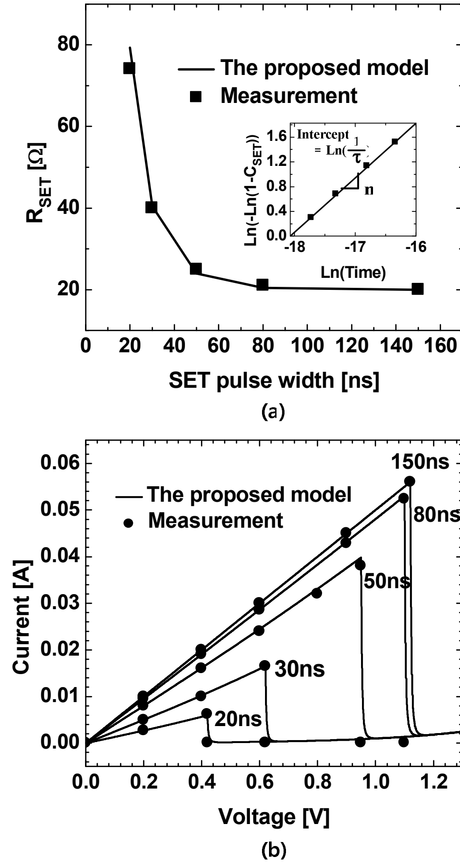


**Fig. 2.** (a) Comparison of the proposed model and measured data [8]. The inset figure shows Ln(-Ln(1-$C_{SET}$)) versus Ln(time) plot. Here 'n' in Eq. (2) can be extracted by the slope of Ln(-Ln(1-$C_{SET}$)) versus Ln(time) relationship. The Ln(1/τ) can be calculated by the y-intercept point of Ln(-Ln(1-$C_{SET}$)) with respect to Ln(time), (b) Comparison of the proposed behavioral model and the measured data that are obtained by Choi et al [8].

equation [11]. Thus, according to the JMA equation, the percentage volume fraction of RESET region, 1-$C_{SET}$, can be expressed with

$$
\begin{aligned}
1 - C_{SET} &= K_0 e^{-\frac{t^n}{\tau}} && \text{for} \quad v(t) \geq V_{TH,SET} \\
&= 1 - K_1 e^{-\frac{t^n}{\tau}} && \text{for} \quad V_{TH,RESET} \leq v(t) < V_{TH,SET} \\
&= 0 && \text{for} \quad v(t) < V_{TH,RESET}
\end{aligned}
\tag{2}
$$

Here $K_0$ and $K_1$ are the coefficients for accounting for the initial values of 1-$C_{SET}$. If we assume the full RESET state at the initial point, $K_0$ is 1. Otherwise, assuming the full SET state, $K_1$ should be 1. In Eq. (2), τ means the time constant of phase-transformation in unipolar memories. The value of τ in this paper is $1.08\times10^{-8}$ [sec]. In Eq. (2), 'n' means Avrami exponent. Here the value of 'n' is 1. $V_{TH,SET}$ and $V_{TH,RESET}$ are threshold voltages for SET and RESET, respectively.

Fig. 2(a) compares the measured $R_{SET}$ and the proposed model with respect to the SET pulse width. As the SET pulse width increases, $R_{SET}$ becomes smaller. If the SET pulse width is longer than 80 ns, $R_{SET}$ begins to saturate around 20 Ω. Here the measured data obtained by Choi et al [8] that are shown in rectangle symbols are in good agreement with the proposed model that is shown in solid line. Here the inset figure in Fig. 2(a) shows that the plot of Ln(-Ln(1-$C_{SET}$)) versus Ln(time) has a very good linearity. This good linearity means that the phase transformation in $TiO_2$ unipolar resistive memories follows the JMA equation well. Fig. 2(b) compares the proposed behavioral model and the measured data that are obtained by Choi et al [8]. For different intermediate states, the proposed model shows good agreement with the measured data, as shown in Fig. 2(b).

## III. Circuit Simulation Results with the Proposed Behavioral Model

The transient simulation of unipolar resistive memories is shown in Figs. 3(a)-(d). Here, the voltage waveform in Fig. 3(a) is applied to a resistive memory with the proposed behavioral model. Here, RESET voltage with the amplitude of 1.5 V and the pulse width of 150 ns is applied first. And, then, SET voltage with the amplitude of 2.5 V and the pulse width of 150 ns comes next. Fig. 3(b) shows the percentage volume fraction of SET region $C_{SET}$ that is changed by the applied voltage with respect to time. After the first RESET pulse, ($1-C_{SET}$) becomes 1 that means the resistive memory is in full RESET state. And, then, ($1-C_{SET}$) becomes 0 by the first SET pulse thereby the resistive memory moves to full SET state. In Fig. 3(a), after the first RESET and SET pulses, the second RESET and SET pulses comes again. From Fig. 3(a), we can know that RESET pulses are long enough to change the resistive memory to full RESET state. However, SET pulses have different pulse widths thereby the resistive memory can be changed to different intermediate states, where the percentage volume fraction of SET region is between 0 and 1. Fig. 3(c) shows the current waveform of resistive memory. Resistance values that are changed according to the applied voltage in Fig. 3(a) are shown in Fig. 3(d). Here we can know that resistance values after RESET pulses become as large as $R_{RESET}$. The resistance values after various SET pulses that

have different pulse widths can be different each other by the pulse width duration. These different resistance values indicate that there are intermediate states between SET and RESET states. Fig. 3(e) shows a block diagram of the read and write circuits for the proposed behavioral Verilog-A model of unipolar resistive memories. In Fig. 3(e), when $S_1$ is closed, the memristive behavioral model is connected to the read circuit. When $S_2$ is closed, the write circuit can change memristance of the behavioral model that is calculated with Eqs. (1) and (2).

To show that the proposed behavioral model can universally describe not only unipolar resistive memories but also bipolar ones, we compared the proposed model with various measured data that are obtained by different bipolar memories [12, 14-17] in Figs. 4(a)-(d). Here one more thing to note is that various materials including

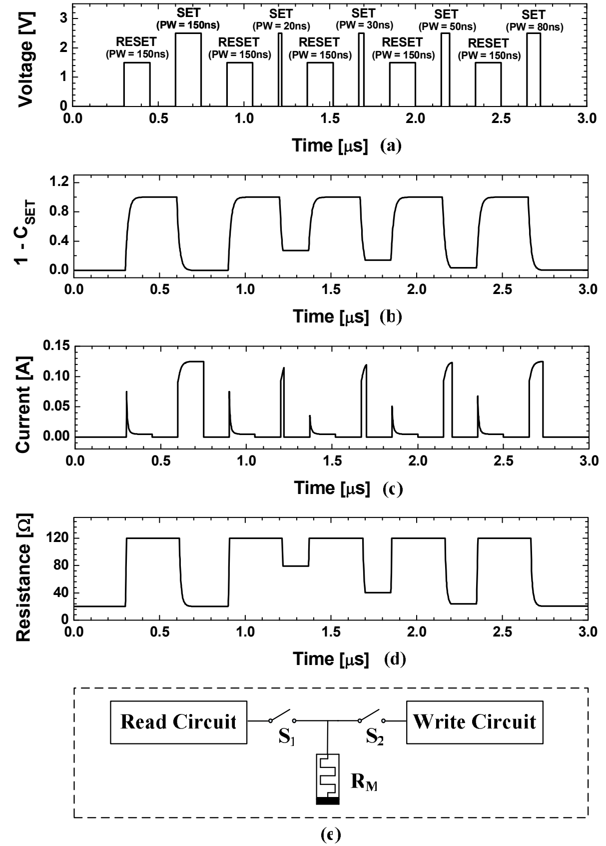


**Fig. 3.** (a) Voltage waveform of RESET and SET pulses. Here all RESET pulse widths are 150 ns. For SET pulse, the first pulse width is as long as 150 ns to change the resistive memory from RESET to full SET state. The second, third, fourth, and fifth are 20 ns, 30 ns, 50 ns, and 80 ns, respectively. By applying different SET pulse widths, the resistive memory can be changed to intermediate states, where intermediate SET resistance is larger than SET resistance with full SET state, (b) Here $1-C_{SET}$ means the percentage volume fraction of SET region that is changed by the applied RESET and SET pulses, (c) Current waveform of resistive memory, (d) Resistance waveform of resistive memory, (e) Block diagram of the read and write circuits for the proposed behavioral Verilog-A model of unipolar resistive memories

$TiO_2$ were verified by the proposed model. For example, Fig. 4(a) compares the behavioral model with the silver chalcogenide based resistive memory that contains $Ge_2Se_3$ and Ag [12, 14]. Figs. 4(b) and (c) show the measured data from $TiO_2$ based resistive memories that have bipolar switching characteristics [12, 15, 16]. The measured data in Fig. 4(d) were obtained from a layered device with co-sputtered Ag and Si active layers. Here Ag/Si mixture ratio can be changed to form an Ag-rich region or a Si-rich region thereby the conductivity of Ag/Si mixed layer can be variable [12, 17].

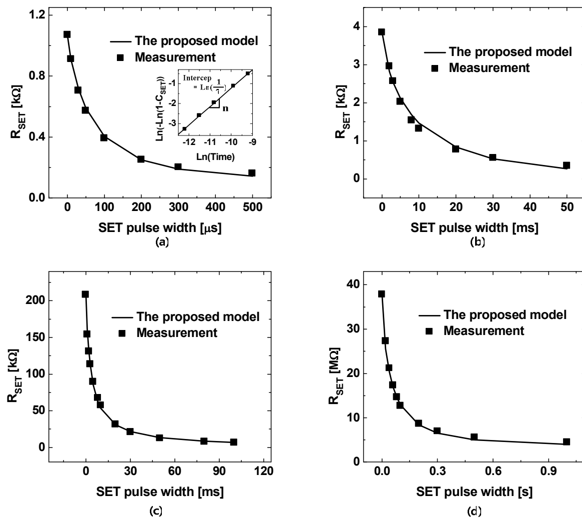


**Fig. 4.** Comparison of the proposed behavioral model and various devices (a) The measured device is silver chalcogenide based bi-polar resistive memory that contains $Ge_2Se_3$ and Ag [12, 14], (b) The measured device is $TiO_2$ crossbar resistive memory with bi-polar hysteresis loops [12, 15], (c) The measured device is another bi-polar $TiO_2$ memristive switching memory [12, 16], (d) The measured device is made by co-sputtering Ag and Si active layers, where Ag/Si mixture ratio can be changed to form a Ag-rich region or a Si-rich region [12, 17].

**Table 1.** Comparison of the previous models [5, 6] and this work [7]

| | The previous model [5] | The previous model [6] | This work [7] |
|---|---|---|---|
| Spice macromodel vs. Behavioral model | Spice macromodel | Behavioral model | Behavioral model |
| Complexity of the macromodel or behavioral model | Complicated circuit blocks | Complex mathematical equation | Simple |
| Intermediate states | Considered but many complicated circuit blocks added | Not considered | Considered |
| Be able to universally describe both uni-polar and bi-polar memories | Tested only for unipolar memories | Tested only for unipolar memories | Tested for both unipolar and bipolar memories |

In all the comparison with different materials and different processing technologies, the proposed behavioral model shows very good agreement with the measured data [12, 14-17]. In Fig. 4(a), $R_{SET}$ changes from 1070 Ω to 162 Ω with a dynamic range as wide as one order of magnitude. Fig. 4(c) shows wider dynamic range of $R_{SET}$ which is as wide as two orders of magnitude than one order of magnitude in Fig. 4(a). Fig. 4(c) indicates that the proposed behavioral model can fit to the measured data very well in spite of this wide dynamic range of $R_{SET}$ variation. Though the dynamic range of $R_{SET}$ in Fig. 4(b) is much smaller than Figs. 4(a) and (c), the calculated memristance values in Fig. 4(b) show good agreement with the measurement [12, 15]. In Fig. 4(d), the pulse width becomes as long as almost 1 sec. Despite this long programming pulse, the calculated $R_{SET}$ values in Fig. 4(d) are in good agreement with the measurement.

Finally, we summarized the proposed model in comparison with the previous ones in Table 1.

## IV. CONCLUSIONS

In this paper, we proposed the behavioral current-voltage model with intermediate states that was implemented by Verilog-A for unipolar resistive memories. The proposed model was verified by the measurement results of $TiO_2$ unipolar memory and tested by the SPECTRE circuit simulation with CMOS read and write circuits for unipolar resistive memories. With the proposed model, we also showed that the behavioral model that combines the blending equation and JMA kinetics could universally describe not only unipolar memories but also bipolar ones. This universal behavioral model can be useful in practical applications, where various kinds of unipolar and bipolar memories are being intensively studied, regardless of polarity of resistive memories.

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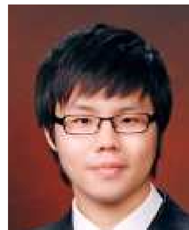

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