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초음파 의료 영상시스템용 고집적 아날로그 Front-End 집적 회로

(A Highly-Integrated Analog Front-End IC for Medical Ultrasound Imaging Systems)

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(Aditya Banuaji and Hyouk-Kyu Cha©)

요 약

초음파 의료 영상 응용 분야를 위한 고전압 고집적 아날로그 front-end 집적회로를 0.18-μm 표준 CMOS 반도체 공정을 이용하여 구현하였다. 제안 된 아날로그 front-end 집적회로는 2.6 MHz에서 15 Vp-p 전압까지 동작하는 트랜지스터 stacking 구조를 이용한 고전압 펄서와, 저전압에서 동작하는 저잡음 transimpedance 증폭기, 그리고 송신부와 수신부의 분리를 위한 고전압 차단 스위치로 구성되어 있다. 설계 된 집적회로는 0.15 mm^2 이하의 작은 면적을 사용함으로써 휴대용 영상 시스템을 포함한 다중 어레이 초음파 의료 영상 시스템에 적용이 가능하다.

Abstract

A high-voltage highly-integrated analog front-end (AFE) IC for medical ultrasound imaging applications is implemented using standard 0.18-μm CMOS process. The proposed AFE IC is composed of a high-voltage (HV) pulser utilizing stacked transistors generating up to 15 Vp-p pulses at 2.6 MHz, a low-voltage low-noise transimpedance preamplifier, and a HV switch for isolation between the transmit and receive parts. The designed IC consumes less than 0.15 mm^2 of core area, making it feasible to be applied for multi-array medical ultrasound imaging systems, including portable handheld applications.

Keywords : ultrasound, analog front-end, pulser, preamplifier, switch

Ⅰ. Introduction

The interest in the development of ultrasound medical imaging systems has grown in the past few years due to its low cost, real-time monitoring capability, and harmless characteristics with decent performance in comparison to other imaging methods[1]. Modern ultrasound imaging systems are becoming more complex and powerful with large number of transducer arrays, and at the same time portable hand-held type devices are being developed for hospital and home usage. In both cases, the physical area of each single-channel interface front-end IC has to be minimized when considering multi-channel realization and integration with a large-array transducer. Previous interface IC

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solutions utilize high-voltage (HV) CMOS process options[2] in order to implement analog front-end (AFE) IC as ultrasound systems require high-voltage operation in the transmit path to drive the transducer for maximum acoustic pressure generation. However, in comparison to regular CMOS transistors, such HV transistors consume much amount of die area which greatly increase the size of overall multi-array interface IC.

Ⅱ. System Architecture

The block diagram of a typical multi-array ultrasound imaging system is shown in Fig. 1. The transducer elements interface with the multi-channel analog front-end, consisting of HV pulsers, low-noise preamplifiers, and HV protection switches to isolate the low-voltage (LV) circuits in order to prevent breakdown. On the transmitter side, the HV pulsers are driven by LV trigger pulses generated by the transmit beamformer with controlled delays. On the receiver part, receive beamformer is used to process the returning echo signals and ultimately construct an image from the pulse-echo information.

This work includes the single-channel analog front-end part, which is designed to interface with the capacitive micromachined ultrasound transducer (CMUT)[3]. The CMUT is gaining much interest from the ultrasound community due to its superior frequency characteristics, simpler fabrication for large-arrays, and ease of integration with interface ICs, in comparison to the dominantly-used piezoelectic transducer.

The designed AFE IC is targeted for ultrasound medical imaging in a highly integrated needle device for obstetrics and gynecology applications. The required transmit pulse voltage is 15-V, so that sufficient acoustic pressure is generated from the CMUT device at 2.6 MHz center frequency in immersion. In the receiver side, a low-supply voltage of 1.1 V is used for the preamplifier in order to minimize the power consumption without affecting its performance. A HV switch is used in between the Tx and Rx for isolation. To achieve high integration, all the proposed HV circuits utilize transistor stacking so that standard CMOS transistors may be used to process HV signals above the technology limits.

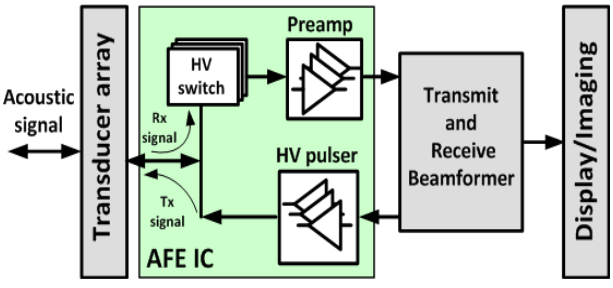

그림 1. 초음파 의료 이미징 시스템의 전체적인 블록도
Fig. 1. Overall block diagram of the ultrasound imaging system.

Ⅲ. Circuit Design

1. HV Pulser

The architecture of the overall HV pulser is shown in Fig. 2. The primary requirement of the pulser is to generate a HV pulse signal without compromising the reliability of the operating transistors in the circuit. The overall pulser consists of a 1.8-to-3.3 V level-shifter, which converts the externally generated 1.8 Vp-p trigger

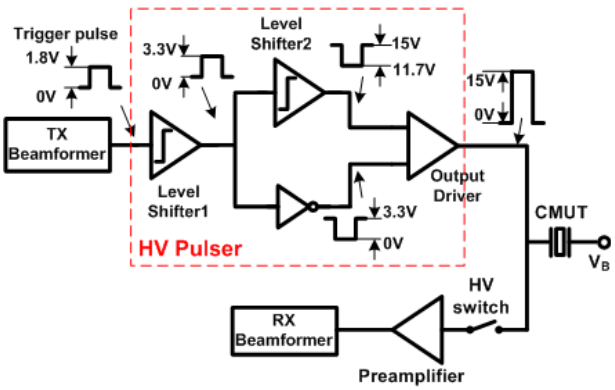

그림 2. 고전압 펄서의 전체 블록도
Fig. 2. Overall architecture of the HV pulser.

signal to swing between 0 and 3.3 V at the output. Then the 3.3 Vp-p signal is divided into two separate paths. The upper path contains a second level-shifter to convert the signal to swing between 11.7 V and 15 V in order to drive the gate of PMOS transistor of the output driver. The lower path, on the other hand, goes through inverter-based buffers to drive the gate of NMOS transistor of the output driver. The output driver is followed by the CMUT element where the CMUT is driven with a 15 Vp-p HV pulse so that an ultrasound signal with sufficient acoustic pressure is generated for propagation through the acoustic medium.

Previous pulsers use double-diffused MOS (DMOS) transistors[2, 4], illustrated in Fig. 3, in the output driver and the level-shifter blocks in order to sustain large voltages without device breakdown. In the proposed output driver design, shown in Fig. 4, all the DMOS transistors have been replaced by stacked standard 3.3-V CMOS transistors in order to minimize the area and reduce the process cost. Five stacks of NMOS transistors, MN1-MN5, and PMOS transistors, MP1-MP5, are used to support up to 15-Vp-p output swing. In addition, dynamic biasing circuitry (inside dotted rectangle) is used to make sure appropriate voltages are applied to the gates of the stacked transistors during ON-OFF transitions so that 15 V is distributed among the stacks and all the voltages in the terminals are maintained within the technology limits. The basic ON-to-OFF and OFF-to-ON push-pull operation of the dynamically-biased stacked output driver is similar to that presented in [5~6] with additional stacks to support higher voltage swing. In addition, some modifications to support the integration with the HV switch and preamplifier part have been done along with the inclusion of power down circuitry consisting of MP6, MP7, and INV1 to power down the bottom

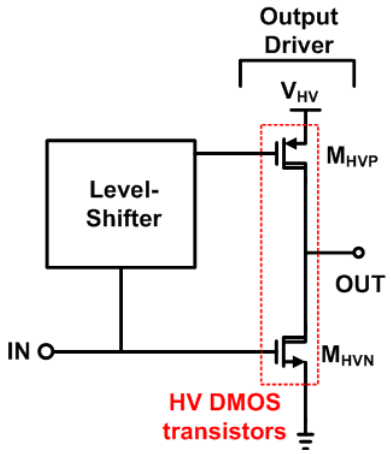

그림 3. DMOS 트랜지스터를 이용한 기존의 고전압 펄서의 회로도 [4]

Fig. 3. Simplified circuit schematic of previous HV pulser using DMOS transistors [4].

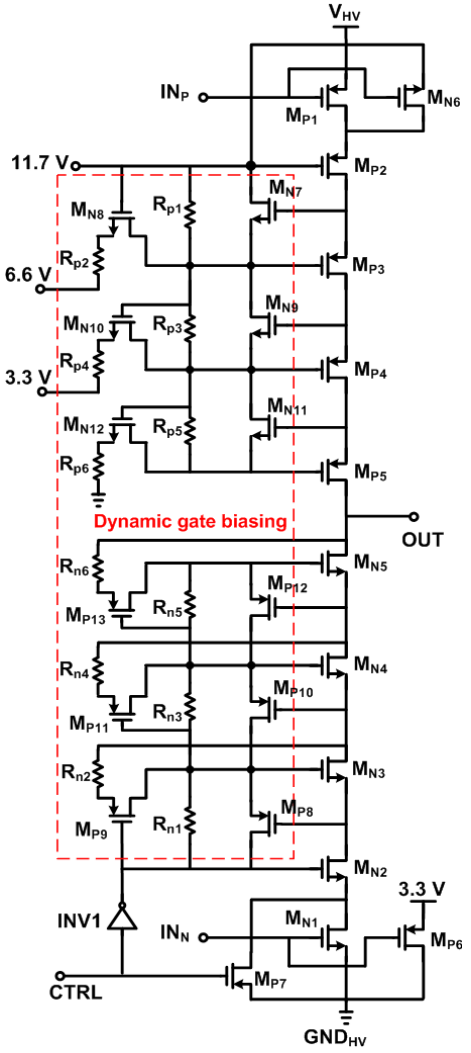

그림 4. CMOS 트랜지스터를 이용한 제안 된 고전압 펄서의 출력 드라이버

Fig. 4. Proposed output driver of HV pulser using CMOS transistors.

half of the output driver (NMOS parts) during the receive mode. The power down of the upper half of the output driver (PMOS parts) is done by powering down the preceding second level-shifter. The second level-shifter also follows the similar approach of the output driver, where DMOS transistors have been replaced with 3.3-V CMOS transistors using stacking and dynamic bias circuitry[6].

2. Low-Noise Preamplifier and HV switch

Fig. 5 shows the schematic of the proposed low-noise preamplifier. There are several candidates, such as continuous or discrete-time capacitive feedback, common-gate or regulated cascode topology, and resistive-feedback transimpedance amplifier (TIA)[7~8], which can be utilized as the preamplifier in the CMUT interface. Among these, the TIA topology is chosen for its ease of DC biasing and its low input-impedance, which is suitable for current signal sensing with a high-impedance source such as the CMUT. The TIA consists of a common-source amplifier followed by a source follower and a feedback resistance path using pseudo-resistors for higher integration. Source-to-source-connected NMOS transistors biased in the triode region is utilized to achieve symmetric resistance which is known to be robust with small variation of voltage change across the pseudo-resistor. In order to maximize the input signal current, the input impedance R_{IN} of the closed-loop preamplifier is minimized, with $R_{IN} = R_F/(1+A)$, where R_F and A represent the feedback resistance and open-loop gain of the TIA, respectively.

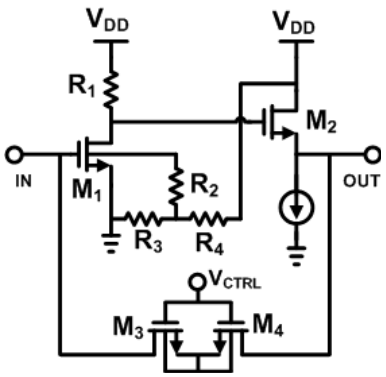

그림 5. 제안 된 TIA의 회로도 (바이어스 회로 생략)
Fig. 5. Simplified circuit schematic of proposed TIA (biasing and power down circuits omitted).

The input referred noise current can be expressed as [7];

$$\overline{i_{N_{total}}^2} = \overline{i_{N_{amp}}^2} + \overline{v_{N_{amp}}^2}\left(\frac{1}{R_{IN_{amp}}} + \omega C_{IN} + \frac{1}{R_F}\right) + \overline{i_{R_F}^2} \quad (1)$$

where $\overline{i_{N_{amp}}^2}$ and $\overline{v_{N_{amp}}^2}$ are the input referred current and voltage noise of the open-loop amplifier, respectively, $\overline{i_{R_F}^2}$ is the noise of feedback resistance, $R_{IN_{amp}}$ is the input resistance of the open-loop amplifier, C_{IN} is the total input capacitance including the CMUT and parasitic capacitance. From [7], it can be seen that the transconductance of the input transistor M1 is dominant in deciding the input referred noise of the core amplifier and thus must be maximized while considering the bias and power consumption. In addition, the value the feedback resistance is critical in deciding the transimpedance gain, noise, and bandwidth of the TIA. For this application, the value is set to be 65 kΩ to achieve around 94 dBΩ of transimpedance gain within in the bandwidth of interest at 2.6 MHz, providing 400 mV of maximum output voltage swing at maximum current input signal condition.

A self forward-body-biased (FBB) technique [9] is applied to the common-source transistor to reduce the threshold voltage of the transistor so that the supply voltage of the preamplifier can be lowered to around 1.1 V without affecting its performance. The designed overall preamplifer consumes a total of 347 μA of current at 1.1 V supply, at typical condition, which includes the constant-gm bias circuit.

Previous HV switch [2] is also designed using HV DMOS transistor in order to prevent the HV signal from being applied to the preamplifier input during the transmit mode. In the proposed work, similar to

the HV pulser, the DMOS transistor is replaced using five stacked NMOS transistors with dynamic bias circuitry to distribute up to 15 V between the terminals for protection. The sizing of the switches are carefully done considering the switch-on resistance, so that the gain loss and noise degradation is negligible during the receive mode.

Ⅳ. Simulation Results

The AFE IC is designed using 0.18-μm CMOS process. The chip layout is shown in Fig. 6, where the total area of the core is less than 0.15 mm^2. The metal width of the HV supply and ground lines are made sufficiently wide in order to support large amount of dynamic current in the output driver. The path to/from the transducer interface pads are made short as possible to minimize the added resistive and capacitive parasitics.

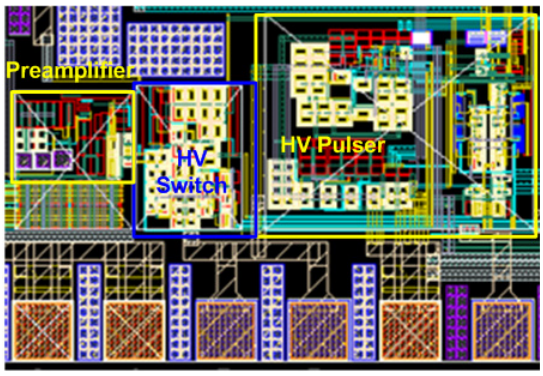

그림 6. AFE IC의 레이아웃
Fig. 6. Layout of designed AFE IC.

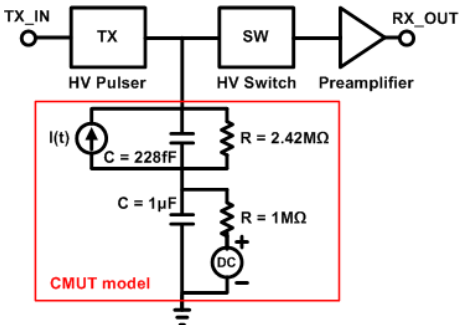

그림 7. 시뮬레이션에서 사용 된 CMUT의 전기적인 등가모델
Fig. 7. Equivalent electrical model of CMUT used in simulation.

For the simulation of the AFE IC, an equivalent electrical CMUT model is used as shown in Fig. 7. To check the operation of the HV pulser, Fig. 8 shows the transient simulation plot in which 1.8-Vp-p input signal with 192-ns pulse width is applied to the pulser input and the 15-Vp-p signal results at the output of the driver with a delay of 20.6 ns. Additional parallel parasitic load capacitance of 10 pF is added to the equivalent CMUT model for the transmit path simulation.

For the receiver, Fig. 9 shows the closed-loop gain response plot of the preamplifier at different process, voltage, and temperature (PVT) corner conditions. A transimpedance gain of 94 dB is achieved at all corners in the bandwidth of interest and the 3-dB

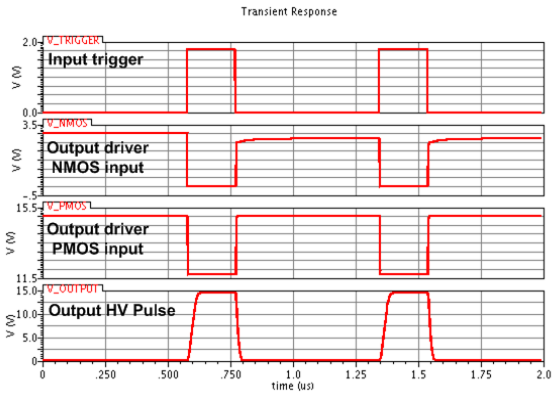

그림 8. 고전압 펄서의 transient 특성 그래프
Fig. 8. Transient simulation plot of the HV pulser.

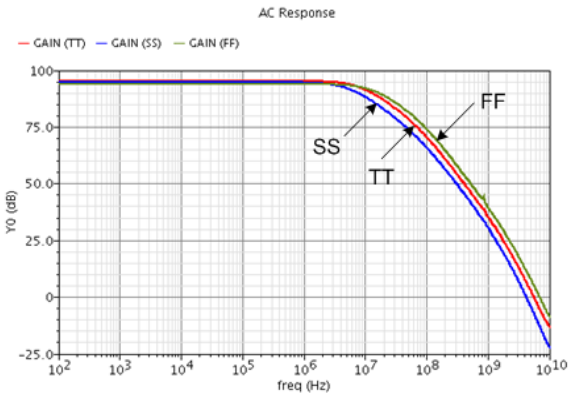

그림 9. 여러 corner조건에서의 preamplifier 이득특성
Fig. 9. Gain response of preamplifier at different corners.

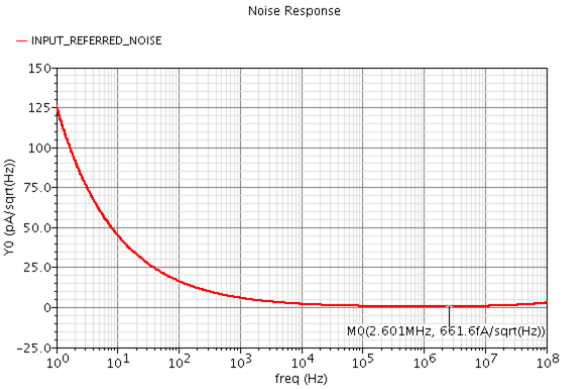

그림 10. Preamplifier의 노이즈 특성
Fig. 10. Input current noise response of preamplifier.

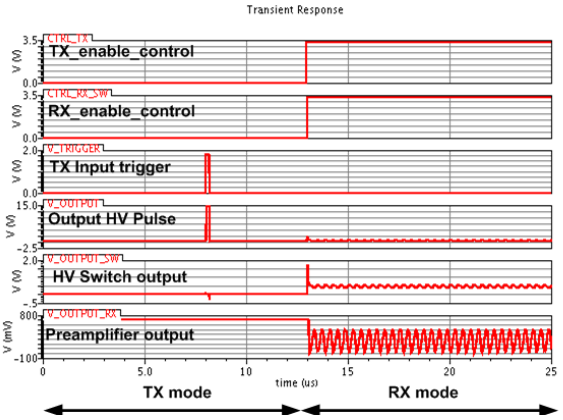

그림 11. AFE IC의 transient 특성 그래프
Fig. 11. Transient simulation plot of the AFE IC.

표 1. 제안 된 초음파 AFE IC의 성능 요약표 및 기존 회로들과의 비교
Table 1. Performance summary of proposed AFE IC and comparison with previous works.

Parameter	[2]	This work
Blocks	HV pulser/Preamp/HV switch	HV pulser/Preamp/HV switch
HV pulser output voltage	30 V	15 V
HV pulser trigger width	150-170 ns	192 ns
Preamp gain	96.6 dBΩ	94 dBΩ
Preamp input referred noise	0.56 mPa/√Hz @ 3 MHz	662 fA/√Hz @ 2.6 MHz
Preamp bandwidth	5.2 MHz	8.3 MHz
Preamp power consumption	14.3 mW	382 μW
Area (1-channel AFE)	0.33 mm²	0.15 mm²
Technology	0.18μm HVCMOS	0.18μm CMOS

bandwidth of 8.3 MHz is achieved at typical operation condition with a capacitive load of 5 pF at the preamplifier output. The input current noise density of 662 fA/√Hz at 2.6 MHz is achieved as shown in Fig. 10.

Figure 11 shows the overall transient plot of the AFE IC, first starting from transmit mode and then switching to receive mode. The transient simulations confirm correct operation of the AFE IC, operating as both the transmit and receive interface for the transducer. Table I presents the summarized performance of the designed AFE IC and compares it with recently published AFE IC for ultrasound medical imaging applications. Our designed IC shows favorable performance in the overall area while using standard CMOS process.

V. Conclusions

A highly-integrated high-voltage AFE IC for ultrasound medical imaging applications is designed using 0.18-μm standard CMOS technology. The proposed single-channel AFE IC, designed to interface with capacitive transducer at 2.6 MHz, consumes less than 0.15 mm^2 in core area and can be a viable solution for various large-array medical ultrasound imaging systems.

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