Image Independent Driving Power Reduction for High Frame Rate LCD Televisions

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In this letter, the constant driving power reduction ratio has been achieved for column drivers regardless of the input image by incorporating a new static power reduction scheme into the previous dynamic power reduction method. The measured power reduction ratio is around 50% for a 120 Hz liquid crystal display panel in such cases of still input video and fallback.

Keywords: Low power, constant power reduction ratio, image independent, high frame rate, 120 Hz, LCD.

I. Introduction

It is essential to reduce the power consumption in mobile applications to prolong battery operation time. Intel has proposed several techniques to lower the display power consumption, such as adaptive backlight control, dynamic refresh rate scaling, and interlaced driving [1], because a liquid crystal display (LCD) uses about 30% of the total power in a notebook PC. These days, it is necessary to employ a power reduction scheme in compliance with global power consumption regulations to cut down on greenhouse gases [2], even in the area of LCD televisions (TVs), which have become mainstream consumer products.

An LCD consists of a panel and a backlight that control the transmittance and the maximum luminance, respectively. Typically, a backlight consumes up to more than 80% of the overall power in TV products. As a result, various active dimming schemes have been introduced to decrease the backlight power consumption [3]-[5]. To date, it has been reported that active dimming algorithms can achieve 30% to 60% power reduction, on average.

Unlike backlights, panels have adopted power increasing techniques, such as higher resolutions of ultra definition (3840×2160) and 4K2K (4096×2160) and higher frame rates of 120 Hz and 240 Hz, for higher picture quality. Because relatively less power has been used in panels compared to that in backlights, this increased panel driving power has been neglected. However, considering the fact that an active dimming technique allows substantial backlight power to lessen, the increased power consumption of a panel is no longer an insignificant element.

In early 2010, we proposed a dynamic driving power reduction scheme for 120 Hz high frame rate LCD panels by means of reducing the frame rate in the cases of fallback and still input video [6]. A fallback is the simple frame repetition method adopted by most motion interpolation schemes to cover the visible artifacts where there are irregular, erratic motion changes or abrupt image changes with very little correspondence. The previous low power method replaces the interpolated frame with vertical blank time, which has no voltage transitions at the column lines, resulting in reduced dynamic power consumption of the column drivers. However, since the previous scheme addresses only the dynamic power consumption for the total power, which consists of the static and dynamic components, the resultant power reduction ratios of a column driver show different values according to the input images. In this letter, a static power reduction scheme that is integrated into the previous dynamic power reduction scheme is introduced so that the total power reduction ratio remains invariable, irrespective of image content. Consequently, minimum power consumption is achieved.

II. Low Power 120 Hz LCD Driving Scheme

Since the loads of column lines in LCD panels can be simply modeled as capacitors, the power consumption at the outputs of column drivers can be described as

$$P_{\text{TOTAL}} \approx a C_{\text{LOAD}} V_{\text{SWING}}^2 f_{\text{LINE}} + b I_{\text{BIAS}} V_{\text{AVDD}} N_{\text{AMP}}, \qquad (1)$$

where a and b are coefficients, f_{LINE} is a line frequency, V_{SWING} is the voltage swing level of a column driver's output, C_{LOAD} is the total load capacitance, I_{BIAS} is the bias current of an output amplifier in a column driver, V_{AVDD} is the supply voltage of amplifiers, and N_{AMP} is the total number of amplifiers to drive an LCD panel, as shown in Fig. 1.

The first term on the right side in (1), $a C_{\text{LOAD}} V_{\text{SWING}}^2 f_{\text{LINE}}$, is the dynamic power consumed at the transitions of output voltages of column drivers, and the second term, $b I_{\text{BIAS}} V_{\text{AVDD}} N_{\text{AMP}}$, is the static power consumption mainly caused by biasing output amplifiers in column drivers. Now that the line frequency is proportional to the frame frequency, the higher frame rate also increases the dynamic power consumption by the increased line frequency f_{LINE}. On the other hand, the static power consumption is multiplied by the number of column lines, which is generally equal to the number of amplifiers, N_{AMP}.

To keep the LCD panels from wasting dynamic power, the previous low dynamic power technology was proposed to drive the 120 Hz LCD panel at the input frame rate, 60 Hz, under the specific circumstances of fallback and still input video [6]. While the conventional method displays all the high-speed frames produced by repeating 60 Hz input images, the proposed frame rate reduction scheme illustrates only the first frame of repeated frames and the remaining frame is changed into the vertical blank period without scanning gate lines as shown in Fig. 2. Therefore, the image driven at the first frame is held during one following frame for 120 Hz LCD panels.
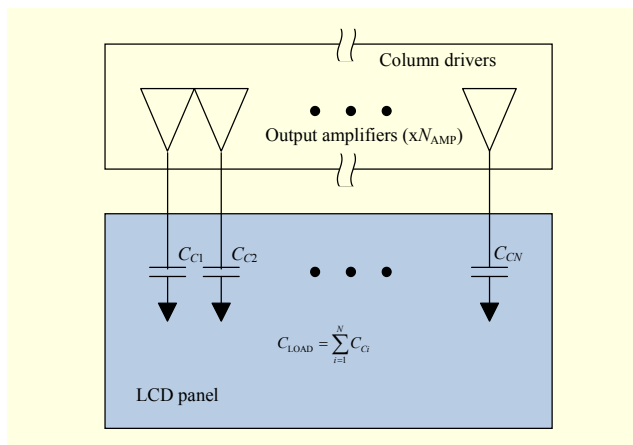
Even though the line time is the same as that of the conventional scheme, the total number of transitions and the average line frequency turn out to be reduced up to half. Consequently, the dynamic power consumption can be reduced by 50% at a 120 Hz frame rate.

However, given that the dynamic power has the direct proportion to the number and amplitude of the transitions in the frame and the static power remains constant, the portion of the dynamic power in the total power is changeable in accordance with the input image, leading to the power saving ratio varying with the input images.

To make the effective power reduction algorithm that is independent of the input image, the time-based bias current control scheme is enabled to lower the average bias current. The proposed scheme maintains the bias current level during the active period, in which output amplifiers are driving the pixels of a panel, and shuts the bias current off during the vertical blank period extended by the dynamic power reduction. Thus, the average static power (SP) can be reduced to half for a 120 Hz application as in (2). The total power, which is the sum of the dynamic and static powers, is lowered to about half.

$$SP_{\text{proposed,120Hz}} = b \left(I_{\text{BIAS}} \right)_{\text{avg@120Hz}} V_{\text{AVDD}} N_{\text{AMP}}$$

$$= b \frac{I_{\text{BIAS}}}{2} V_{\text{AVDD}} N_{\text{AMP}} = \frac{1}{2} SP_{\text{conventional,120Hz}} \qquad (2)$$

The static power reduction method provides the output waveforms of Fig. 3 with the dynamic power reduction method for a 120 Hz display. During the extended vertical blank period, the output voltage levels are held at the common-mode voltage (VCOM) and both the static and dynamic current consumptions become zero. Unless the voltage level is

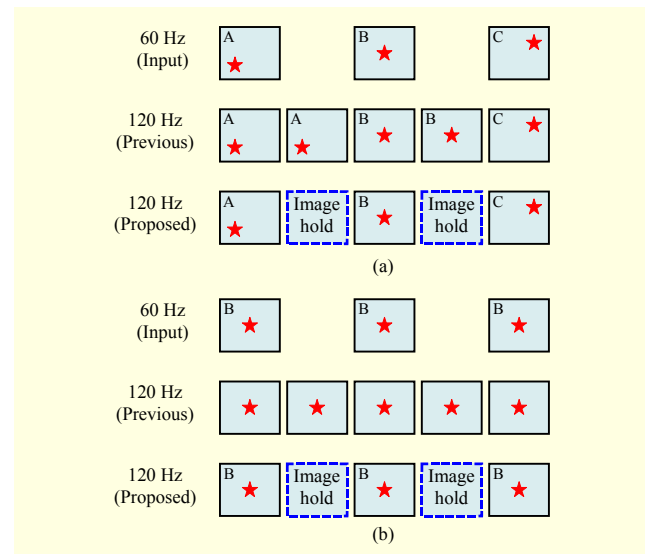Fig. 1. Simple circuit model of LCD panel.

Fig. 2. Conventional and proposed 120 Hz technologies for (a) fallback and (b) still input video [6].
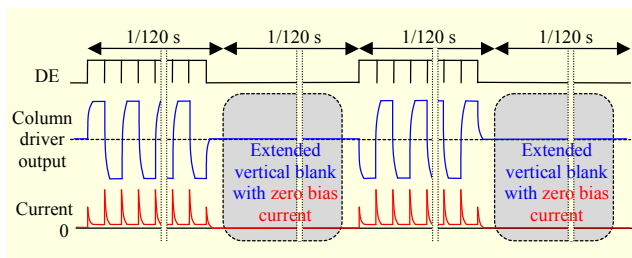
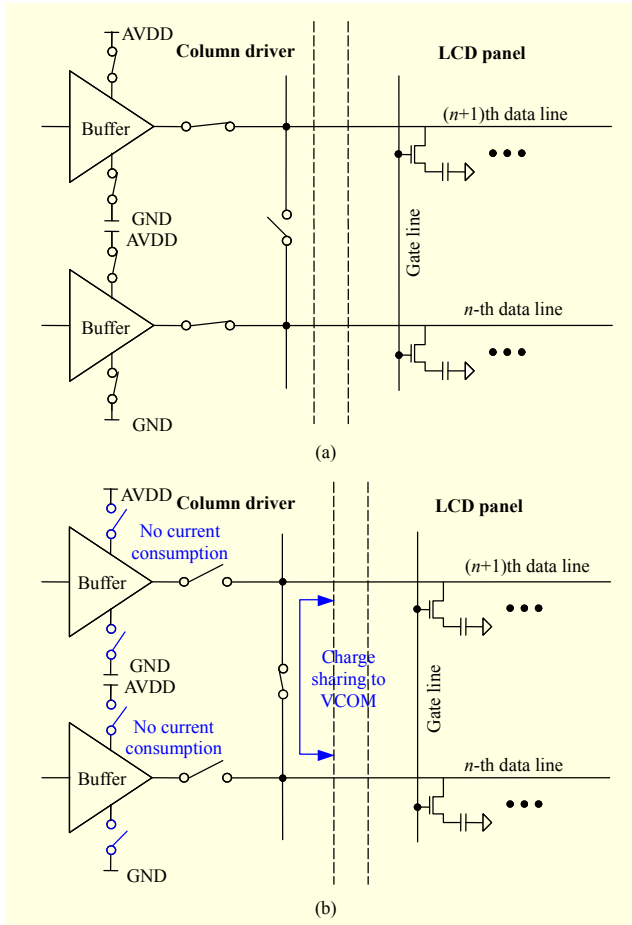Fig. 3. Signal waveforms of proposed low power scheme.

(a)

(b)

Fig. 4. Bias current control scheme during (a) active period and (b) extended vertical blank period.

(b)

Fig. 5. Bias current control circuit: (a) circuit configuration and (b) waveform.

maintained at VCOM, the inversion pattern artifact is observed in the solid gray pattern that has the only one gray level over all pixels.

To keep the output voltage at VCOM during the extended vertical blank period, the charge sharing scheme used in the column driver has been exploited. In addition, we implement the supply switch operation into a column driver, which controls the current paths to AVDD and GND, that is, the bias current; this concept is illustrated in Fig. 4.

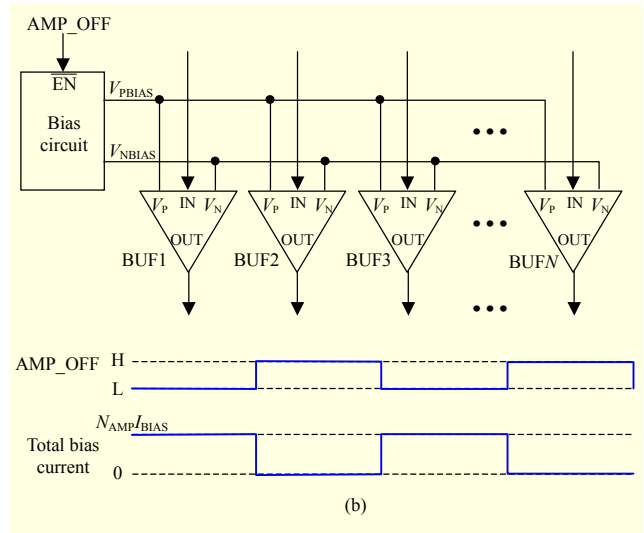During the active period, the supply switches connected to

amplifiers are turned on to provide the bias current to the amplifiers as depicted in Fig. 4(a). As shown in Fig. 4(b), during the vertical blank period, the proposed static power reduction scheme turns off the bias currents of output amplifiers while the voltages of column lines are held at VCOM by the charge sharing. Because all output amplifiers are controlled by one bias circuit, it is easily established to turn off amplifiers by modifying only the bias circuit as illustrated in Fig. 5.

III. Experiment Results

We applied our power reduction method to a 46-inch full-HD (full high definition: 1920×1080) 120 Hz super-patterned vertical alignment (S-PVA) LCD panel. As depicted in Fig. 6, the algorithm has been implemented in a field programmable gate array (FPGA) timing controller (TCON) that programs a start-vertical (STV) signal for gate drivers and timing pulse (TP) and AMP_OFF signals for column drivers to generate the extended vertical blank and shut down the source drivers. We utilize the maximum power pattern for 1G2D [7] of 120 Hz, which is the horizontal line pattern, to measure the output waveform of Fig. 7 in the first and the second columns of a 120 Hz LCD panel. In the first frame, the square waveform is observed, and then the DC voltage at the VCOM level is held by charge sharing in one following frame that is converted into the extended vertical blank period.

The measured power consumption of the analog supply voltages of source drivers, which are set to 15 V, for the conventional, dynamic power reduction, and proposed schemes are compared with one another in Table 1 by applying four test patterns used in the previous power reduction scheme
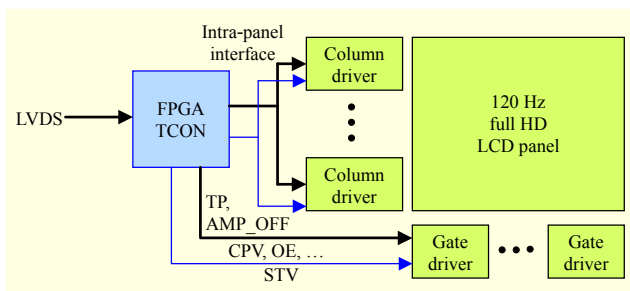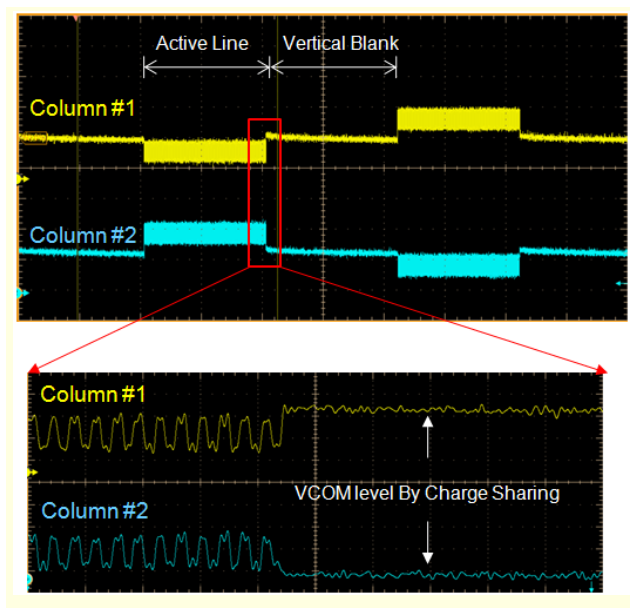
Fig. 6. Proto-type low power 120 Hz LCD panel.

Fig. 7. Measured waveforms of column data signals in low power 120 Hz LCD panel.

Table 1. Measured power consumption and reduction ratios.

Pattern		White	V-shade	G-130	H-line
Conv.	Power (W)	3	4.86	6.39	13.89
Prev. [6]	Power (W)	2.97	4.365	5.13	8.90
	Ratio (%)	1.0	10.2	19.7	34.0
This work	Power (W)	1.61	2.60	3.51	7.40
	Ratio (%)	46.5	46.6	45.7	46.8

[6]. Unlike the dynamic power reduction scheme that shows the different power reduction ratios for the input images, the proposed scheme establishes the constant reduction ratio.

IV. Conclusion

Higher refresh rate LCD panels feature lower motion blur on the screen but at the expense of the increased panel driving power consumption. Hence, the low power LCD driving technique without degradation in motion blur performance is suggested in this letter. The proposed static power reduction method is incorporated into the previous dynamic power reduction scheme. While the dynamic power reduction method extends the vertical blank time, the static power reduction scheme makes use of a charge sharing scheme and an additional bias control circuit to reduce the bias current consumption of the column drivers during the extended vertical blank time. Subsequently, total power reduction by about 50% is reached for a 120 Hz LCD panel. Furthermore, when this scheme is deployed in a 240 Hz LCD panel, around 75% power reduction can be accomplished.

References

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