Simulation and Fabrication Studies of Semi-superjunction Trench Power MOSFETs by RSO Process with Silicon Nitride Layer

Kyoung Il Na, Sang Gi Kim, Jin Gun Koo, Jong Dae Kim, Yil Suk Yang, and Jin Ho Lee

In this letter, we propose a new RESURF stepped oxide (RSO) process to make a semi-superjunction (semi-SJ) trench double-diffused MOSFET (TDMOS). In this new process, the thick single insulation layer (SiO_2) of a conventional device is replaced by a multilayered insulator (SiO_2/SiN_x/TEOS) to improve the process and electrical properties. To compare the electrical properties of the conventional RSO TDMOS to those of the proposed TDMOS, that is, the nitride_RSO TDMOS, simulation studies are performed using a TCAD simulator. The nitride_RSO TDMOS has superior properties compared to those of the RSO TDMOS, in terms of drain current and on-resistance, owing to a high nitride permittivity. Moreover, variations in the electrical properties of the nitride_RSO TDMOS are investigated using various devices, pitch sizes, and thicknesses of the insulator. Along with an increase of the device pitch size and the thickness of the insulator, the breakdown voltage slowly improves due to a vertical field plate effect; however, the drain current and on-resistance degenerate, owing to a shrinking of the drift width. The nitride_RSO TDMOS is successfully fabricated, and the blocking voltage and specific on-resistance are 108 V and 1.1 mΩcm^2, respectively.

Keywords: Superjunction (SJ), semi-SJ, TDMOS, power MOSFET.

I. Introduction

To overcome the "silicon limit" of a discrete power device, trench double-diffused MOSFETs (TDMOSs) with the RESURF [1]-[4] and superjunction (SJ) [5]-[10] concepts are preferred over a vertical double diffused MOSFET (VDMOSFET). These devices have such inherent characteristics as a low specific on-resistance ($R_{ON,SPEC}$), a high switch speed, and a high current derivability. However, power MOSFETs with the SJ concept are complicated by the fact that they must achieve ideal alternatively-stacked p and n layers using multi-epitaxy and multi-implantation [7], and deep etching/epitaxial growth [8], [9] technologies are generally restricted to the charge balance between the p and n layers [10]. Additionally, a power MOSFET with the SJ concept is superior to a RESURF-type device in a high-voltage application (BV_{DS} > 200 V). However, RESURF-type devices are promising for a medium voltage application (BV_{DS} < 200 V) as they can be easily made compared to SJ-type devices and have relatively high electrical properties compared to conventional power MOSFETs. These RESURF-type devices have been realized using RESURF stepped oxide (RSO) [1]-[3] or vertical local oxidation of silicon (LOCOS) processes [4]. In the case of a conventional RSO process, however, it is difficult to achieve separation and control the thickness between the gate oxide and insulator layers, owing to the use of the same material. Moreover, the LOCOS process has electrons traveling at the boundary between the channel edge and the bird beak region.

In this letter, we propose a new RSO process to more easily control the thickness of the insulation layer; in this process, the material of the single layer is altered from SiO_2 to create a SiO_2/SiN_x/TEOS multilayered insulator. Moreover, simulation studies are performed to determine the electrical characteristics of a conventional RSO TDMOS and those of the proposed

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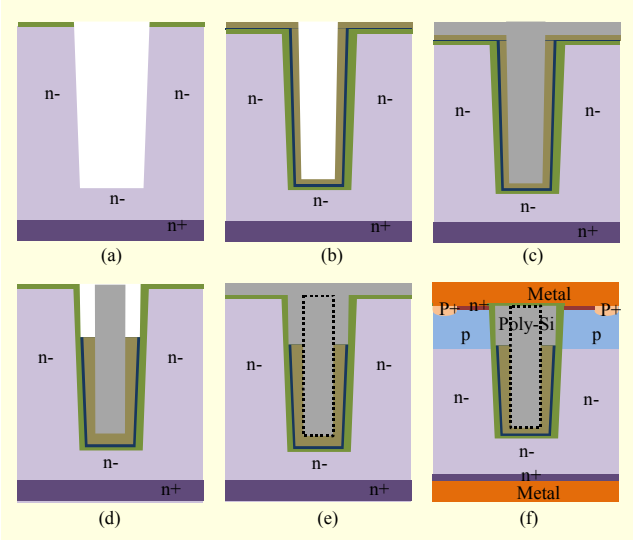

Fig. 1. Schematics of nitride_RSO TDMOS process flow with nitride layer: (a) trench etch, (b) $SiO_2/SiN_x/TEOS$ deposition, (c) polysilicon trench filling, (d) polysilicon, nitride and TEOS etch-back, (e) second polysilicon deposition, and (f) implantation and metalization.

nitride_RSO TDMOS, which is fabricated through nitride_RSO, a modified process. In addition, the electrical properties, such as the maximum drain current ($I_{D,MAX}$) and blocking voltage (BV_{DS}), of the fabricated nitride_RSO TDMOSs are measured using a Tektronix curve tracer and high-power measurement systems.

II. New RSO Process

To easily form a thick insulation layer for a vertical field plate effect, the conventional RSO process is modified to transform a SiO_2 layer into a $SiO_2/SiN_x/TEOS$ layer (multilayered insulator). The insertion of nitride film during the RSO process has several advantages. The first is a good etching selectivity between the SiO_2 and SiN_x layers, which means that the SiN_x layer acts as an etching stop layer during oxide etching. The second is that the SiN_x layer can improve the electrical performance using stress control (either tensile or compressive stress) and high permittivity compared to a thermal-oxide layer. These effects of SiN_x layers are well known and have already been used by industrial device makers to improve n- and p-type carrier mobility in low-power CMOS technology [11]. As shown in Fig. 1, the process flow of a semi-SJ TDMOS with nitride_RSO can be described as follows. First, the deep trench is etched. Next, the $SiO_2/SiN_x/TEOS$ layer is deposited. The trench is then filled with the first doped polysilicon. Next, the polysilicon is etched back and the TEOS layer is removed to the end level of the channel. The second doped polysilicon is then deposited.

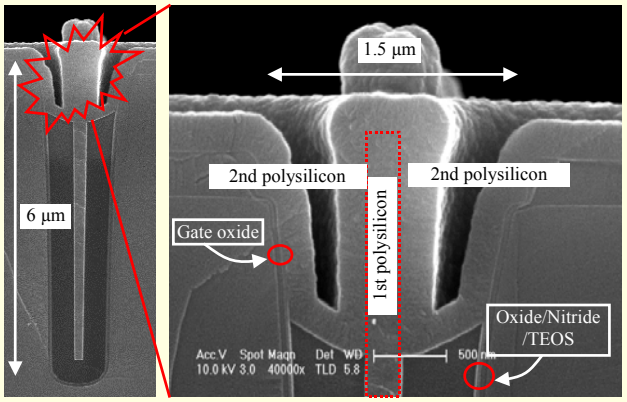

Fig. 2. Cross-section images of fabricated device with 6-µm Si etched full device image and gate/nitride_RSO interface region.

Finally, a fabrication process, such as channel implantation, drive-in, source and p+ region definitions, wafer thinning, and metallization, is performed. Figure 2 shows a cross-section image of the fabricated device with a sharp dividing line between the gate oxide and thick trench oxide. For medium voltage operation, this device is designed with a 4-µm cell pitch, 1.5-µm gate width, 6-µm trench depth, 50-nm gate oxide, and 500-nm-thick insulator layer.

III. Device Simulation

To compare the electrical characteristics of the conventional RSO TDMOS with those of the nitride_RSO TDMOS, the BV_{DS}, threshold voltage (V_{TH}), and I_D (V_D) are investigated using a SILVACO TCAD simulator based on an 8-µm/0.8-Ωcm epitaxially grown substrate. Figure 3(a) shows the distribution of electric potential of the nitride_RSO device. In a conventional planar-type power MOSFET, the concentration of electric potential is generated at the p-base/n-drift junction. However, the potential drop of an RSO-type TDMOS is concentrated at the edge region of the deep trench and gradually alleviated in the vertical field plate region, as shown in Fig. 3(a). Figures 3(b) and 3(c) show that the BV_{DS} and V_{TH} of the conventional RSO device and the nitride_RSO device have the same properties, such as BV_{DS} = 120 V and V_{TH} = 3.5 V. However, Fig. 3(d) shows the comparable results of the typical I_D/V_D characteristics between the two devices. The nitride_RSO device features a slightly higher drain current and relatively lower on-resistance compared to a conventional RSO device. This is because the electrons accumulate along the thick trench oxide layer during the on-resistance of a gate. The amount of total accumulated charge basically depends on the total thickness and permittivity of the dielectric material in the MOS capacitor structure. Accordingly, in the nitride_RSO

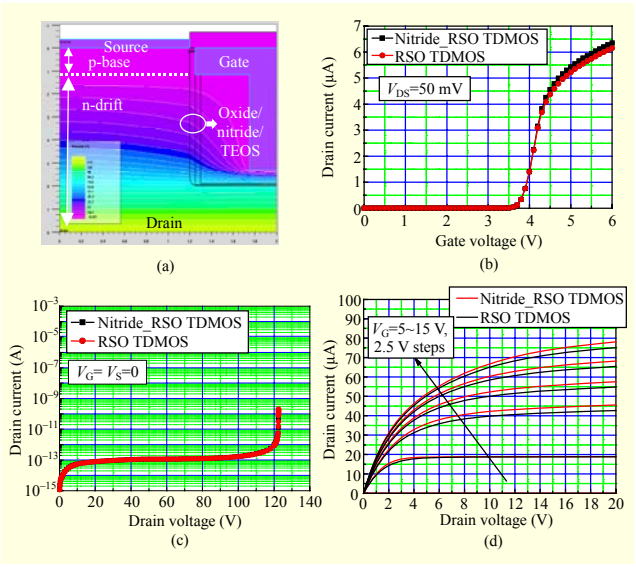

Fig. 3. (a) Potential distribution of nitride_RSO structure, electrical comparison between RSO TDMOS and nitride_RSO TDMOS, such as (b) I_D vs. V_G with V_{GS} = 50 mV, (c) I_D vs. V_D with V_{GS} grounded (BV_{DS} property), and (d) I_D and V_D with various V_G.

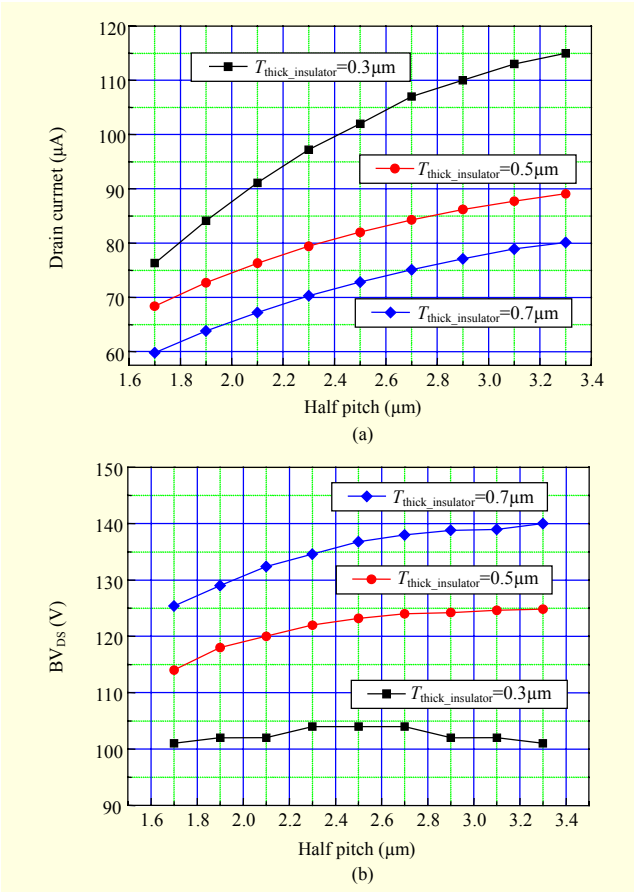

Fig. 4. (a) Drain current and (b) BV_{DS} properties of nitride_RSO TDMOS as function of cell half-pitch size and thickness of thick insulator layer.

TDMOS, the higher permittivity of the inserted nitride layer can increase the accumulated charge, which means an increase of drain current. At V_G = 20 V and V_D = 15 V, the drain current levels of the nitride_RSO TDMOS and the RSO TDMOS are 7.8 × 10^{-5} and 7.5 × 10^{-5} A per unit cell pitch, respectively. These results indicate that the difference in resistance between the two devices overall is around 3%.

As shown in Figs. 4(a) and 4(b), the typical I_D (V_D) and BV_{DS} characteristics strongly depend on the thickness of the insulation layer and the cell pitch size. When the cell pitch size is gradually scaled up from 1.7 μm to 3.3 μm, not only the drain current but also the BV_{DS} of 0.5-μm-thick and 0.7-μm-thick RSO devices slowly increase and become saturated. In the case of the BV_{DS} aspect, as the cell pitch becomes too small, the potential lines are pushed too much toward the substrate, resulting in a high electrical field focused at the trench bottom. The evidence of this effect is shown in Fig. 5, in which the distribution of the simulated electrical field at the drift region with 1.7-μm and 3.3-μm half-pitch devices under a blocking voltage condition is plotted. The blocking voltages of the twodevices are 114 V and 125 V, respectively. This result means that the device with a small cell pitch has a higher electrical field than the device with a large cell pitch at the end region of the RSO structure. With an increase in the thickness of the insulator, a higher blocking voltage can be sustained due to the vertical field plate effect. A drain current degradation as a function of the cell pitch is due to the decrease in the current path of the drift region. This effect is significant in a device with a thin insulator. Moreover, in this case, when the cell pitch is too large, BV_{DS} also drops as the drift region cannot be fully depleted.

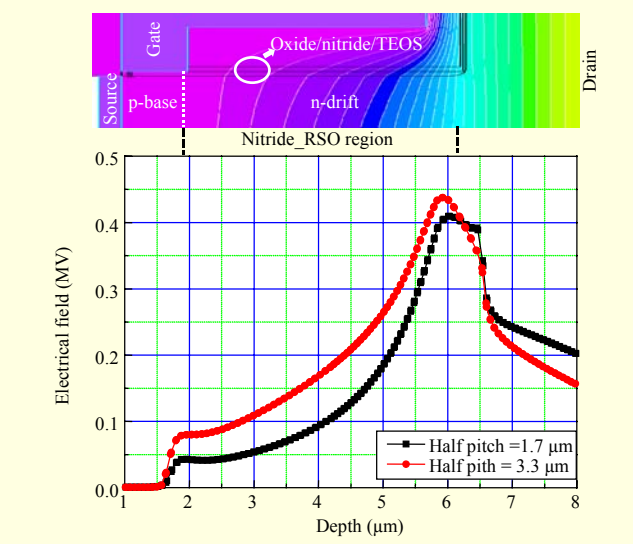

Fig. 5. Comparison of electrical field at drift region between 1.7-μm and 3.3-μm half-pitch devices at blocking voltage condition.

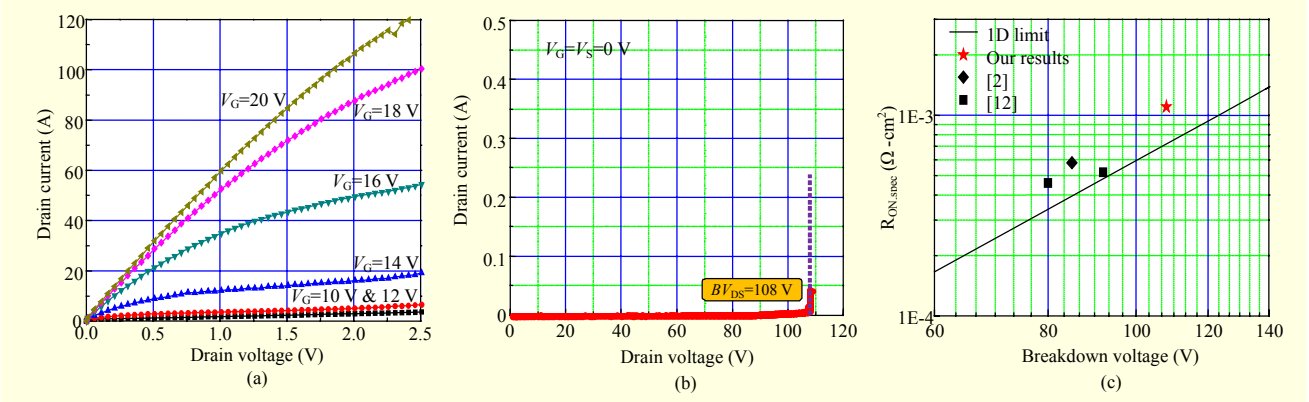

Fig. 6. (a) Drain current and (b) BV_{DS} properties of fabricated nitride_RSO TDMOS. (c) Benchmarking of result with respect to 1D silicon limit and best-in-class RSO-type TDMOSs in 100-V rated power application. Device designed with 2.5-μm half-pitch and 5,500-Å-thick insulator.

IV. Device Results

For a 100-V/100-A motor control application, power devices with a 2.5-μm half pitch and 5,500-Å-thick insulator are successfully fabricated using a new RSO process with an inserted nitride layer. Figures 6(a) and 6(b) show the drain current as a function of drain voltage with various gate voltages and BV_{DS} properties, respectively. When the gate voltage is 20 V, the aximum current and $R_{ON,SPEC}$ of this device reach 120 A and 1.1 mΩcm^2, respectively. Also, the BV_{DS} is about 108 V under V_{GS} = 0 V. In a 100-V rated power application, this result shows excellent performance and matches the best-in-class trend of the RSO-type TDMOSs. However, the difference of BV_{DS} between the simulated and fabricated devices is considered to be due to the edge termination. A nonoptimized edge termination structure of a power device can make a cylindrical and/or spherical junction at the bottom assisted layer through a depletion extension as a blocking voltage bias condition. Accordingly, cylindrical and/or spherical junctions decrease the blocking properties.

V. Conclusion

In this letter, we proposed nitride_RSO, which is a new fabrication process of an RSO power device with an inserted nitride layer in the thick insulator region. In addition, simulation using a TCAD simulator was performed to compare the electrical properties of a conventional RSO TDMOS to those of a nitride_RSO TDMOS with various cell pitch sizes and insulator thicknesses. Moreover, a nitride_RSO TDMOS device was successfully fabricated, and its BV_{DS} and $R_{ON,SPEC}$ were 108 V and 1.1 mΩcm^2, respectively.

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