Low Temperature Characteristics of Schottky Barrier Single Electron and Single Hole Transistors

Moongyu Jang, Myungsim Jun, and Taehyoung Zyung

Schottky barrier single electron transistors (SB-SETs) and Schottky barrier single hole transistors (SB-SHTs) are fabricated on a 20-nm thin silicon-on-insulator substrate incorporating e-beam lithography and a conventional CMOS process technique. Erbium- and platinum-silicide are used as the source and drain material for the SB-SET and SB-SHT, respectively. The manufactured SB-SET and SB-SHT show typical transistor behavior at room temperature with a high drive current of 550 μA/μm and –376 μA/μm, respectively. At 7 K, these devices show SET and SHT characteristics. For the SB-SHT case, the oscillation period is 0.22 V, and the estimated quantum dot size is 16.8 nm. The transconductance is 0.05 μS and 1.2 μS for the SB-SET and SB-SHT, respectively. In the SB-SET and SB-SHT, a high transconductance can be easily achieved as the silicided electrode eliminates a parasitic resistance. Moreover, the SB-SET and SB-SHT can be operated as a conventional field-effect transistor (FET) and SET/SHT depending on the bias conditions, which is very promising for SET/FET hybrid applications. This work is the first report on the successful operations of SET/SHT in Schottky barrier devices.

Keywords: Schottky barrier, single electron transistor, single hole transistor, tunneling.

I. Introduction

Transistors have been continuously decreasing in size with the progress of integrated circuit technology, and, now, more than a billion transistors are being integrated into a single chip. However, these integrated decananometer transistors are suffering from crucial problems, such as short channel effects and power dissipation, and the downscaling must eventually stop, owing to a physical size limitation. Thus, new functional devices, such as quantum devices, are being studied [1]-[4].

As charge-based transistors, Schottky barrier single electron transistors (SB-SETs) and Schottky barrier single hole transistors (SB-SHTs) are ultimate devices, in which the respective electrons and holes are transported one by one with very low power dissipation. In addition, the electrical characteristics of smaller-sized SB-SETs and SB-SHTs are expected to improve compared to conventional SETs and SHTs owing to a larger charging energy with the existence of an electrically induced Schottky tunnel barrier. Silicon SB-SETs and SB-SHTs have been studied for practical applications as they can utilize advanced silicon technologies and can be easily integrated with electronic circuits. Moreover, SB-SETs and SB-SHTs show conventional field-effect transistor (FET) behavior at room temperature. Thus, an SET-FET hybrid structure can be easily implemented.

In this letter, we offer the first report of the electrical characteristics of SB-SETs and SB-SHTs.

II. Experiment

The fabrication processes of SB-SETs and SB-SHTs are as follows. Phosphorous-doped n-type and boron-doped p-type silicon-on-insulator (SOI) wafers 20 nm thick are prepared for the SB-SETs and SB-SHTs, respectively. An ultrathin SOI wafer is used to enlarge the charging energy of the quantum dots. The doping concentration is 1×10^{15} cm^{-3} for both the n- and p-type wafers. Silicon nanowires 15 nm in width are defined using e-beam lithography. A thermally grown 4-nm-thick gate oxide insulator and a phosphorous-doped 50-nm-thick polysilicon layer are sequentially formed on the wafers. The polysilicon gate electrodes are patterned into a 20-nm

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width using e-beam lithography and dry etching techniques. Low-pressure tetraethyl orthosilicate oxide is deposited, followed by a dry etching process for the sidewall spacers. After the sidewall spacer etching, the remaining sidewall thickness was around 14 nm per side. Erbium and platinum were sputtered for the formation of the metallic source and drain for the SB-SETs and SB-SHTs, respectively. Erbium and platinum were chosen as the source and drain metal of the SB-SETs and SB-SHTs owing to their low Schottky barrier height for an electron and hole, respectively. Erbium-silicide ($ErSi_{1.7}$) and platinum-silicide (PtSi) were formed through rapid thermal annealing at 500ºC for five minutes. The nonreactive erbium and platinum were removed using a sulfuric peroxide mixture and aqua regia for 10 minutes, respectively. The detailed silicide processes were discovered in our previous papers [5], [6].

III. Results and Discussion

SB-SETs and SB-SHTs are composed of a tiny silicon island, metallic source and drain (S/D), gate oxide layer, and poly silicon gate, as shown Fig. 1(a). These are the same structures used in previously reported SB-MOSFETs [7], [8], except for a smaller width and length. Figure 1(b) shows a schematic energy band diagram of the SB-SET for a clearer understanding. The Schottky barriers are formed at the junctions between the S/D and island and work as tunneling barriers for the electron and hole in the SB-SET and SB-SHT, respectively. When the appropriate gate bias voltage is applied, the silicon island becomes conductive and can contain only one electron or hole in each discrete charge state [9].

Figures 2(a) and 2(b) show scanning electron microscope (SEM) images of the $ErSi_{1.7}$ S/D SB-SET and PtSi S/D SB-SHT, respectively. The insets show transmission electron microscope (TEM) images of the gate stack. Although the FET characteristics of these devices at room temperature have already been reported [10], for greater clarity, the FET characteristics are briefly summarized as follows. The manufactured SB-SET and SB-SHT with a 20-nm gate length showed a large on/off current ratio ($>10^6$) with a low leakage current of less than 10^{-5} μA/μm at room temperature, owing to the existence of the Schottky barrier between the source and channel region. The extracted threshold voltages were 0.90 V and –1.04 V for the SB-SET and SB-SHT, respectively, at room temperature. For the SB-SET and SB-SHT at room temperature, the saturation currents were 550 μA/μm and –376 μA/μm when the drain and gate voltages were 2/–2 V and 3/–3 V, respectively.

As the temperature is reduced, Coulomb oscillation behavior should appear if the device operates as an SB-SET or SB-SHT.

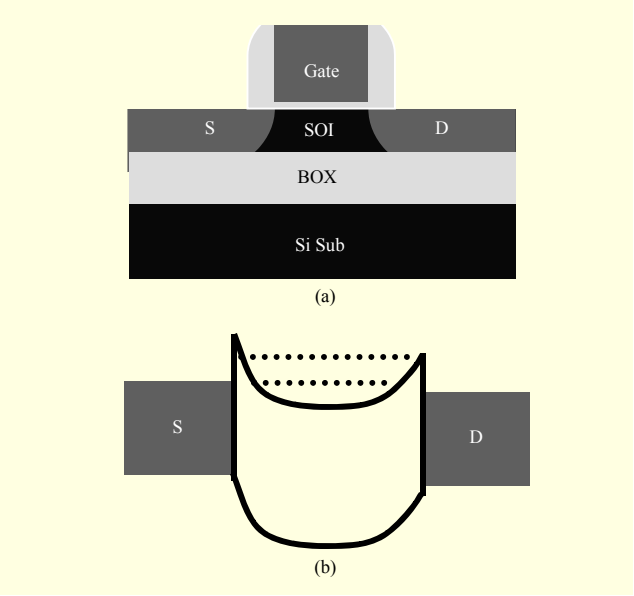

Fig. 1. (a) Schematic diagram of SB-SET/SB-SHT structures and (b) schematic energy band diagram of SB-SET (S and D denote source and drain, respectively).

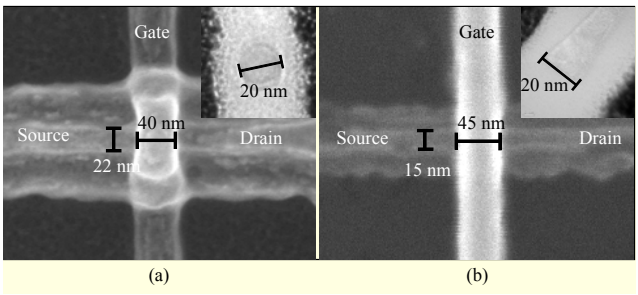

Fig. 2. SEM and TEM (inset) images of (a) erbium-silicided SB-SET and (b) platinum-silicided SB-SHT with 20-nm gate length.

Figures 3(a) and 3(b) show the drain current (I_D) to gate voltage (V_{GS}) characteristics of the SB-SET and SB-SHT measured at a temperature of 7 K as a function of the drain voltage (V_{DS}). The open and closed circles in Figs. 3(a) and 3(b) correspond to a V_{DS} of 1.5 V and 2.0 V for the SB-SET and –5 mV and –10 mV for the SB-SHT. As a typical characteristic of a single-charge transistor, periodic Coulomb oscillations are observed in both the SB-SET and SB-SHT. The measured Coulomb gaps are about 150 mV and 220 mV for the SB-SET and SB-SHT, respectively. From these results, the diameters of the islands are estimated to be 22 nm and 18 nm for the SB-SET and SB-SHT, respectively. These electrically determined island sizes are very close to those obtained from the TEM images in Fig 2. The applied V_{DS} values are very high in the SB-SET compared to those in the SB-SHT, and the Coulomb oscillation behavior is slightly degraded in the SB-SET. The extracted transconductance values are 0.05 μS and 1.2 μS for the SB-

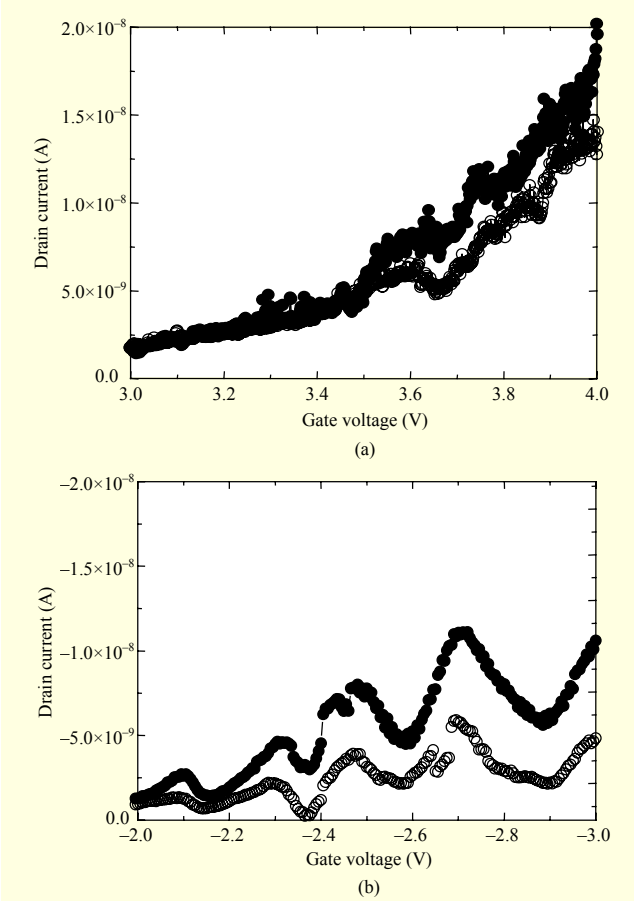

Fig. 3. Drain current (I_{DS}) vs. gate voltage (V_{GS}) characteristics of (a) erbium-silicided SB-SET and (b) platinum-silicided SB-SHT.

SET and SB-SHT, respectively. The reasons for these values are as follows. $ErSi_{1.7}$/silicon junctions have a greater inhomogeneous Schottky barrier height and many more interface trap states than PtSi/silicon junctions owing to the existence of an amorphous layer, resulting in the broadening of the conductance peaks.

From the TEM images, an amorphous silicon layer exists at the interface between the $ErSi_{1.7}$ S/D and the silicon island. On the other hand, a smooth interface is observed in the SB-SHT. The reasons for this are as follows. Platinum is the main diffuser during the formation of PtSi, whereas silicon is the main diffuser in $ErSi_{1.7}$ formation. Thus, the crystal structures of silicon at the interface between the silicon and $ErSi_{1.7}$ are heavily damaged, as shown in the TEM images in Fig. 4. Another noticeable point is that the formed island is smaller in the SB-SHT than in the SB-SET because the PtSi source and drain are formed under the sidewall spacers, and there is no underlap between the S/D and gate in the SB-SHT. Therefore, we can expect better electrical characteristics in the SB-SHT, and thus the more clearly observed Coulomb oscillations in the

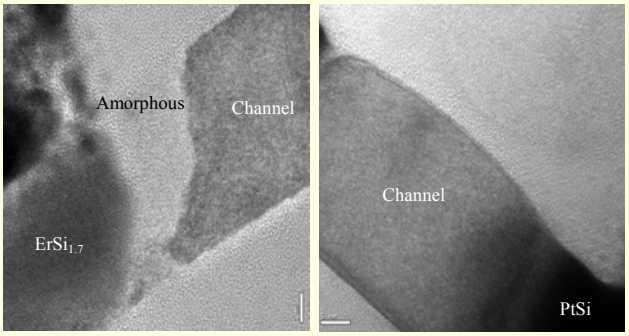

Fig. 4. TEM images of silicide/silicon interface for (a) erbium-silicided SB-SET and (b) platinum-silicided SB-SHT.

SB-SHT than in the SB-SET, shown in Fig. 3, that seem to be attributable to the smooth interface at the PtSi/silicon junction.

To analyze the interface characteristics in greater detail, the current-voltage characteristics of the $ErSi_{1.7}$ and PtSi Schottky diodes are investigated. The extracted ideality factors are 1.23 and 1.02 for the $ErSi_{1.7}$ and PtSi diodes, respectively. This result supports the idea that the interface between $ErSi_{1.7}$ and silicon has many interface trap states [11]. For the enhanced electrical characteristics, the interface trap states should be minimized at the $ErSi_{1.7}$/silicon interface.

IV. Conclusion

In summary, an SB-SET and an SB-SHT were fabricated using silicon technologies. Erbium silicide and platinum silicide were used as the S/D material of the SB-SETs and SB-SHTs, respectively. The Schottky barriers were naturally formed at the junction between the silicide S/D and the silicon island and worked as tunneling barriers. Coulomb oscillations of the SB-SETs and the SB-SHTs were clearly observed at a temperature of 7 K. The sizes of the islands were estimated to be 22 nm and 18 nm from the observed Coulomb gaps for the SB-SET and SB-SHT, respectively.

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