16-QAM-Based Highly Spectral-Efficient E-band Communication System with Bit Rate up to 10 Gbps

Min-Soo Kang, Bong-Su Kim, Kwang Seon Kim, Woo-Jin Byun, and Hyung Chul Park

This paper presents a novel 16-quadrature-amplitude-modulation (QAM) E-band communication system. The system can deliver 10 Gbps through eight channels with a bandwidth of 5 GHz (71-76 GHz/81-86 GHz). Each channel occupies 390 MHz and delivers 1.25 Gbps using a 16-QAM. Thus, this system can achieve a bandwidth efficiency of 3.2 bit/s/Hz. To implement the system, a driver amplifier and an RF up-/down-conversion mixer are implemented using a 0.1 μm gallium arsenide pseudomorphic high-electron-mobility transistor (GaAs pHEMT) process. A single-IF architecture is chosen for the RF receiver. In the digital modem, 24 square root raised cosine filters and four (255, 239) Reed-Solomon forward error correction codecs are used in parallel. The modem can compensate for a carrier-frequency offset of up to 50 ppm and a symbol rate offset of up to 1 ppm. Experiment results show that the system can achieve a bit error rate of 10^{-5} at a signal-to-noise ratio of about 21.5 dB.

Keywords: E-band, 16-QAM, 10 Gigabit Ethernet, error correction code.

I. Introduction

As the demand for high-speed and high-capacity data communications increases, high-speed network technologies, such as Gigabit Ethernet (GbE) and 10 GbE, are being developed. However, it is quite difficult to establish wired networks in rough terrain, such as jungles, mountains, and waterways, and in regions affected by natural disasters. Thus, wireless point-to-point broadband networks, that is, wireless backhaul networks, are necessary in these areas. Recently, the USA, Canada, Europe, Korea, Australia, and Russia have allocated a total of 10 GHz of bandwidth in the E-band spectrum (71-76 GHz and 81-86 GHz) for wideband multi-gigabit wireless communications [1]. Most existing wireless backhaul systems are not bandwidth efficient, owing to the use of amplitude shift keying. Some recent studies showed that the bandwidth efficiency may be improved to 2.4 bit/s/Hz in 60 GHz communication and to 2 bit/s/Hz in E-band communication [2]-[7].

This paper presents a 16-quadrature-amplitude-modulation (QAM)-based highly spectral efficient eight-channel E-band wireless point-to-point broadband communication system. This system can achieve a bandwidth efficiency of 3.2 bit/s/Hz and a bit rate of up to 10 Gbps.

II. System Architecture and Function Blocks

Figure 1 and Table 1 show a block diagram and the specifications of the proposed system, respectively. The transmitter consists of eight digital modulators, eight quadrature digital-to-analog converters (DACs), eight IF up-converters, and one RF up-converter. Each digital modulator generates 16-QAM signals with a symbol rate of 312.5 Ms/s

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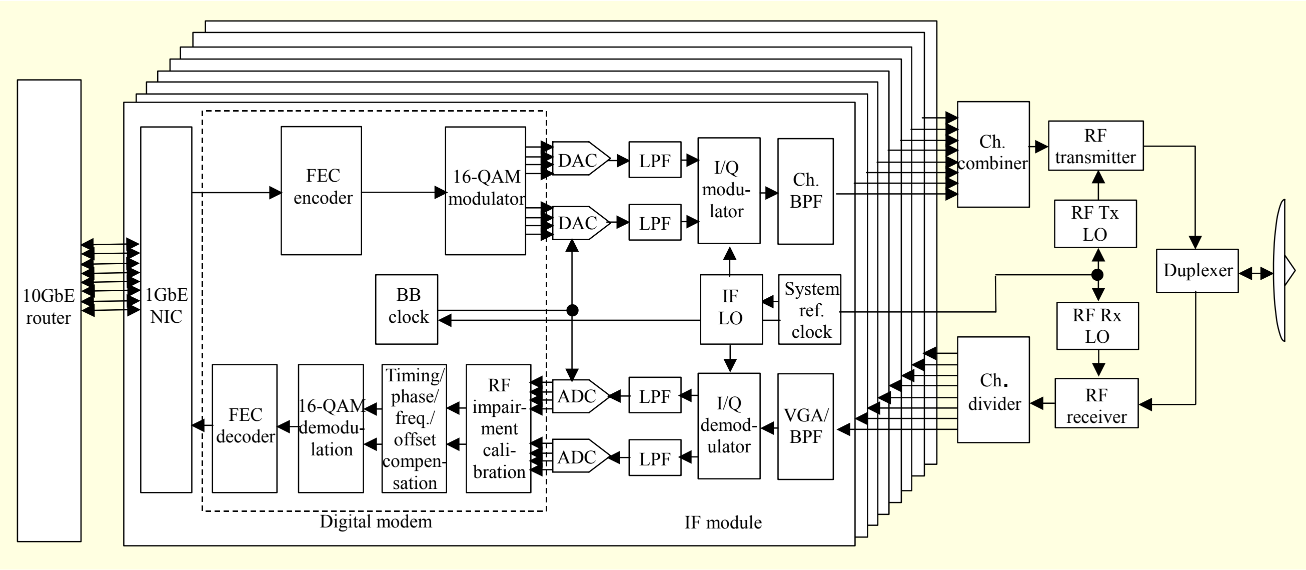


Fig. 1. Block diagram of proposed system.

Table 1. Specifications of proposed system.

Parameter	Specification
Frequency band	71-76 GHz, 81-86 GHz
Data rate	10 Gbps
No. of channels	8
Channel spacing	390 MHz
Modulation	16-QAM
Max. transmit power	10 dBm
Gain (RF transmitter)	22 dB @70 GHz band 24 dB @80 GHz band
Gain (RF receiver)	19 dB @70 GHz band 20 dB @80 GHz band
Output P1dB (RF transmitter)	10.5 dB @70 GHz band 15.6 dB @80 GHz band
Noise figure (RF receiver)	<10 dB

and an oversampling ratio of 3. For each DAC, the resolution is 12 bits and the sampling rate is 937.5 Ms/s. Eight IF up-converters up-convert the eight modulated signals to the 5 GHz to 10 GHz IF band with a channel spacing of 390 MHz. The RF up-converter up-converts the IF signal and transmits the resultant signal in the E-band spectrum. The maximum transmission power is 10 dBm. The receiver consists of one RF down-converter, eight IF down-converters, eight quadrature analog-to-digital converters (ADCs), and eight digital demodulators. The RF down-converter down-converts the RF signal to the 5 GHz to 10 GHz IF band. Each IF down-converter down-converts each channel signal to the baseband. The resolution of each ADC is 8 bits, and the sampling rate of each ADC is identical to that of the DAC. Each digital demodulator produces 1.25 Gbps of binary data.

Figure 2 shows a detailed block diagram of the RF/IF transceiver. In the IF transmitter, the digital-to-analog converted signal is low-pass filtered by a seventh-order Butterworth filter with a cutoff frequency of 288 MHz. A passive-type I/Q mixer is used for the up-conversion, with a conversion loss of 7 dB.

The channel band-pass filter (BPF) is used to reduce interchannel interference due to the output harmonic signals of the I/Q mixer. The insertion loss of the BPF is less than 2 dB. Eight IF channel signals are combined for RF transmission. For the RF up-converter, a driver amplifier (DA) and subharmonically pumped (SHP) mixer are designed and fabricated using a 0.1 μm gallium arsenide pseudomorphic high electron mobility transistor (GaAs pHEMT) process with a 50 μm wafer thickness, a cutoff frequency of $f_T \approx 120$ GHz, and a maximum oscillation frequency of $f_{max} > 200$ GHz. The DA uses a low impedance transmission line in an input matching network to achieve broadband gain [8]. In addition, a second SHP mixer is designed to decrease the package loss and cost. Figures 3 and 4 show chip microphotographs, schematics, and measurement results of the DA and SHP mixer, respectively. The chip sizes of the DA and SHP mixer are 2.8 mm × 2.1 mm and 1.1 mm × 1.5 mm, respectively. Table 2 summarizes the key measurement results for the DA and the SHP mixer. The developed system employs a Cassegrain-type antenna with 41 dBi gain, and a balanced-type low-noise amplifier (LNA) is used in the receiver. In addition, the receiver and transmitter RF mixers are identical. After channel band-pass filtering and I/Q mixing, automatic gain control (AGC) is

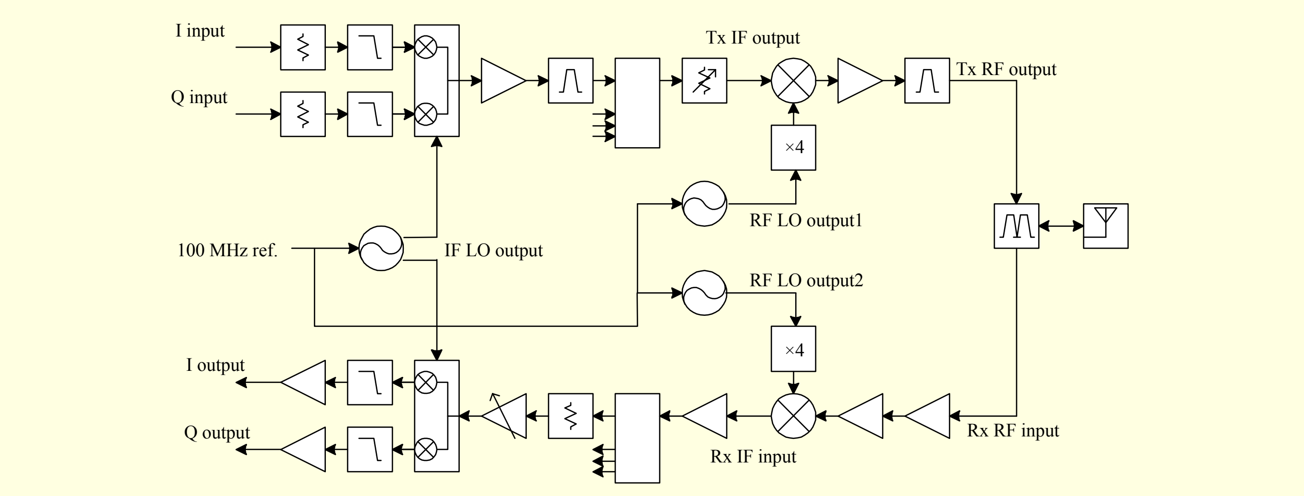
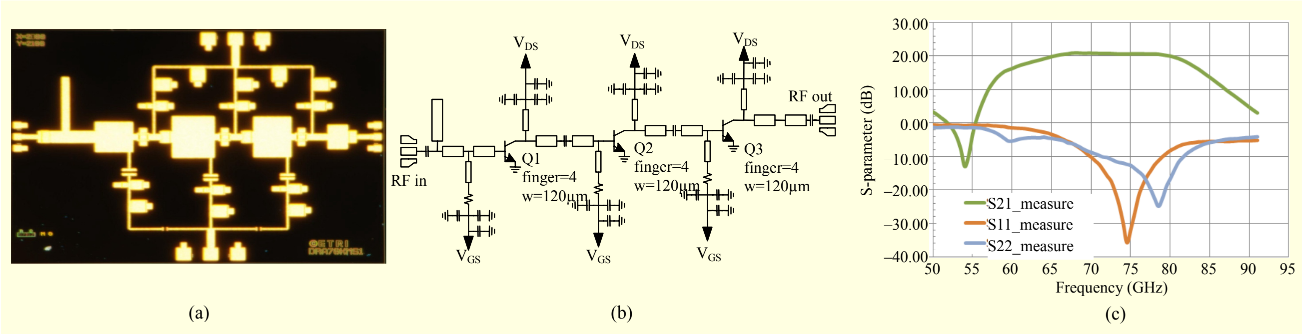
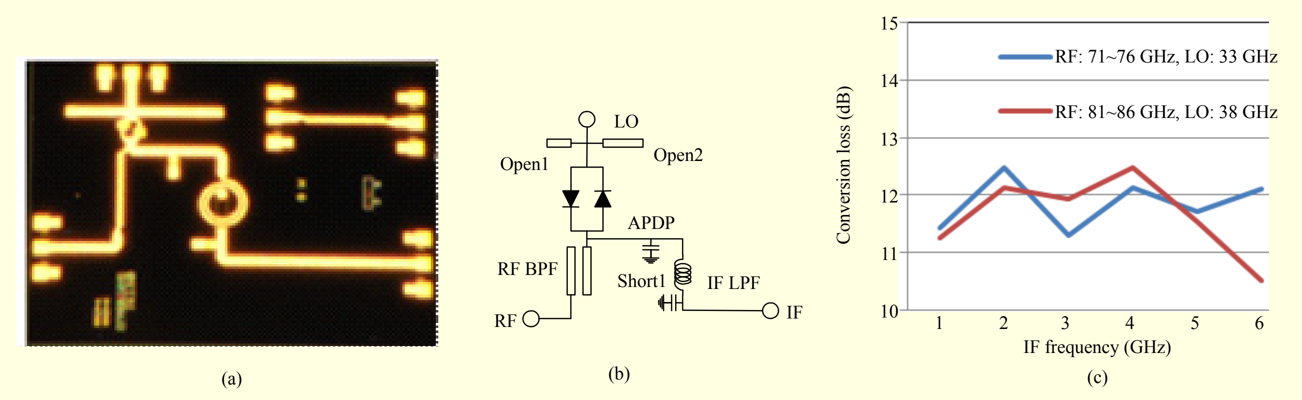


Fig. 2. Block diagram of RF/IF transceiver.



(a) (b) (c)

Fig. 3. (a) Chip microphotograph, (b) schematic, and (c) measured results of DA.



(a) (b) (c)

Fig. 4. (a) Chip microphotograph, (b) schematic, and (c) measured results of SHP mixer.

used to maximize the ADC dynamic range while avoiding clipping. The dynamic range of the AGC is 30 dB.

Figure 5 presents a block diagram of the digital modulator and demodulator. A digital modem is implemented in a XC5VSX240T field-programmable gate array (FPGA). Each data packet is composed of a preamble, start frame delimiter (SFD), and physical layer (PHY) payload. The preamble and SFD use a 32-symbol constant-amplitude zero autocorrelation (CAZAC) sequence and are modulated using quadrature phase-shift keying (QPSK). The SFD sequence is generated by exchanging the first 16 symbols and the second 16 symbols of the preamble CAZAC sequence. The PHY payload is modulated using 16-QAM. To reduce the operating frequency of each processing element, parallel processing with multiple function units is used in the modem. In each modulator, four (255, 239) Reed-Solomon (RS) forward error correction (FEC)

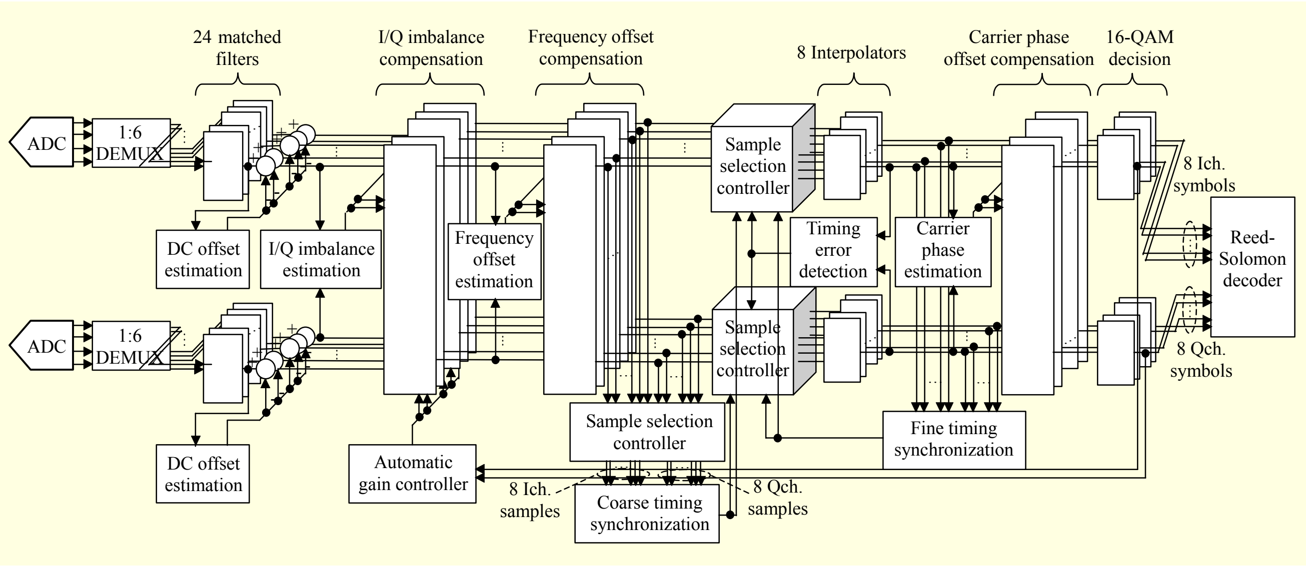


Fig. 5. Block diagram of digital modulator and demodulator.

Table 2. Key measurement results for DA and SHP mixer.

Parameter		Measurement result
DA	Gain	> 18 dB
	Output P1dB	> 16 dBm
	Power dissipation	54 mA @ 4 V
SHP mixer	Conversion loss	11-13 dB
	Input P1dB	1 dBm @86 GHz
	LO frequency	33 GHz @70 GHz band 38 GHz @80 GHz band

encoders load 32-bit data simultaneously [9]. Hence, when the input data rate is equal to 1.25 Gbps, the output symbol rate in each RS encoder becomes 41.68 Msymbol/sec. Four parallel RS encoded output symbols are mapped into eight parallel 4-bit streams by eight 16-QAM mappers. Using 24 polyphase pulse-shaping filters (PSF), the eight parallel 4-bit streams become 24 samples. A square root raised cosine (SRRC) filter with a roll-off factor of 0.25 is used for PSF. Finally, to utilize the 4:1 multiplexer in the DAC, 24 parallel samples are converted into four parallel samples using 6:1 multiplexing.

In each demodulator, utilizing the 1:4 demultiplexer in the ADC, the four parallel input sample streams are converted into 24 parallel samples with 1:6 demultiplexing. These samples are then match-filtered with 24 parallel SRRC filters with a roll-off factor of 0.25. The DC offset is removed using the feed-forward-based DC-offset compensation method. A feed-forward-based statistical I/Q imbalance estimation method is used to eliminate any I/Q imbalance [10]. The digital AGC has two operation modes: data-aided mode and decision-directed mode. Data-aided mode is used for the QPSK-modulated preamble signal, and decision-directed mode is used for the 16-QAM modulated PHY payload. Initial timing synchronization is then accomplished with the noncoherent cross-correlation scheme in two steps [11]. The first step is coarse timing synchronization within a 1/3 symbol period. The second step is fine timing synchronization and uses a third-order Lagrange interpolation filter. The timing accuracy is within a 1/24 symbol period. In the PHY payload, a modified Gardner timing error detector is used to estimate the residual timing error. A cross-product discrimination method is used to compensate for the carrier frequency offset [11]. It is worth noting that a frequency offset of up to 4 MHz, that is, 50 ppm, can be corrected to a residual frequency offset of 10 kHz. Carrier phase recovery is a two-step process [11]. In the first step, the data-aided mode is used to acquire the carrier phase for the QPSK-modulated preamble signal. In the second step, the decision-directed mode is used for the 16-QAM modulated PHY payload to track the residual carrier phase offset. Since the initial carrier phase acquisition is completed during the preamble, the coherent cross-correlation method can be used for SFD detection.

III. Experiment Results

Figure 6 shows photographs of the developed system. In Fig. 6(a), the gray box at the top is the RF transceiver and the black box at the bottom represents the eight-channel IF transceiver and digital modem. The demonstration system provides a data rate of 5 Gbps using four channels. Figure 7

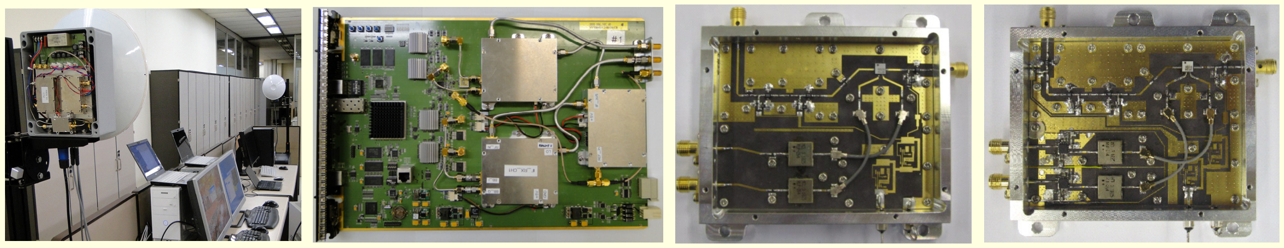

(a) (b) (c) (d)

Fig. 6. Photographs of developed system: (a) system setup for demonstration, (b) digital baseband and analog IF module, (c) IF transmitter module, and (d) IF receiver module.

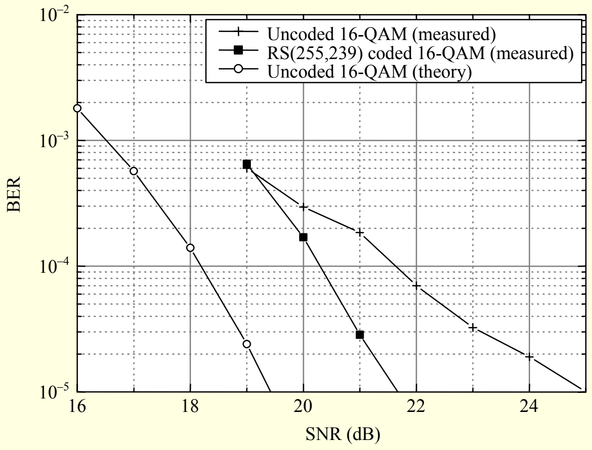


Fig. 7. Measured BER performance.

shows the measured bit error rate (BER) performance.1) The system produces a BER of 10^{-5} at a signal-to-noise ratio (SNR) of about 21.5 dB with an RS-FEC code. Likewise, it produces the same BER at an SNR of about 25 dB for the uncoded case, which is a performance degradation of about 5.5 dB at a BER of 10^{-5} compared to the theoretical 16-QAM performance in an additive white Gaussian noise (AWGN) channel. This degradation is caused by implementation loss in the digital modem (about 1 dB), high-pass filtering of the baseband analog signal, and implementation loss in the E-band microwave module.

IV. Conclusion

This paper presented an eight-channel E-band wireless point-to-point broadband communication system with 3.2 bit/s/Hz spectral efficiency. The system used 16-QAM to improve the spectral efficiency and an RS-FEC code to improve the performance. A DA and SHP mixer were fabricated and resulted in a gain of more than 18 dB and a conversion loss of 11 dB to 13 dB, respectively. The hardware measurement results showed a BER of 10^{-5} at an SNR of about 21.5 dB. If two-feet Tx/Rx antennas are used, the available communication range can be more than 1 km at a rain rate of 42 mm/hr. The developed system is applicable for high-speed wireless networks, wireless home networks, and wireless backhaul networks.

References

[1] SPP 2006-11, “Planning of the 71-76 GHz and 81-86 GHz Bands for Millimeter Wave High Capacity Fixed Link Technology,” *Australian Commun. Media Authority* (*ACMA*), Dec. 2006.

[2] V. Dyadyuk, Y. Jay Guo, and John D. Bunton, “Multi-Gigabit Wireless Communication Technology in the E-band,” *Proc. 1st Int. Conf. Wireless VITAE*, May 2009, pp. 137-141.

[3] S. Emami et al., “A 60GHz CMOS Phased-Array Transceiver Pair for Multi-Gb/s Wireless Communications,” *Proc. IEEE Int. Solid State Circuits Conf.*, Feb. 2011, pp. 164-166.

[4] A. Natarajan et al., “A Fully-Integrated 16-Element Phased-Array Receiver in SiGe BiCMOS for 60-GHz Communications,” *IEEE J. Solid-State Circuits*, vol. 46, no. 5, May 2011, pp. 1059-1075.

[5] D. Nakano et al., “Multi-Gbps 60-GHz Single-Carrier System Using a Low-Power Coherent Detection Technique,” *Proc. IEEE Symp. On Low-Power and High-Speed Chips* (*COOL Chips*), Apr. 2011, pp. 1-3.

[6] M. Kang et al., “Wireless PtP System in E-band for Gigabit Ethernet,” *Proc. Int. Conf. Adv. Commun. Technol.* (*ICACT*), Feb. 2010, pp. 733-736.

[7] *EtherHaul E-Band Radio*, Siklu Communication Ltd. Available: http://www.siklu.com

[8] M.S. Kang et al., “Power Amplifier for E-band Wireless Link Using 0.1 μm GaAs pHEMT,” *Proc. Int. Conf. Solid State Devices Mater.* (*SSDM*), Sept. 2011, pp. 192-193.

[9] S. Lin and D.J. Costello, Jr., *Error Control Coding: Fundamentals and Applications,* 2nd ed., Englewood Cliffs, NJ: Prentice-Hall, 2004.

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1) To measure the BER performance, transmitter, receiver, and AWGN signal generator are connected using cable and an adjustable attenuator is used to sweep the receiver input power.

[10] P. Rykaczewski et al., "Non-Data-Aided I/Q Imbalance Compensation using Measured Receiver Front-End Signals," *Proc. IEEE PIMRC*, 2006, pp. 1-5.

[11] U. Mengali and A.N. D'Andrea, *Synchronization Techniques for Digital Receivers*, New York: Plenum Press, 1997.

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