Dynamic Pixel Models for a-Si TFT-LCD and Their Implementation in SPICE

In-Soo Wang, Gi-Chang Lee, Tae-Hyun Kim, Won-Jun Lee, and Jang-Kyoo Shin

A dynamic analysis of an amorphous silicon (a-Si) thin film transistor liquid crystal display (TFT-LCD) pixel is presented using new a-Si TFT and liquid crystal (LC) capacitance models for a Simulation Program with Integrated Circuit Emphasis (SPICE) simulator. This dynamic analysis will be useful when predicting the performance of LCDs. The a-Si TFT model is developed to accurately estimate a-Si TFT characteristics of a bias-dependent gate to source and gate to drain capacitance. Moreover, the LC capacitance model is developed using a simplified diode circuit model. It is possible to accurately predict TFT-LCD characteristics such as flicker phenomena when implementing the proposed simulation model.

Keywords: Dynamic pixel models, a-Si:H TFT modeling, liquid crystal modeling, LCD SPICE simulation.

I. Introduction

The high quality of liquid crystal display (LCD) products is obtained through enhancing individual aspects such as high contrast, fast response, low power consumption, and compact shape, which results in high development cost. Being able to estimate the quality of the end product via computation is becoming imperative in the flat panel display industry.

We have rendered a dynamic simulation by implementing the amorphous silicon (a-Si) thin film transistor (TFT) model and the liquid crystal (LC) capacitance model in the commercial engineering software, Simulation Program with Integrated Circuit Emphasis (SPICE). An analysis of an a-Si TFT-LCD is presented in this letter. This analysis will be useful to the active matrix LCD designers for evaluating and predicting the performance of LCDs.

II. Dynamic Pixel Models

1. a-Si:H TFT Modeling

As shown in Fig. 1, the large size of the overlap capacitance, due to the four-mask TFT process adopted in the industry, and the dynamic characteristics of the gate and source/drain (S/D) contribute to the performance of the LCD. Therefore, we introduce a novel method to implement the dynamic capacitance characteristics of TFTs in the analysis model. The dynamic capacitance of a TFT consists of channel capacitance (C_{ch}), gate-source capacitance (C_{gs}), and gate-drain capacitance (C_{gd}). The values of each capacitance are measured, as shown in Fig. 2. The correlation between C_{gs} and C_{gd} is thoroughly investigated and the empirical equation of these two parameters is established (C_{gs} and C_{gd} are the overlap capacitance between gate and S/D metal). The capacitance between the channel and the dynamic behavior of these parameters, C_{ch}, is predicted by the conventional Rensselaer Polytechnic Institute TFT model [1].

The empirical equation (1) of the dynamic characteristics of the parameters C_{gs} and C_{gd} is as

$$C = C_{max} \times \left(1 - \frac{C_{max} - C_{min}}{C_{max} \times (1 + \mathrm{SLOPE}^{(V_{gs} - V_0)})} \right), \qquad (1)$$

where V_0 denotes initial voltage. Equation (1) is applied to TFT SPICE simulation. The measurement data is in agreement with the SPICE simulation results, as shown in Fig. 3. The TFT SPICE model [2] using (1) increases the accuracy of the LCD panel simulation [3].

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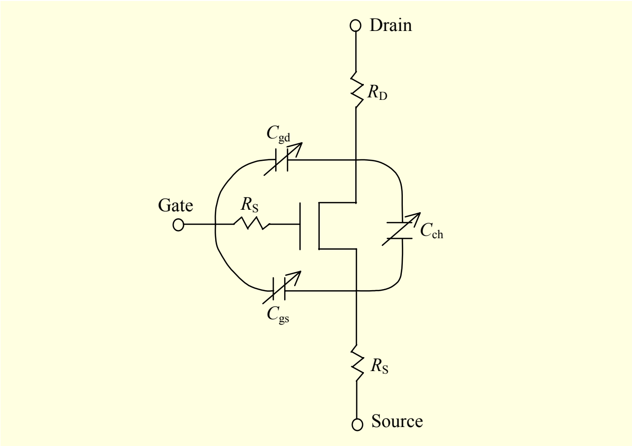

Fig. 1. Equivalent circuit of 4-mask processed TFT.

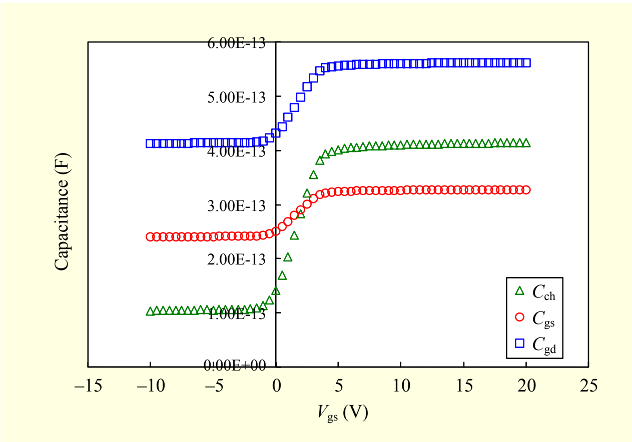

Fig. 2. Measured data of C_{ch}, C_{gs}, and C_{gd}.

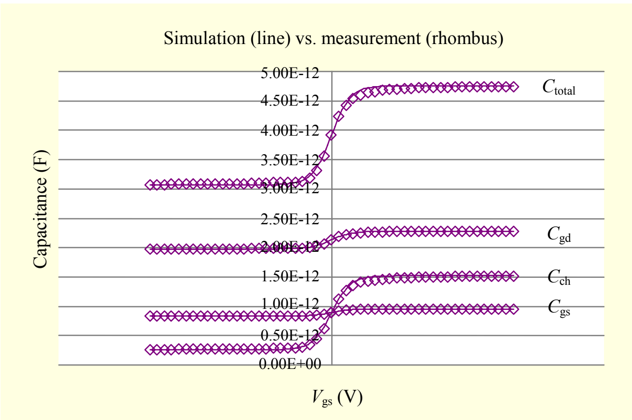

Fig. 3. Results of SPICE simulation matches up with measurement data.

The dynamic capacitance variation of C_{gs} and C_{gd} with the TFT width scale can be considered by the linear formula of the model parameters script, as listed in Fig. 4. The linear formula (the variation of capacitance with the TFT width scale) can be expressed using C_{max} and C_{min}.

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Dynamic model implementation for SPICE

xcgs g s dynamic_cap area="100"
xcgd g d dynamic_cap area="20000"
.subckt dynamic_cap a c
c1 a c c='c_max * (1 – (c_max – c_min) / (c_max * (1 + pwr(cslope, (v(a, c) –
cv0)))))'
.param
+c_MAX="2.00e–16*area"
+c_MIN="1.00e–16*area"
+cslope=10
+cv0=1
```

Fig. 4. TFT modeling for dynamic capacitance characteristic.

2. Liquid Crystal Modeling

To calculate the TFT-LCD charging ratio, which will increase the accuracy of the LCD panel simulations, LC capacitance models, as well as TFT capacitance models, should be estimated in the dynamic simulation. The value of LC permittivity, which directly relates to the change of the LC capacitance, varies in time because of the anisotropic characteristic of the LC. The permittivity of LCs is proportional to the voltage between LC electrode nodes. As a result, the capacitance of the LC panel varies with the time and voltage. Figure 5 shows the structure of a typical LC cell. Light passing through the LC is transmitted to the front view of the LCD panel with phase retardation heavily influenced by the LC capacitance [4].

In general, the response time of the LC depends on the externally applied voltage (V_{ext}). The time constant (τ) is as

$$\tau = \left(\frac{1}{a1 + a2 \cdot V_{ext}^2} \right). \tag{2}$$

Dynamic behavior of LCs is accurately predicted using the developed equivalent diode circuit, as shown in Fig. 6. The dynamic governing equation (3) of V_x in the macro-model of the LC pixel is derived from the equivalent diode circuit model. The equation is as follows:

$$I_1 = \frac{V_{in}}{(M1 + R1) + R2} = \frac{V_x}{R2}$$

$$\therefore V_x(t) = \frac{V_{in} R2}{(M1 + R1) + R2} \cong \frac{V_{in}(t)}{ax^2 + b}. \tag{3}$$

In (3), x denotes the physical rotational position of the LC and V_x denotes the output voltage determined by x (the rotational position of LC) and $V_{in}(t)$ (input voltage varying with time). Particularly, $M1$ denotes the transistor load model that is capable of describing the parabolic dynamic behavior of the LC(ax^2).

The transmittance predicted by SPICE simulation utilizing (3) is in agreement with the measured data, as shown in Fig. 7.

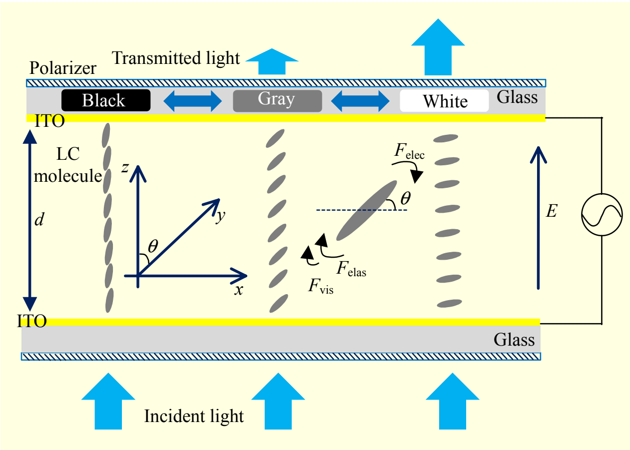

Fig. 5. Structure of typical LC cell.

The values of $M1$, $R1$, and $R2$ are optimally chosen for the SIPCE simulation using the optimization function provided by the SPICE.

There are a few differences at the rising edge between the experiment results and simulation results in Fig. 7. The accuracy of the simulation can be readily improved by developing an elaborate numerical model of the empirical equation (3). However, for the purpose of reducing computational cost, the simple and efficient empirical equation (3) is adopted for the simulation in this study.

3. LCD SPICE Simulation

To analyze the characteristics of the LCD panel, the SPICE

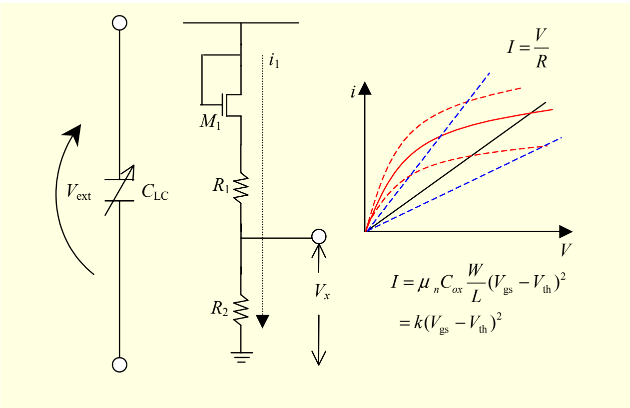

Fig. 6. Macro-model for LC dynamic characteristics.

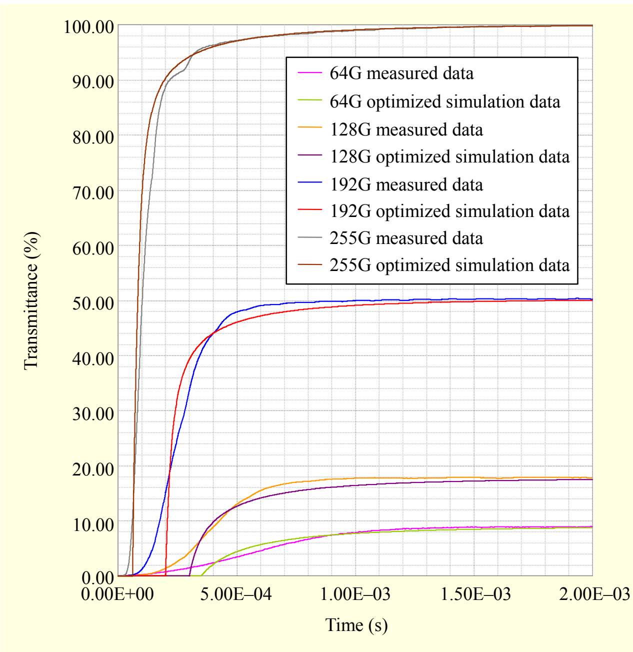

Fig. 7. Dynamic behavior comparison measurement with transmittance simulation result.

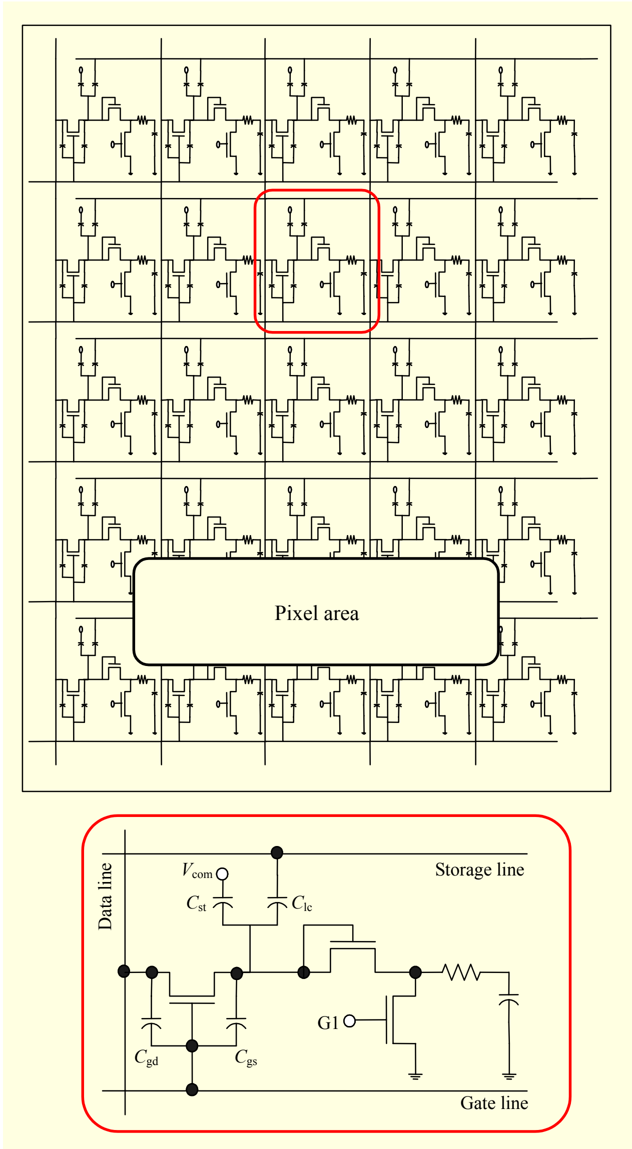

Fig. 8. Schematic drawing of array circuit and electrical diagram of one-pixel elements.

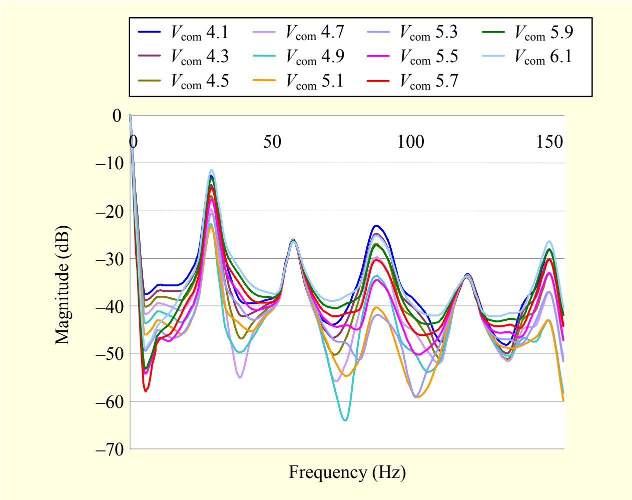

Fig. 9. Flicker simulation in LCD dependency on V_{com}.

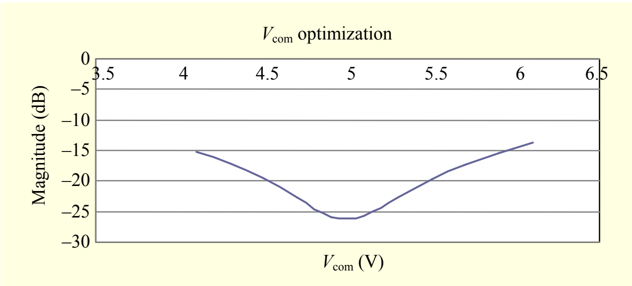

Fig. 10. Flicker level dependency on V_{com}.

simulations are performed utilizing the developed TFT model (C_{gs} and C_{gd}) and LC capacitance model. These models are directly used in the full panel simulation based on the equivalent one-pixel circuit model shown in Fig. 8.

In the TFT-LCD panel, the data line voltage signal alternates 1/frame. The frame itself also alternates at 75 Hz. The transmittance differences between the alternating frames induce a flicker into the image and degrade the quality of the display.

The simulation result, as shown in Fig. 9, proves that the flicker level is reduced using the full panel model, which consists of the proposed pixel models when the optimized V_{com} value of 5.1 V is applied.

These results demonstrate that the optimal value of V_{com} to reduce the flicker level can be sought using the full panel model simulation with the proposed pixel models.

Furthermore, these results also show that the magnitude level at 30 Hz is the main source of the flicker and the threshold level is 20 dB. In this case, 30 Hz corresponds to half of the frame rate of the TFT-LCD. To obtain the optimal value of V_{com}, a calculation is performed using the Fourier transformation, the result of which is shown in Fig. 10. This result suggests that V_{com} should be optimized as 5.0 ±0.5 V to minimize the flicker level.

III. Summary

In this letter, a full panel model was developed using the proposed TFT (C_{gs} and C_{gd}) and LC capacitance models. The dynamic characteristics of the LCD products, such as flickers, were accurately predicted through the SPICE simulation with our proposed full panel model.

The product designers will be able to apply our full panel model to optimize the V_{com} level with the help of the developed SPICE simulation method to avoid flicker phenomena in the LCD products, achieving the required quality with a benefit of cost reduction.

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