A Low-Spur CMOS PLL Using Differential Compensation Scheme

Seok-Ju Yun, Kwi-Dong Kim, and Jong-Kee Kwon

This paper proposes LC voltage-controlled oscillator (VCO) phase-locked loop (PLL) and ring-VCO PLL topologies with low-phase noise. Differential control loops are used for the PLL locking through a symmetrical transformer-resonator or bilaterally controlled varactor pair. A differential compensation mechanism suppresses out-band spurious tones. The prototypes of the proposed PLL are implemented in a CMOS 65-nm or 45-nm process. The measured results of the LC-VCO PLL show operation frequencies of 3.5 GHz to 5.6 GHz, a phase noise of –118 dBc/Hz at a 1 MHz offset, and a spur rejection of 66 dBc, while dissipating 3.2 mA at a 1 V supply. The ring-VCO PLL shows a phase noise of –95 dBc/Hz at a 1 MHz offset, operation frequencies of 1.2 GHz to 2.04 GHz, and a spur rejection of 59 dBc, while dissipating 5.4 mA at a 1.1 V supply.

Keywords: Phase-locked loop (PLL), differentially-tuned, CMOS, voltage-controlled oscillator (VCO), spur rejection, transformer, integrated circuit design.

I. Introduction

Phase-locked loops (PLLs) are important building blocks in modern communication systems. A PLL generates a clock signal with a sufficiently large frequency range to account for process, voltage, and temperature variations and to support multi-band and multi standard operation. With a seamless scale-down of the CMOS process and integration of digital circuits, an operating supply voltage is being lowered for low-power, nanoscale implementation. Hence, voltage-controlled oscillators (VCOs) generating the output frequency are required to have a large tuning constant (K_{VCO}-frequency variation per volt).

Unfortunately, for integrated PLLs, a large K_{VCO} leads to PLL phase noise degradation as it translates various noise sources on the control line to the frequency modulation in the output signals. Moreover, fluctuation of the VCO control line from the common mode noise coupling becomes more sensitive for a low supply in a scaled down CMOS process and a wide loop bandwidth. To reduce the sensitivity, dividing a frequency tuning curve into several small bands is used such that a wide frequency range can be achieved with a small K_{VCO}. However, the required switches for the subband degrade the VCO phase noise performance.

A differentially-tuned PLL (DT-PLL) topology is a good choice for low common-mode sensitivity and a wide tuning dynamic range [1]-[6]. However, the DT-PLL has unwanted spurious tones from the frequency comparison process, which may create severe problems since a phase error from a current mismatch of the charge pump is larger compared to the normal PLL [5]. Moreover, reference ripples on the VCO control line from the leakage current increase in scaled-down CMOS processes. The ripples can be reduced either by increasing the

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Seok-Ju Yun (phone: +82 10 2518 6617, stoneju@kaist.ac.kr) was with the Convergence Components & Materials Research Laboratory, ETRI, Daejeon, Rep. of Korea, and is now with Samsung Electronics, Rep. of Korea.

Kwi-Dong Kim (kdkim@etri.re.kr) and Jong-Kee Kwon (jkkwon@etri.re.kr) are with the Convergence Components & Materials Research Laboratory, ETRI, Daejeon, Rep. of Korea.

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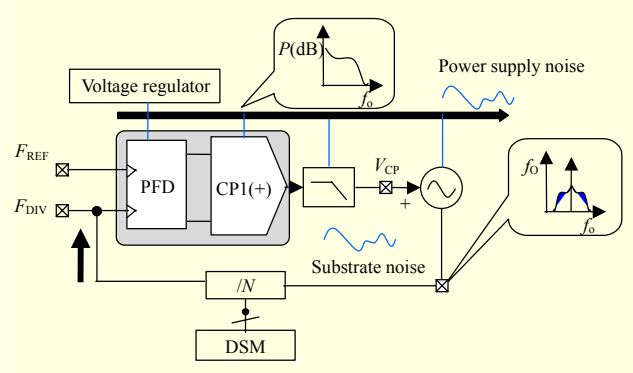

Fig. 1. Common-mode noise in PLL.

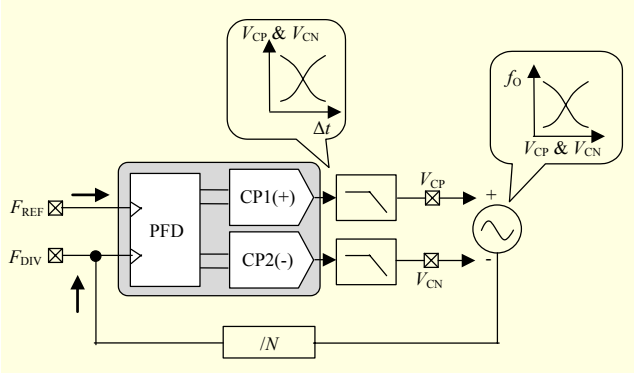

Fig. 2. Concept of DT-PLL.

size of the loop filter capacitor for a given PLL bandwidth, leading to an increased die area, or by reducing VCO gain, resulting in a reduction of the tuning range.

A ring-VCO PLL with a wide bandwidth is popular due to a small die area and scalable usage. In a wide bandwidth PLL, in-band noises from phase frequency detectors (PFDs), charge pumps, and loop filters can be more degradable in terms of overall jitter performance. Moreover, the output spur noise is less filtered out in a wide bandwidth and is difficult to remove. To remove the spur, complicated ripple-suppression blocks are required [7].

In this paper, section II presents a discussion on the common-mode noise of the integrated PLL and its loop sensitivity. In section III, to suppress the spurious tone and common-mode noise effectively, a new DT-PLL topology is suggested. Section IV suggests a ring-VCO-based DT-PLL and analyzes its noise. Section V gives measurement results of the two DT-PLLs, that is, the LC-VCO- and ring-VCO-based PLLs, implemented in CMOS 65-nm and 45-nm processes, respectively. The PLL prototypes exploit the performance of low-phase noise and low out-band spur. Finally, section VI provides some concluding remarks.

II. Common Noise in Integrated PLL

In integrated circuits, a supply fluctuation and substrate noise due to a low resistance substrate in various paths degrades the circuit performance. These fluctuations act on common-mode nodes in a differential circuit, and the common-mode noise can be effectively suppressed during differential operation while a single-ended circuit undergoes severe interference. Similarly, in the general PLL designs, high common-mode sensitivity leads to high phase noise performance; moreover, as the supply voltage is lower, the PLL becomes more sensitive to the noise.

The common-mode noise mostly disturbs signals at the VCO terminals, which determine the oscillation frequency. The noises are transferred into an oscillation frequency and added to the phase noise as shown in Fig. 1 [5]. To implement an insensitive PLL for a supply fluctuation and common-mode noises, much consideration is required.

In addition, spurious tones as a large noise source in the PLL outputs are generated mostly by a voltage ripple from the up-down current mismatch of the charge pump, leakage current, and so on. The spurious tones can be suppressed by reducing the loop bandwidth and improving the linearity of the key circuit block such as the charge pump, divider, and PFD. However, reducing the bandwidth degrades in-band phase noise, increases the loop filter size, and makes a resulting slow settling time.

To increase the input dynamic voltage range and keep K_{VCO} at a proper value in a given frequency band, the DT-PLL architecture is effective [1]. Figure 2 shows a conventional DT-PLL. The DT-PLL is composed of two feedback loops and includes a DT-VCO, two PFDs, loop filters, and charge pumps. The output frequency of the VCO is controlled by plus and minus tuning voltages (V_{CP} and V_{CN}), complementally. Since the DT-PLL uses two control loops, the varactor dynamic voltage is extended and is not bound by power or supply noise modulating the bias and common-mode noise [1].

In a single loop PLL, the output spur is proportional to the square of $K_{VCO} \cdot v_m / f_m$ (assuming that the tuning voltage of the VCO is modeled by $v_m \cdot \cos(2\pi \cdot f_m t)$), where K_{VCO} is the gain of the tuning voltage, v_m is the voltage ripple amplitude, and f_m is a comparison frequency of the PFD. Although voltage ripples from the up-down current mismatch and current leakage are inevitable, the ripple should be suppressed for high performance in a charge pump PLL, and a small K_{VCO} is suitable to reduce the spur noise in a low supply design.

Figure 3 shows the current mismatches of the two charge pumps in the DT-PLL. In the steady state of the PLL, the two control voltages are settled to lock a fixed frequency. Assuming that the current mismatch between the two charge pumps is much smaller than the mismatch between the up-down currents, the relation of the current mismatches of the charge

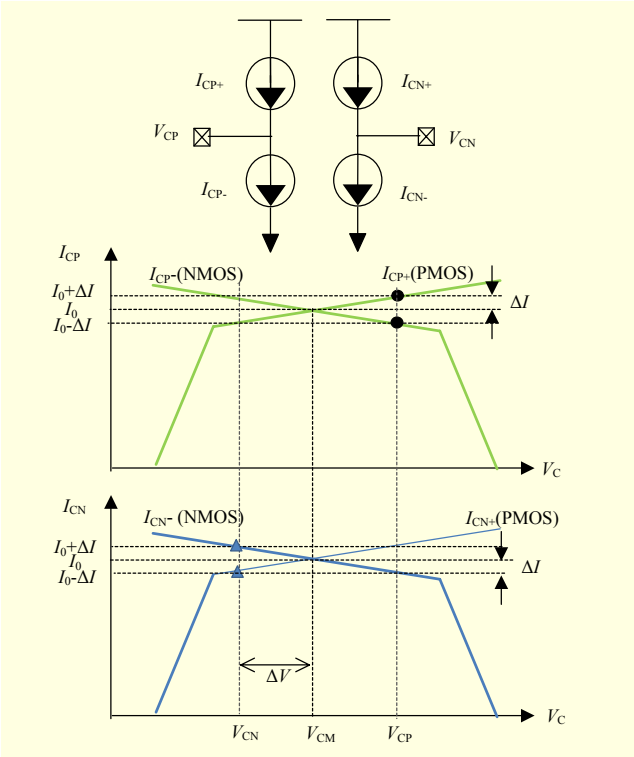

Fig. 3. Current mismatches of charge pumps in DT-PLL.

pump can be expressed as

$$I_{CP+} \approx I_{CN-} = I_0 + \Delta I, \\ I_{CP-} \approx I_{CN+} = I_0 - \Delta I, \quad (1)$$

where I_{CP+}, I_{CP}- and I_{CN+}, I_{CN}- are the up-down currents of the two charge pumps, respectively, I_0 is the current at the common-mode voltage, V_{CM} (that is, $(V_{CP}+V_{CN})/2$), and ΔI is a current error. The common and differential components of the current error can be given as

$$\Delta I_{cm} = I_{CP+} - I_{CP-} + I_{DN+} - I_{DN-} = 0, \\ \Delta I_{diff} = I_{UP+} - I_{DN+} - (I_{DN-} - I_{UP-}) = 4\Delta. \quad (2)$$

In the DT-PLL, the differential current error is twice that of the singe path PLL (≈ 2Δ). Hence, the voltage ripple caused by the current error worsens the PLL noise.

In terms of control voltages of the VCO, two control voltages accompany the voltage ripples. The output frequency of DT-PLL with the ripple voltages can be expressed by $f_{OSC} = f_0 + k_{VCOp}[V_{CP}(t) + v_{m1}(t)] + k_{VCOn}[V_{CN}(t) + v_{m2}(t)]$, where f_0 is the VCO free-running frequency, k_{VCOp} and k_{VCOn} are VCO gains for positive and negative control voltages, and $v_{m1}(t)$ and $v_{m2}(t)$ are voltage ripples on the control voltages. In a conventional DT-PLL, $v_{m1}(t)$ and $v_{m2}(t)$ are almost differential due to the contrary polarity of the charge pump current. In the output frequency through a DT VCO, two control voltages $V_{CP}(t)$ and $V_{CN}(t)$ are subtracted from each other ($V_{CD}(t) = V_{CP}(t) - V_{CN}(t)$). Assuming that the plus- and minus-frequency tuning curves are almost symmetrical (that is, $k_{VCOp} \approx -k_{VCOm} = k_{VCO}$) [4], the oscillation frequency is revised as

$$f_{OSC} = f_0 + k_{VCO}[V_{CD}(t) + v_{m1}(t) - v_{m2}(t)]. \quad (3)$$

From (3), the modulated output spur is proportional to the multiplication of $[v_{m1}(t)-v_{m2}(t)]$ and k_{VCO}. Therefore, in a conventional DT-PLL, the differential error from charge pump mismatches is directly converted into reference spurs with the offsets of multiple reference frequencies modulating the output frequency. With the usage of two charge pumps, total mismatch errors may increase twofold compared to the single loop PLL [6]. By taking the differential voltage, the common-mode components of the voltage ripples in the DT-PLL are suppressed, whereas the differential components of the ripples are increased resulting in a drastic increase of the output spur. To reduce the effective voltage ripples, the phases of the ripples should be properly adjusted. In the next session, the architectural solution of the DT-PLL will be presented with improved common mode immunity.

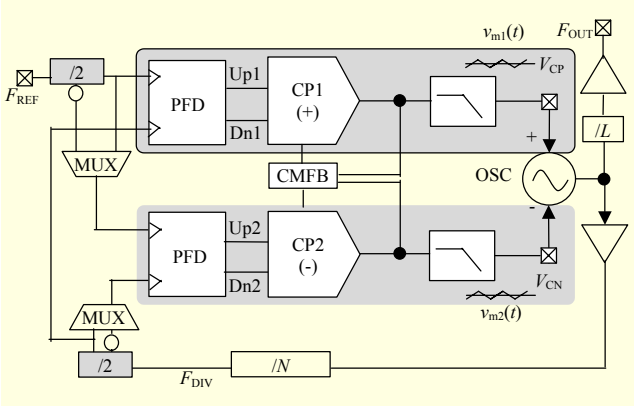

Fig. 4. Proposed DT-PLL.

III. DT-PLL Design

Figure 4 shows a proposed DT- PLL. Two feedback loops of the proposed DT-PLL comprise differently phased operating blocks. By selecting one of two outputs of a divider with a mux-switch, the input signals of a PFD can be differential or a common signal compared to inputs of the other PFD. In differential mode, open-loop circuits (PFD & charge pump) are operated with a timing delay of $1/2f_{REF}$ compared to the other loop circuits. As a result, the phase between the voltage ripples is adjusted to be similar. Figure 5 shows the timing diagram of the differential paths at a PLL locking state in the common- and differential-mode DT-PLL, in (a) and (b), respectively. With the up-down current mismatch in the two charge pumps, mismatch pulses (ΔI_{CP1}, ΔI_{CP2}) are created, resulting in the voltage ripples (ΔV_{CP} and ΔV_{CN}) of the control voltages. These voltage ripples

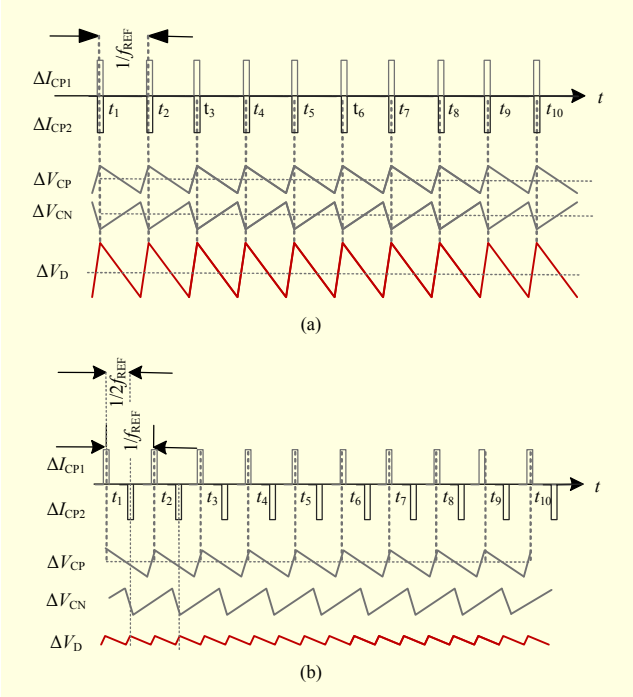

Fig. 5. Timing diagrams of differential paths in DT-PLL: a) common-mode; b) differential-mode.

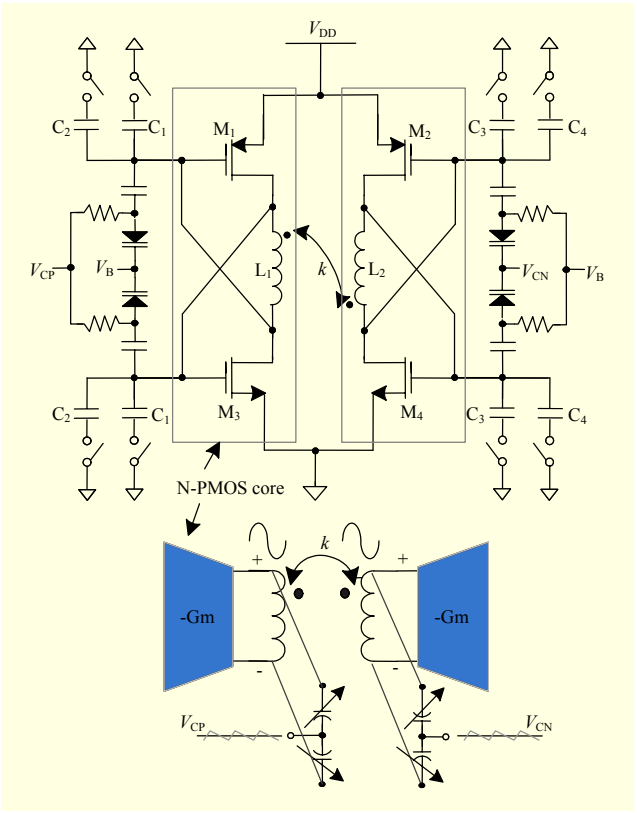

Fig. 6. LC-VCO schematic.

are periodic with the reference frequency (that is, $v_{m1,2}(t) = v_{m1,2}(t+1/f_{ref})$). As shown in Fig. 5, the voltage ripples in the differential mode are almost in phase due to the phase delay of $1/2f_{REF}$, while the voltage ripples are differential in the common-mode. Thus, by taking the differential voltage (V_D), the voltage ripples in the differential-mode DT-PLL are reduced considerably while the common-mode DT-PLL produces the large amplitude of the ripple.

In other words, the differential-mode DT-PLL suppresses a common-mode signal, which contains various mismatches occurring from noisy PLL blocks. The common-mode fluctuations of the PLL block disturb the VCO frequency at the control nodes. Therefore, as another requirement for high common-mode noise suppression, a high common-mode rejection ratio (CMRR) in the differential control ports of the VCO is needed [8]. In the DT-PLL operation, a high CMRR is achieved by symmetry between the differential control ports and by maintaining the common-mode voltage on half of the supply voltage through internal common-mode feedback circuits.

Generally, increasing the charge pump current causes a large current mismatch and noise increase in the CP-based PLL. Whereas, in the proposed DT-PLL, the operation current and delay mismatches do not directly result in the noise and spur increase because the common-mode mismatch is eliminated internally. Figure 6 shows a schematic of a DT-VCO. A symmetrical transformer is used as an inductor of a resonator. In each coil of the transformer, a complementary oscillator core [8] and a varactor pair for the differential-tuning are connected. The current source of the VCO is omitted for a larger output swing with a provision of enough large operational current. Equivalent circuits for the differential ports will improve the symmetry and LC-tank quality [9]. The low-noise characteristic of the complementary structure in a low frequency offset allows the PLL loop bandwidth to be reduced for low out-band spurious tones [10]. The inputs of the VCO are connected to a differential loop filter through the large register to prevent the oscillation from frequency shifting. Moreover, the metal routing of the two control lines in the layout is carefully drawn for differential symmetry, representing the high CMRR.

IV. Ring-VCO-based PLL

A ring-VCO is frequently chosen for compact implementation and easy realization in the PLL design. Setting the loop bandwidth as large, the phase noise can be optimized by shrinking the VCO noise contribution. Figure 7 shows a schematic of the ring-VCO used in the DT-PLL. The ring-VCO is composed of 4-stage differential delay cells. Each stage adopts a pair of varactors that adopt differential tuning

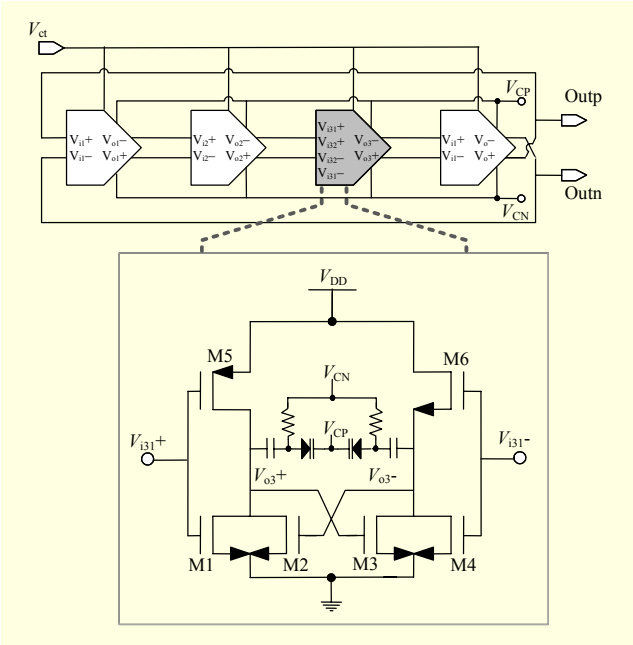

Fig. 7. Ring-VCO schematic with differential tuning ports.

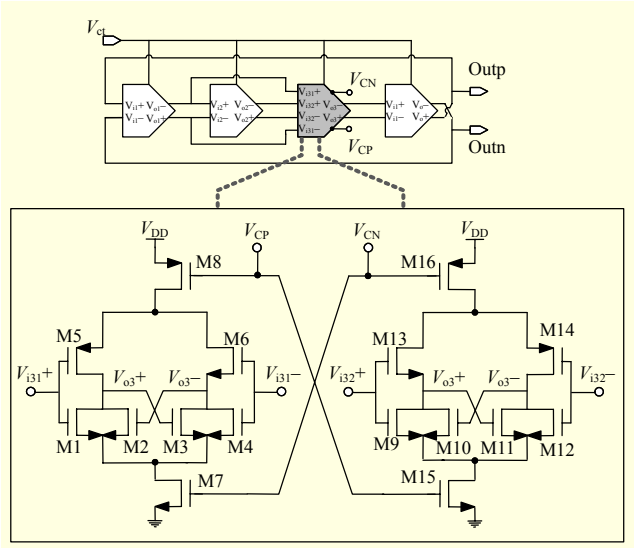

Fig. 8. An example of ring-VCO schematic with differential tuning ports.

ports, and 3-bit binary capacitors are included to extend the frequency range.

The oscillation frequency of the ring-VCO is in inverse proportion to $2 \cdot N \cdot R_{load} \cdot C_{load}$, where N is the number of stages, and R_{load} and C_{load} are respectively the equivalent loading resistance and the equivalent loading capacitance seen at the output node of each stage. Therefore, K_{VCO} of the VCO is given by

$$K_{VCO} = \frac{\partial f_{osc}}{\partial V_C} = -\frac{1}{2 \cdot N \cdot R_{load} \cdot C_{load}^{\ 2}} \cdot \frac{\partial C_{load}}{\partial V_C} = -\alpha \cdot \frac{\partial C_{load}}{\partial V_C} \text{ (Hz/V)}. \quad (4)$$

In Fig. 7, a differentially controllable varactor provides variable capacitance through plus- and minus-tuning voltages (V_{CP} and V_{CN}). Therefore, the varactor tuning voltage is not bound to supply noise modulating the bias and common-mode noise. The sensitivity of the tuning voltage is only valid at the differential voltage, not the common-mode voltage. The common-mode sensitivity, K_{CM}, is the rate of frequency changes from common-mode signals, such as supply voltage fluctuations or input common-mode noise. The value of K_{CM} is affected by differential errors due to compensation of leakage currents or imperfections in the charge pump's implementation or asymmetry between the plus- and minus-tuning curves. K_{CM} derived from two open-loop paths of the differential tuning (that is, control paths through a PFD, charge pump, loop filter, and VCO in Fig. 4) can be expressed by a multiplication of the two sensitivities, a sensitivity of the common-mode signal (V_{CM}) to the filter output voltage (V_{LF}) and a sensitivity of the filter voltage to the VCO frequency. This common-mode sensitivity can be given as

$$K_{CM} = \frac{\partial \omega_0}{\partial V_{CM}} \approx \frac{\partial I_{CP}}{\partial V_{CM}} \cdot \frac{\partial V_{LF}}{\partial I_{CP}} \cdot K_{VCOCM}, \quad (5)$$

where I_{CP} and K_{VCOCM} are the charge pump current and common mode sensitivities of the control voltage to VCO frequency, respectively. K_{VCOCM} is approximately expressed as a summation of the plus- and minus-tuning, and the equation is revised as

$$K_{CM} = \frac{\partial I_{CP}}{\partial V_{CM}} \cdot \left| \frac{\partial V_{CP}}{\partial I_{CP}} \cdot K_{VCOp} + \frac{\partial V_{CN}}{\partial I_{CP}} \cdot K_{VCOn} \right|$$
$$= -\alpha \cdot \frac{\partial I_{CP}}{\partial V_{CM}} \cdot \left[\frac{\partial V_{CN}}{\partial I_{CP}} \cdot \frac{\partial C_{loadp}}{\partial V_{CN}} - \frac{\partial V_{CP}}{\partial I_{CP}} \cdot \frac{\partial C_{loadm}}{\partial V_{CN}} \right] \text{(Hz/V)}, \quad (6)$$

where C_{loadp} and C_{loadm} are equivalent capacitances that are controllable by the plus- and minus-tuning voltages, respectively. From (6), to reduce common-mode sensitivity, mismatch compensation between two charge pumps and the common-mode immunity of the VCO tuning curves are required.

The DT-PLL architecture described in section III has an error-compensated control loop generated from the charge pumps. Symmetry between the plus and minus tuning curves improves the ability to reject common-mode noise from the differential input ports.

The role of the differentially-controlled varactor in Fig. 7 can be implemented by complementary current switches. Figure 8 shows another ring-VCO schematic with differential tuning ports. Three or four delay cells are activated through the use of

control voltages, and three- or four-stage ring-VCOs generate high- and low-frequency bands, respectively. The number of changes of stages provides wide frequency tuning compared to the current controlled ring-VCO. Current switches ($M_7/M_8/M_{15}/M_{16}$) select operational delay numbers controlled through the differential tuning voltage. When the control voltage is high, the number of stages is three, and the VCO operates at maximum frequency, and when the control voltage is low, the number of the stages is four, and the VCO operates at minimum frequency. The VCO will generate an intermediate frequency around the middle of the control voltage. The optimized width of the control switch transistors helps the ring-VCO produce quite symmetrical frequency tuning curves between the differential control ports. Assuming that two tuning curves are equivalent as a unity value, K_{VCO} can be calculated approximately as $1/24 \cdot R_{eq} \cdot C_{eq}$ (that is, $f_{max} - f_{min} = 1/2 \cdot 3 \cdot R_{eq} \cdot C_{eq} - 1/2 \cdot 4 \cdot R_{eq} \cdot C_{eq}$).

In the DT-PLL implementation, the ring-VCO in Fig. 8 is excluded, as the current controlled oscillator exhibits relatively high phase noise due to noisy currrent sources.

V. Measurement Results

Two DT PLLs are implemented in the CMOS processes. These are an LC-VCO-based DT-PLL and ring-VCO-based DT-PLL implemented in 65-nm and 45-nm CMOS processes, respectively. In the LC-VCO PLL, as shown in Fig. 9, a symmetrical transformer is used by means of coupled octagonal coils that are symmetrical, with a thickness of 3.2 μm. The measured frequency range is 3.5 GHz to 5.6 GHz. Figure 10 shows the phase noise of the DT-PLL observed in a loop bandwidth of 200 kHz. The measurement was performed in common- and differential-mode DT-PLLs, as described in Fig. 5. As shown in Fig. 10, the differential-mode DT-PLL shows a measured phase noise of –117.9 dBc/Hz at a 1 MHz offset, and a measured out-band spur tone is measured with an 89.2 MHz reference frequency. The spur suppression at

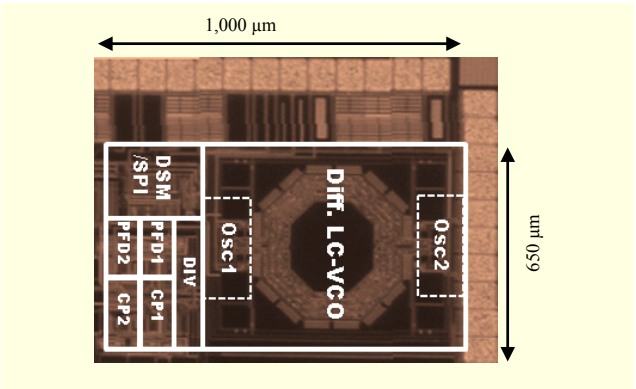

Fig. 9. Photograph of DT-PLL based on LC-VCO.

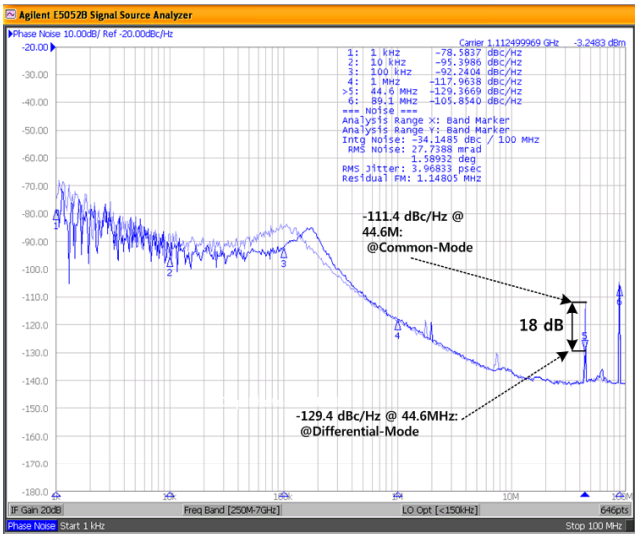

Fig. 10. Measured phase noise performance of DT-PLL.

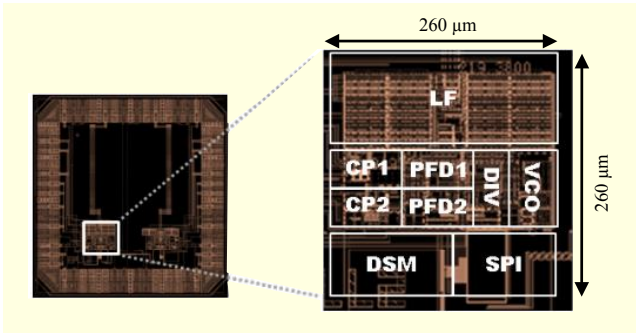

Fig. 11. Layout of DT-PLL based on ring-VCO.

44.6 MHz is 66 dB, which is about an 18 dB improvement compared to that of a common-mode DT-PLL (≈ 48 dB suppression). The measurements are performed at the outputs of a divider-by-4 after the VCO. The total power consumption of the DT-PLL is 3.2 mW at a 1 V supply, and the active chip size of the PLL is 0.65 mm^2. The DT-PLL with a ring-VCO is implemented in a 45-nm CMOS process. The DT-PLL has a fully integrated loop filter for a small chip size. Figure 11 shows a layout of the DT-PLL, and the active chip size of the DT-PLL is only 0.067 mm^2. Because the surface of the chip is entirely covered with the molding material, the layout picture is suggested instead of the chip photograph.

Figure 12 shows the measured tuning curves of the PLL. Each delay cell in the ring VCO has a 3-bit binary capacitor array, and the VCO covers a frequency range of 1.204 GHz to 2.044 GHz.

Figure 13 shows the measured phase noise of the DT-PLL. The measurement result is a phase noise of –95 dBc/Hz at a 1 MHz offset. To compensate the high phase noise of using the ring-VCO, the bandwidth of the loop filter is extended to

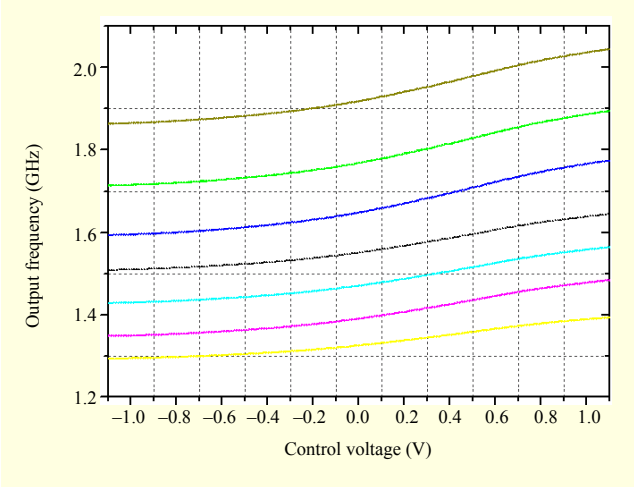

Fig. 12. Measured frequency tuning curves.

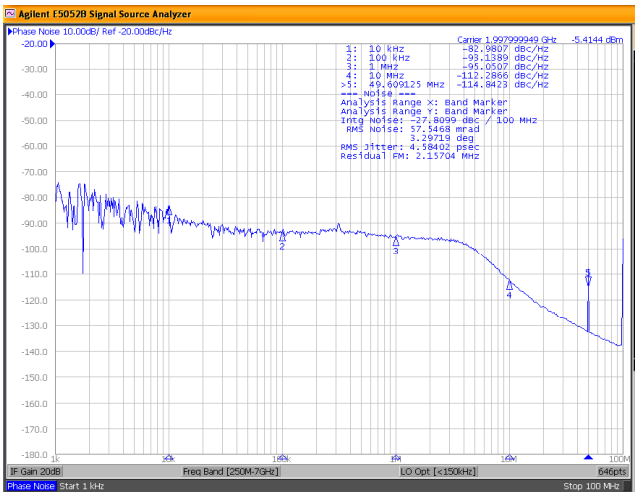

Fig. 13. Measured phase noise of DT-PLL based on ring-VCO.

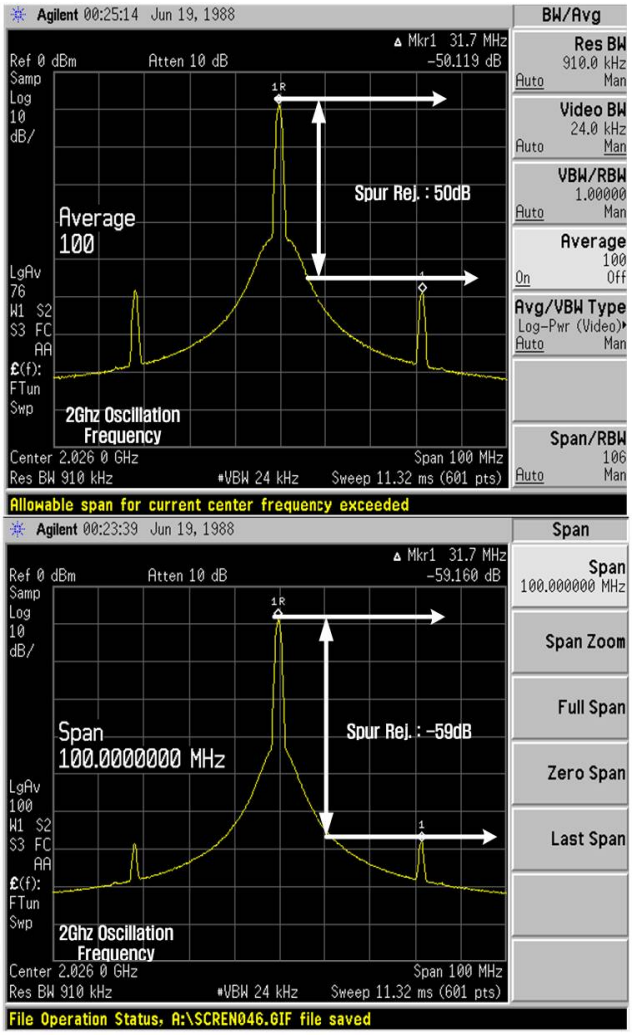

Fig. 14. Measured spectrum of ring-VCO DT-PLL.

4 MHz. The loop filter is implemented through a differential structure, reducing the chip size [1].

Figure 14 shows the measured spectrum representing the spurious tones. In the 2 GHz oscillation frequency, the measured spurious tone rejection at a 31.7 MHz offset is 59 dBc. The measured spur improvement at the differential mode is 10 dB compared to that of the common-mode PLL. Due to the use of a wide loop bandwidth of the DT-PLL, the spur suppression in the differential mode is lower than that of the LC-VCO DT-PLL with a narrow bandwidth.

The differential-mode operation of the DT-PLL is an effective way to suppress common-mode noise and reference spurs in the DT-PLL design. Setting the loop bandwidth sufficiently high reduces the noise contribution of the ring-VCO in the overall PLL noise. Table 1 shows a summary of the differential-mode DT-PLL performances. The ring-VCO DT-PLL is inferior to the LC-VCO DT-PLL in respect to the noise and power dissipation performance, while the die area is much smaller. Compared to previous low spur PLLs, the proposed differential-mode DT-PLL shows good performance even though it has a wide bandwidth. We think that a more considerable design can improve the DT-PLL performance with respect to the ring-VCO design and noise isolations of the chip layout compared to the performance exploited in this research.

VI. Conclusion

Two DT-PLLs were introduced in this paper. The differential operation of the positive and negative control loops suppressed the spurious tones and common-mode imbalance, effectively. The measured results of the LC-VCO DT-PLL implemented in a 65-nm CMOS process showed operation frequencies of 3.5 GHz to 5.6 GHz, a phase noise of –118 dBc/Hz at a 1 MHz offset, and a spur rejection of 66 dBc, while dissipating 3.2 mA at a 1 V supply. The ring-VCO-based DT-PLL implemented in

Table 1. Performance comparison of DT-PLLs and low-spur PLLs.

	Ring-VCO PLL	LC-VCO PLL	[1]	[2]	[11]	[12]	[13]
Supply voltage (V)	1.1	1.2	1.1	1.8	1.8	1.8	1.2
Power consumption (mW)	5.4	3.2	37.4	25	36	59	12
Frequency range (GHz)	1.2 to 2.04	3.5 to 5	4 to 6.4	0.5 to 2.5	5.2 to 6.2	0.4 to 1.2	2.4
Phase noise @ 1 MHz (dBc/Hz)	–95	–119	-	-	–113	-	–120.5
Spur rejection (dBc)	59	66	-	-	76	-	65
Jitter (ps_{RMS})	4.5	2.5	2.1	3.29	-	16.8	-
Chip size (mm^2)	0.067	0.65	1.01	0.15	2.25	0.35	0.8
Loop bandwidth (MHz)*	2	0.2	1.15 to 1.7	-	0.06	-	-
f_{ref} (MHz)	-	44.6	-	-	20	-	26
Process	CMOS 45 nm	CMOS 65 nm	CMOS 65 nm	CMOS 180 nm	CMOS 180 nm	CMOS 180 nm	CMOS 130 nm

* Ring-VCO DT-PLL uses on-chip loop filter.

a 45-nm CMOS process also showed an improved spur rejection of about 10 dB compared to a conventional DT-PLL, while dissipating 5.4 mA at a 1.1 V supply.

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Seok-Ju Yun received his BS in electrical and electronic engineering from Kyungpook National University in 1998 and MS and PhD in electrical engineering from Information and Communications University (ICU) in 2005 and 2009, respectively. Since 2009, he has been with ETRI, Daejeon, Rep of Korea, working mainly on the development of analog integrated circuits (ICs). As the senior engineer of the Convergence Components & Materials Research Laboratory, he is currently involved in the development of high-speed, high-performance mixed-signal ICs, including digitally-assisted low-power RFIC, low-jitter PLL/VCO, CMOS sensors, and sensor interface circuits.

Kwi-Dong Kim received his BS and MS on the subject of "N-P-N lateral bipolar transistor modeling" in electrical and electronic engineering from Kyungpook National University, Daegu, Rep. of Korea in 1983 and 1986, respectively. Since 1987, he has been with ETRI, Daejeon, Rep of Korea, working mainly on the development of analog integrated circuits (ICs). As the principle engineer of the Convergence Components & Materials Research Laboratory, he currently is involved in the development of high-speed, high-performance mixed-signal ICs, including amplifiers, low-jitter PLL/VCO, low-voltage ESD I/O, MEMS/sensor AFE, and analog IP evaluation platforms dedicated to the mixed SoC development.

Jong-Kee Kwon received his BS and MS in electronics engineering from Yeungnam University, Gyeongsan, Rep. of Korea, in 1981 and 1983, respectively, and his PhD in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Rep. of Korea, in 2004. Since 1984, he has been with ETRI, Daejeon, Rep. of Korea, working mainly on the development of analog integrated circuits (ICs). As the technical manager of the Convergence Components & Materials Research Laboratory, he is currently involved in the development of high-speed, high-performance mixed-signal ICs, including low-voltage/low-power analog functions, amplifiers, high-speed/high-resolution data converters, PLL/VCO, and analog interfaces for sensor or MEMS systems.