E-Band Wideband MMIC Receiver Using 0.1 μm GaAs pHEMT Process

Bong-Su Kim, Woo-Jin Byun, Min-Soo Kang, and Kwang Seon Kim

In this paper, the implementations of a 0.1 μm gallium arsenide (GaAs) pseudomorphic high electron mobility transistor process for a low noise amplifier (LNA), a subharmonically pumped (SHP) mixer, and a single-chip receiver for 70/80 GHz point-to-point communications are presented. To obtain high-gain performance and good flatness for a 15 GHz (71 GHz to 86 GHz) wideband LNA, a five-stage input/output port transmission line matching method is used. To decrease the package loss and cost, 2nd and 4th SHP mixers were designed. From the measured results, the five-stage LNA shows a gain of 23 dB and a noise figure of 4.5 dB. The 2nd and 4th SHP mixers show conversion losses of 12 dB and 17 dB and input P1dB of –1.5 dBm to 1.5 dBm. Finally, a single-chip receiver based on the 4th SHP mixer shows a gain of 6 dB, a noise figure of 6 dB, and an input P1dB of –21 dBm.

Keywords: E-band, MMIC, LNA, SHP mixer, receiver.

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I. Introduction

Recently, the use of high-speed data services, such as 4G mobile communication, 802.11n wireless LAN, and HDTV, is increasing due to the development of high-capacity content. For wideband multi-gigabit wireless communication [1]-[3], we need to find not only the existing saturated frequency band but also a new wideband frequency. Millimeter-wave, especially wide E-band (60 GHz to 90 GHz), plays an important role in accomplishing this purpose. Recently, South Korea, the USA, Canada, Australia, Europe, and Russia allocated a total of 10 GHz for the E-band spectrum (71 GHz to 76 GHz and 81 GHz to 86 GHz) [4]. For gigabit point-to-point (PtP) communication, it is preferable to use the E-band over the 60 GHz band due to the latter band's short range caused by a high oxygen loss. According to this trend, many commercial PtP link providers have added 1.25 Gbps links using on-off keying/binary phase-shift keying (PSK)/ quadrature PSK modulation methods to the market, and CSIRO has reported a 6 Gbps link test-bed using 8-PSK [5].

To spread 70/80 GHz PtP communication, problems regarding high monolithic microwave integrated circuits (MMICs) cost and package difficulties must first be solved. First, E-band MMICs must use more than three wires to minimize interconnection insertion loss and return loss [6]-[8]. Figure 1 shows the simulation results of S_{21} and S_{11} according to the number of bonding wires. To interconnect each microstrip line, we use gold ball bond with a 25 μm diameter. The total length of the bondwire is 350 μm. As the number of wires increases, the insertion loss and return loss decrease. However, performance is not improved once the number of wires exceeds three.

Most E-band MMICs have a 50 μm × 50 μm small signal

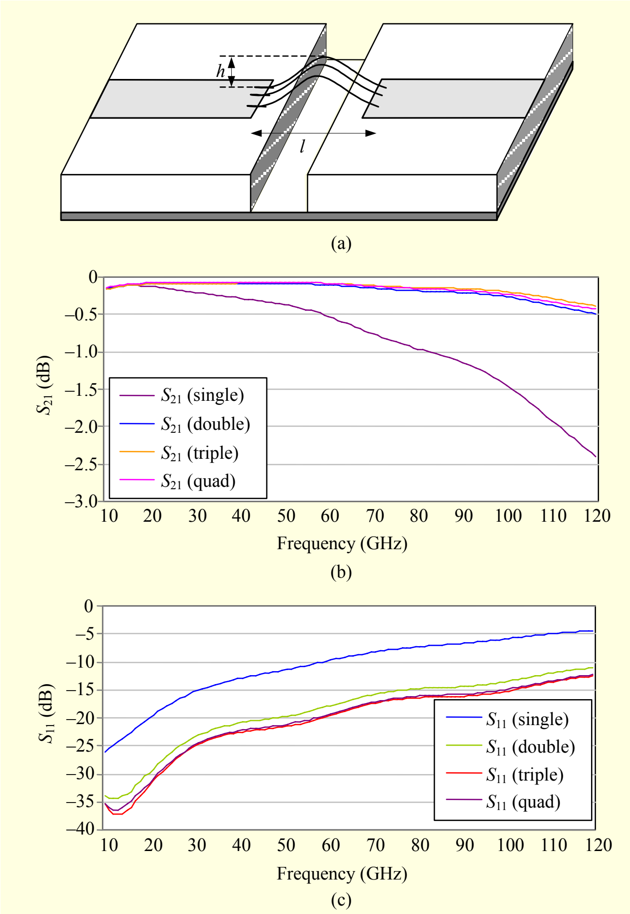

Fig. 1. S_{21} and S_{11} simulation results according to number of bonding wires (simulation parameters: h=0.1 mm, l=0.25 mm, wire diameter=0.025 mm): (a) schematic diagram for bonding wire simulation, (b) simulated results of S_{21}, and (c) simulated results of S_{11}.

pad size. Thus, highly-trained experts need to make the E-band transceiver. To achieve both low cost and easy packaging, a single-chip MMIC receiver without interconnection between chips is proposed in this paper.

Figure 2 shows the receiver structures for a PtP system using the commercial MMICs and the proposed MMICs. For the commercial MMICs shown in Fig. 2(a), two low noise amplifiers (LNAs) with 12 dB gain, a fundamental mixer, a power amplifier (PA) with an output P1dB of more than 18 dBm, and five wirebond interconnections are needed. The PA performs the role of a local oscillator (LO) signal amplifier between the weak LO output signal and mixer. Also, many wirebond interconnections cause performance degradation and price increase. In the proposed MMICs shown in Fig. 2(b), for a single-chip receiver, the LNA with a gain of over 20 dB, the 4th subharmonically pumped (SHP) mixer, and the wirebond interconnection at the input port are needed. The single-chip receiver reduces the chip purchase price, facilitates the package

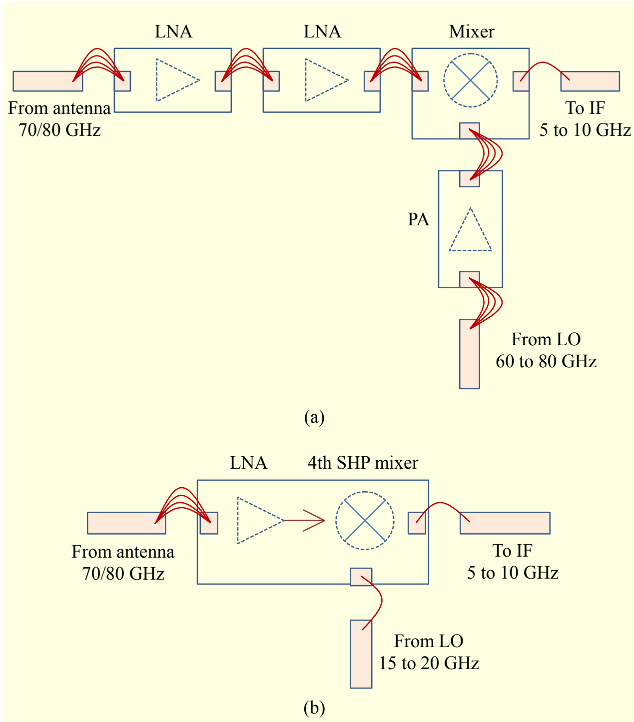

Fig. 2. E-band PtP fixed wireless system: (a) conventional receiver structure and (b) proposed receiver structure.

for high frequency, and improves the performance, such as the noise figure (NF).

II. E-Band MMIC LNA and SHP Mixer

1. High-Gain LNA Design and Fabrication

For 70/80 GHz PtP applications, the LNA has to have good gain flatness, high gain, and a low NF across the 15 GHz band. The LNA and mixers have been designed in a 0.1 µm gallium arsenide (GaAs) pseudomorphic high electron mobility transistor (pHEMT) process with a 50 µm wafer thickness, a cutoff frequency of $f_T \approx 120$ GHz, and a maximum oscillation frequency of $f_{max} > 250$ GHz. The process consists of three metal layers with a 3.5-µm-thick top metal layer for low loss transition lines. The gate-drain breakdown voltage of the transistor BV_{gdr} is typically –6.0 V, and the pinch-off voltage V_{po} is typically –0.6 V [9].

To achieve a high gain of more than 20 dB, a five-stage LNA is designed. In an amplifier with high gain, the amplifier stability worsens. To solve this problem, the resistor insertion method is used at each stage; however, this method can increase the NF of the receiver. Thus, resistor values are chosen to minimize this increase.

Figure 3 shows the maximum stable gain/maximum available gain (MSG/MAG) and F_{min} with 0 Ω, 8 Ω, and 20 Ω

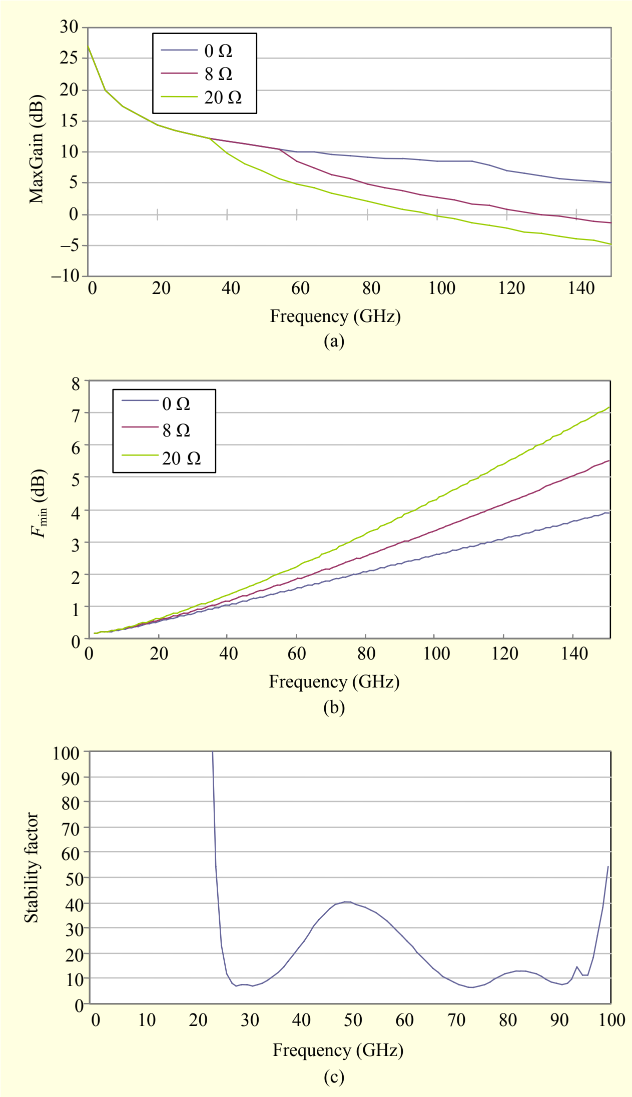

Fig. 3. Transistor design results according to resistor values (transistor parameters: w=60, V_{ds}=2 V, I_d=150 mmA/mm, NF=4): (a) MSG/MAG, (b) F_{min} (the minimum noise factor of the transistor), and (c) simulated results of LNA stability factor.

at the output drain. The MSG/MAG is 1.3 dB, 4.2 dB, and 9.0 dB at 86 GHz, and F_{min} is 3.6 dB, 2.8 dB, and 2.2 dB at 86 GHz. The resistors are chosen for an LNA with a 20 dB gain and a 5 dB NF, based on the above data. The selected resistor values are 8 Ω at the first stage, 8 Ω at the fourth stage, and 20 Ω at the fifth stage. The stability factor of the LNA is more than 6 for the full band (0 GHz to 100 GHz).

To achieve gain flatness for a wideband of 15 GHz (71 GHz to 86 GHz), the lumped element method has difficulty maintaining a constant performance, and the higher the operating frequency, the more influential the chip performance. Studies have shown that the transmission line matching method using EM simulation reaches a wider band

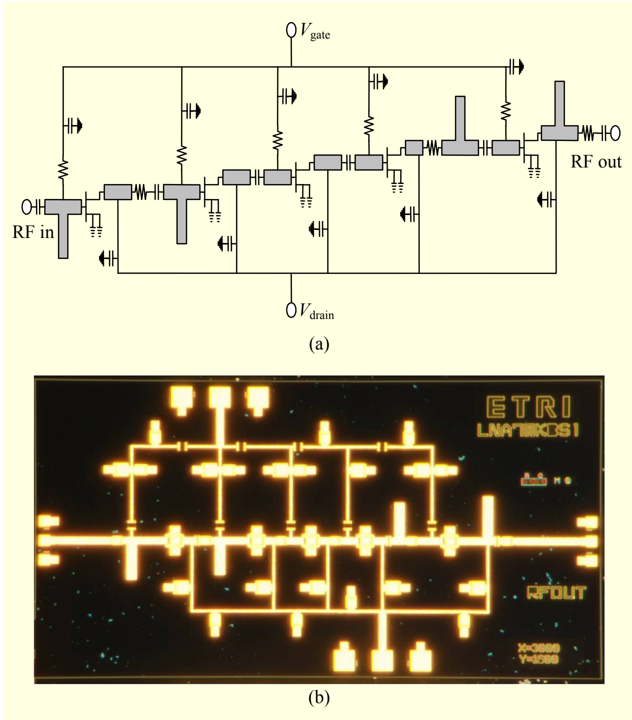

Fig. 4. (a) Final design schematic and (b) photograph of E-band MMIC LNA.

performance [10], [11]. Thus, the transmission line input/output matching method has been chosen in this paper.

Figure 4 shows that the input/output of the transistors are matched by using a T-type transmission line and a photograph of the fabricated LNA. The LNA chip size is 2,950 μm×1,600 μm, and the power consumption is 80 mW (40 mA from 2 V).

The simulated and measured S-parameters of the LNA are shown in Fig. 5. The LNA achieves a small signal gain of more than 23 dB (max. 25 dB), S_{11} and S_{22} of less than –5 dB and –10 dB, respectively, an input P1dB of –18 dBm and –16 dBm at 76 GHz and 86 GHz, respectively, and an NF of less than 4.5 dB. These measurements are found to be in agreement with simulation results.

2. Design and Fabrication of 4th SHP Mixer

The millimeter-wave mixer design is similar to the microwave mixer design. However, as the frequency rises, increasing the LO output power driving the mixer is more difficult than at a low frequency. A commercial mixer (HMC-MDB277) requires an LO module with an 80 GHz band frequency and an output power of more than 14 dBm. The real LO module output power must be more than 17 dBm if 3 dB packaging loss is added. These requirements have zero margin when the output P1dB of a commercial 70/80 GHz PA is 19 dBm to 20 dBm and is an expensive solution.

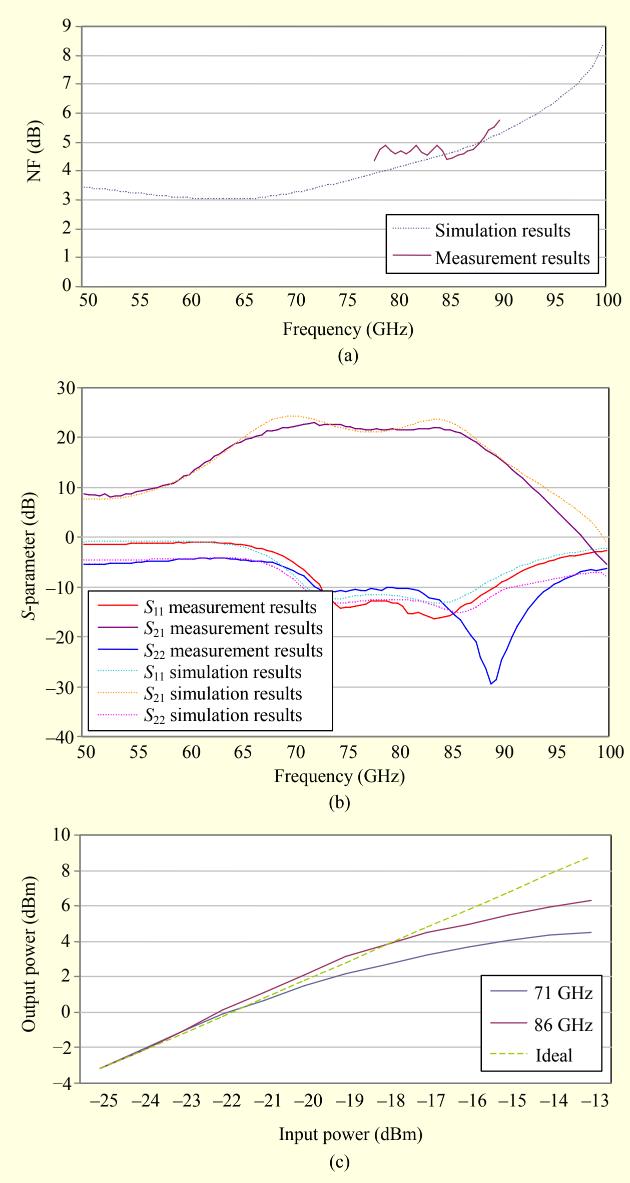

Fig. 5. Simulated (dashed line) and measured (solid line) results of LNA: (a) NF, (b) *S*-parameter, and (c) P1dB.

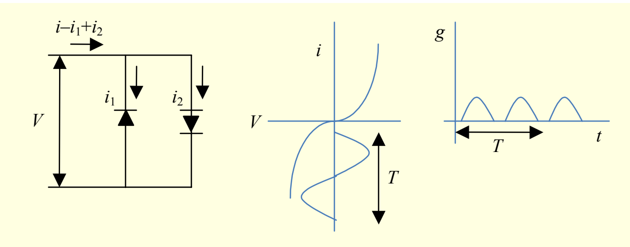

Fig. 6. Schematic of APDP and transconductance variation.

To solve this problem, an SHP mixer using a higher harmonic signal of the input LO signal is designed. To design the SHP mixer, we need a clear understanding of an anti-

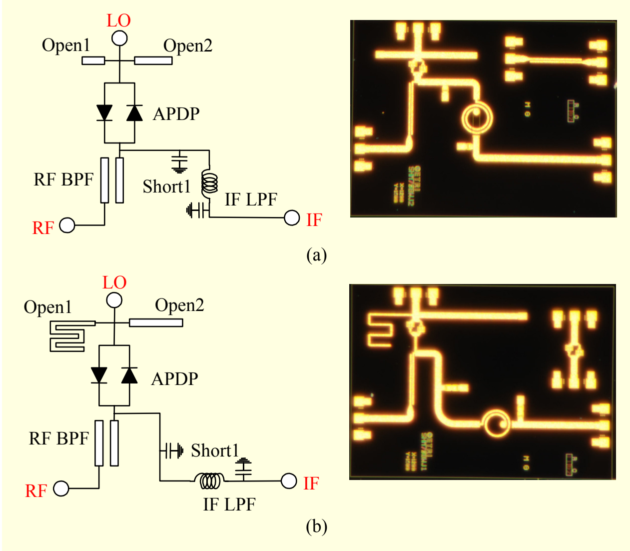

Fig. 7. Schematic and photograph of (a) 2nd and (b) 4th SHP mixers.

parallel diode pair (APDP) structure, as shown in Fig. 6.

Equations (1) through (6) show the fundamentals of the operating APDP structure. First, the total current of the APDP structure is equal to the sum current of each diode, as shown in (1). The nonlinear current of each diode is shown in (2) and (3):

$$i = i_1 + i_2 = g_{\text{total}} V, \tag{1}$$

$$i_1 = -i_s (e^{-\alpha} V - 1), \tag{2}$$

$$i_2 = -i_s (e^{\alpha} V - 1), \tag{3}$$

where α is the diode slope parameter and i_s is the diode saturation current. The total transconductance can be described through (4).

$$\begin{aligned} g_{\text{total}} &= g_1 + g_2 = di_1/dV + di_2/dV \\ &= \alpha i_s (e^{\alpha V} + e^{-\alpha V}) = 2\alpha i_s \cos h(\alpha V), \end{aligned} \tag{4}$$

where V=$V_{\text{LO}}\cos(\omega_{\text{LO}}t)$+$V_{\text{RF}}\cos(\omega_{\text{RF}}t)$. If $V_{\text{LO}} \gg V_{\text{RF}}$, (4) can be expressed as a transconductance form of (5) using only the LO term.

$$\begin{aligned} g_{\text{total}} &= 2\alpha i_s [I_o(\alpha V_{\text{LO}}) + 2I_2(\alpha V_{\text{LO}})\cos(2\omega_{\text{LO}}t)] \\ &\quad + \cdots + 2I_n(\alpha V_{\text{LO}})\cos(n\omega_{\text{LO}}t) + \cdots), \end{aligned} \tag{5}$$

where $I_n(\alpha V_{\text{LO}})$ is the 2nd modified Bessel function and n is an even integer. As the output current expression,

$$\begin{aligned} I &= g_{\text{total}}[V_{\text{LO}}\cos(\omega_{\text{LO}}t) + V_{\text{RF}}\cos(\omega_{\text{RF}}t)] \\ &= A\cos(\omega_{\text{LO}}t) + B\cos(\omega_{\text{RF}}t) + C\cos(3\omega_{\text{LO}}t) \\ &\quad + D\cos(5\omega_{\text{LO}}t) + E\cos((\omega_{\text{RF}} + 2\omega_{\text{LO}})t) \\ &\quad + F\cos((\omega_{\text{RF}} - 2\omega_{\text{LO}})t) + G\cos((\omega_{\text{RF}} - 4\omega_{\text{LO}})t) \\ &\quad + H\cos((\omega_{\text{RF}} - 4\omega_{\text{LO}})t) + \cdots. \end{aligned} \tag{6}$$

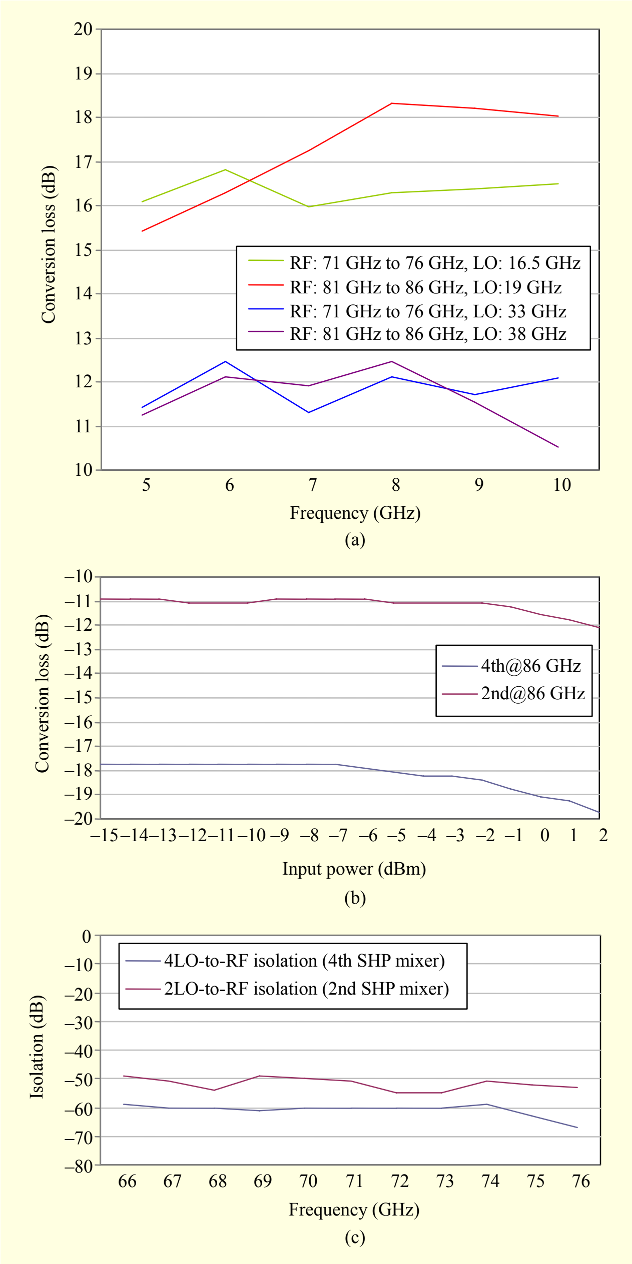

Fig. 8. Conversion loss and nonlinearity results for 2nd /4th SHP mixer: (a) conversion loss, (b) input power vs. conversion loss measurements, and (c) LO-to-RF isolation measurements.

As seen in (6), the APDP output current has a signal at only the ($m\omega_{RF}\pm n\omega_{LO}$) frequency, where ($m+n$) is an odd integer, and we design mixers using the 2nd and 4th harmonic LO signals [12].

A mixer using even harmonics to pump the LO signal of the mixer is called an even harmonic mixer and, with a relatively low LO frequency, has an advantage in obtaining high output power and low phase noise. For example, the output P1dB of a commercial 40 GHz PA (HMC-APH473) is 28 dBm, but an 80 GHz PA (HMC-APH634) has about 19 dBm. Also, as the oscillator frequency doubles, the phase noise of the oscillator increases by 6 dB, and, typically, the lower the oscillator frequency, the better the phase noise. This effect must be considered in the total system design.

Figure 7 shows schematics and photographs of the 2nd/4th SHP mixers. The bandpass filter (BPF) at the radio frequency (RF) port rejects LO harmonics and the intermediate frequency (IF) signal, and the low-pass filter (LPF) at the IF port rejects the $1/n$ LO frequency and all mixed frequencies except the IF. In addition, two open stubs and one short stub are used to cut an unwanted signal by forming a single pole at the specific frequency.

The LO frequency of the 2nd/4th SHP mixer is 33/16.5 GHz at 70 GHz and 38/19 GHz at 80 GHz, and the LO input power is 12 dBm (2nd) and 17 dBm (4th). Figure 8 shows the conversion loss, nonlinearity at 86 GHz, and LO isolation. The conversion loss of the 2nd/4th SHP mixer is observed as 11 dB to 13/16 dB to 18 dB, and the conversion loss of the 6th SHP mixer in a similar structure is 26 dB [13]. We can predict that the conversion loss increases by about 6 dB as the order of the SHP mixer doubles. In addition, the input P1dB of the 2nd/4th SHP mixer is measured as 1/0 dBm at 86 GHz. The 4LO-to-RF isolation of the 4th SHP mixer is better than the 2LO-to-RF isolation of the 2nd SHP mixer at about 10 dB.

III. E-Band MMIC Single-Chip Receiver

An E-band single-chip receiver is implemented by connecting the aforementioned high-gain LNA and the 4th SHP mixer. Figure 9 shows a probe station test setup for the MMIC single-chip receiver measurement and a photograph of the single-chip receiver with fine tuning added to match the impedance between the LNA and the mixer.

The total size of the receiver chip is 3,800 µm×1,800 µm, and the power consumption is 80 mW (40 mA from 2 V).

As shown in Fig. 10, the fabricated E-band receiver achieves a conversion gain (CG) of more than 6 dB, a good gain flatness of about 2 dB, and an input P1dB at 86 GHz of –21 dBm. Here, the input P1dB of the receiver depends on the mixer, and the input P1dB of the receiver can be increased if the LNA has low gain. Also, the simulated receiver NF based on the measured LNA NF is less than 6 dB.

Table 1 shows a summary of the properties of millimeter-wave MMIC receivers: frequency, bandwidth (BW), gate length, NF, LO harmonic order, CG, and LO driving power. The gate lengths of the HEMT devices are also included. The 77 GHz receiver developed at TriQuint shows a low LO driving power, the 60 GHz receivers of DERA have a high CG, the 60 GHz transceiver of National Taiwan University shows

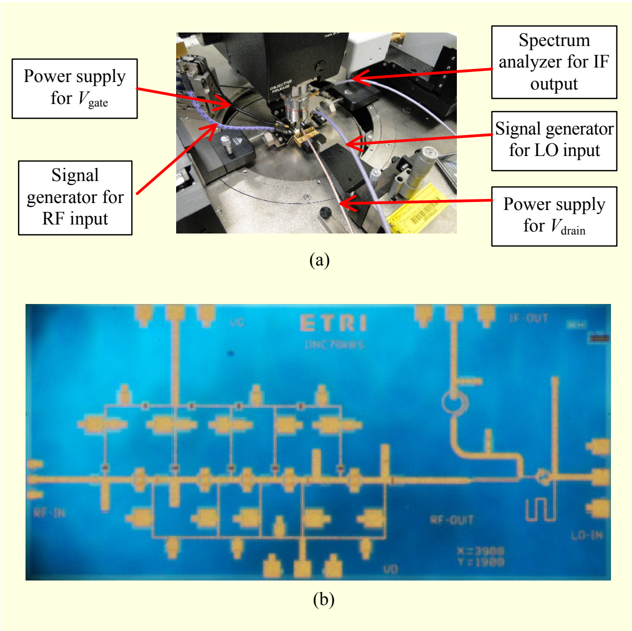

Fig. 9. Test setup and photograph of MMIC single-chip receiver: (a) probe station test setup and (b) chip photo of receiver.

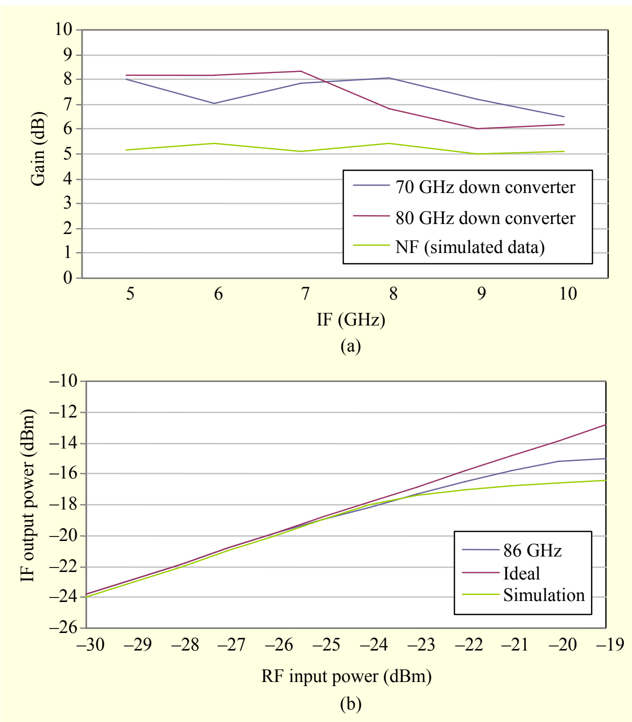

Fig. 10. (a) CG and (b) input power vs. IF output power measurements for E-band single-chip receiver.

poor gain flatness, and the 53 GHz commercial receiver of Gotmic shows low NF [14]-[17]. Finally, this work has a relatively high gain and good gain flatness for the widest BW.

These results show that our design approach is effective for millimeter-wave MMIC single-chip receivers.

Table 1. Comparison of MMICs receiver performances.

	[14]	[15]	[16]	[17]	This work
Frequency (GHz)	77	60	60	53	70/80
BW (GHz)	< 3	9	12	9	15
Gate length (μm)	0.15	0.15	0.15	-	0.1
NF (dB)	4 (only LNA)	5.8	-	4	<6 (sim.)
LO order	2nd	2nd	4th	2nd	4th
CG (dB)	–3 to –1	8 to 11.5	0 to 8	5 to 13	6 to 8.2
LO power (dBm)	10	–5 (with LO amp.)	19	5	17

IV. Conclusion

An E-band MMIC single-chip receiver using a 0.1 μm pHEMT process was presented. From the measured results, the five-stage LNA shows a gain of 23 dB and an NF of 4.5 dB. The SHP mixer shows a 4th conversion loss of 17 dB and an input P1dB of –1.5 dBm to 1.5 dBm. Finally, the single-chip receiver based on the 4th SHP mixer shows good results with a gain of 6 dB to 8.2 dB, an NF of less than 6 dB (simulation), and an input P1dB of –21 dBm.

The advantages of using this work for an E-band receiver are lower production cost, convenience for millimeter-wave packages, and performance improvement by decreasing the interconnection loss. We are hoping that a future study on the on-chip transition between the microstrip line and rectangular waveguide will allow us to remove the last millimeter-wave bondwire at the LNA input port.

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