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Design of an FPGA Based Controller for Delta Modulated Single-Phase Matrix Converters

Anshul Agarwal* and Vineeta Agarwal†

*Dept. of Electrical Engineering, National Institute of Technology, Hamirpur, Himachal Pradesh, India
†Dept. of Electrical Engineering, Motilal Nehru National Institute of Technology, Uttar Pradesh, India

Abstract

A FPGA based delta modulated single phase matrix converter has been developed that may be used in both cyclo-converters and cyclo-inverters. This converter is ideal for variable speed electrical drives, induction heating, fluorescent lighting, ballasts and high frequency power supplies. The peripheral input-output and FPGA interfacing have been developed through Xilinx 9.2i, to generate delta modulated trigger pulses for the converter. The controller has been relieved of the time consuming computational task of PWM signal generation by implementing the method of trigger pulse generation in a FPGA by using Hardware Description Language VHDL in Xilinx. The trigger circuit has been tested qualitatively by observing various waveforms on an oscilloscope. The operation of the proposed system has been found to be satisfactory.

Key words: Cyclo-Converter, Cyclo-Inverter, Field Programmable Gate Array (FPGA), Matrix Converter, Very High Speed Integrated Circuits Hardware Description Language (VHDL)

I. INTRODUCTION

The operation and maintenance of converters requires the development of expertise and hence costly labor [1]. The use of a matrix converter reduces the need for learning many varying converter topologies which is one of the reasons that this is now the subject of current active research [2]. Fully controlled frequency changers based on cyclo-converter arrangement have a topology that is similar to those of single-phase matrix converters [3]. The matrix converter (MC) is an advanced circuit topology that offers many advantages such as the ability to regenerate energy back to the utility, sinusoidal input and output currents and a controllable input current displacement factor [4]. It has the potential for affording an "all silicon" solution for AC-AC conversion and for removing the need for the reactive energy storage components used in conventional rectifier-inverter based systems [5].

This paper proposes a single-phase matrix converter (SPMC) that has been used to perform the functions of a generalized frequency converter capable of operating both as a cyclo-converter and as a cyclo-inverter. A cyclo-converter converts ac input power at one frequency to ac output power at a lower frequency whereas a cyclo-inverter converts ac input power at one frequency to ac output power at a higher frequency. This matrix converter finds application in the speed control of electrical drives, induction heating, fluorescent lighting, ballasts and high frequency power supplies [6], [7].

However, the output of the matrix converter is rich in harmonics [8]. Various modulation techniques employed to improve the quality of the output voltage of matrix converters include sinusoidal PWM [9], space vector PWM [10], [11] and delta modulation [12], [13]. Delta modulation offers a number of advantages such as a simple electronic circuitry without external feedback from a high power circuit, inherent constant volts per hertz control for a preset frequency range, smooth transitions between the constant volt per hertz and the constant volts modes of operation, severe attenuation of the low order harmonics, low communication rates for high modulation signals and guaranteed on/off time for the switches [14]. Microcontroller devices [15] or digital signal processors (DSPs) may be used to implement the delta modulation technique. However, microprocessor-based techniques have the disadvantages of a complex circuitry, limited functions, and difficulty in circuit modification. Digital PWM control with a DSP has the advantages [16] of a simple circuitry, software

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†Corresponding Author: vineeta@mnnit.ac.in
Tel: +91-9838075072, Fax: +915322540581, MNNIT Allahabad
*Dept. of Electrical Engineering, National Institute of Technology, India

control, and flexibility in adaptation to various applications. However, generating PWM gating signals and current control loops requires a high sampling rate to achieve wide bandwidth performance [17].

In recent years, the development of application-specific integrated circuit (ASIC) technology has made it possible to integrate complex analog and digital circuits by utilizing the libraries of basic circuit cells [18]. With the advancement of various technical aspects of ASIC, three major categories have been developed: cell based integrated circuits (CBIC), gate arrays, and programmable logic devices (PLD) [19]. The field-programmable gate array (FPGA) is a new PLD developed by Xilinx, Inc. [20]. The FPGA comprises thousands of logic gates, some of which are grouped together as a configurable logic block (CLB) to simplify the higher-level circuit design. The simplicity and programmability of the FPGA [21] designate it as the most favorable choice for prototyping an ASIC.

When compared with conventional schemes, the advantages of the FPGA include three aspects. First of all, the FPGA IO resource is abundant [22]. Secondly, the real time control needs faster digital circuits than before, and the performance of the FPGA to the design sequential logic circuits is good [23]. Lastly, the development environment of the FPGA is easy to use. The difficulty and time cost for the hardware design have been greatly reduced [24]. With the FPGA implementation of the delta modulation process, the information is faster and the controller architecture can be optimized for space or speed and it is available in radiation tolerant package [25].

II. PRINCIPLE OF OPERATION

Fig. 1(a) shows a single phase matrix converter used as a generalized frequency converter. It consists of four bi-directional switches capable of blocking voltage and conducting current in both directions. In the absence of a bidirectional switch module, a common emitter anti-parallel IGBT with a diode pair, as shown in Fig. 1(b), is used. The diodes provide reverse blocking capability to the switch module. The IGBT was used due to its high switching capabilities and high current carrying capacities, which are desirable for high-power applications. The output can be obtained through proper conduction of the switches in two input cycles. For example, say for the cyclo-converter operation, if the output frequency is half of the input frequency then in the positive input cycle for positive output, switches S1a and S4a will conduct while for the negative input cycle if the output is positive, switches S3b and S2b will conduct (Fig. 2 (a)). The negative half output of the cyclo-converter will be obtained by the conduction of switches S2a and S3a and switches S4b and S1b as shown in Fig. 2 (b). The operation of the cyclo-inverter can be explained in a similar manner. However, the outputs of both the cyclo-inverter and the

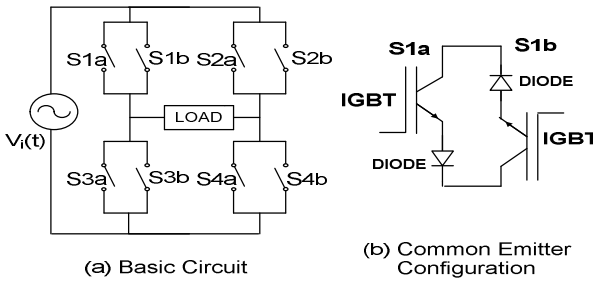
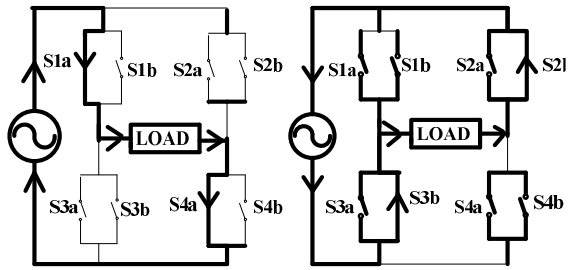
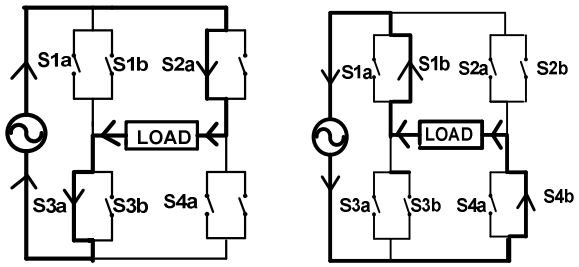


Fig. 1. Single phase matrix converter.



(a) For positive output.



(b) For negative output.

Fig. 2. Cyclo-converter operation.

cyclo-converter are very far from sinusoidal and contain a large number of harmonics. This is reduced by applying the delta modulation technique and implementing it on the FPGA.

III. DELTA MODULATION TECHNIQUE

Delta modulation, consisting of a forward comparator and a feedback filter, utilizes a sine reference wave V_R and a delta shaped carrier wave V_F as shown in Fig. 3. The carrier wave V_F is allowed to oscillate within a defined window extending equally above and below the reference wave V_R.

The reference signal V_R is compared with a carrier signal V_F obtained by integrating the comparator output signal to produce an error signal, e. The error signal, e, is quantized into one of two possible levels $\pm E$ depending on its polarity, whereas the slope of the reference signal determines the time duration

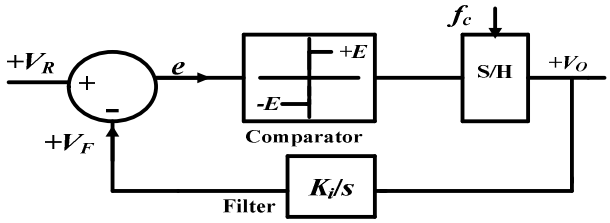


Fig. 3. Block diagram of delta modulator.

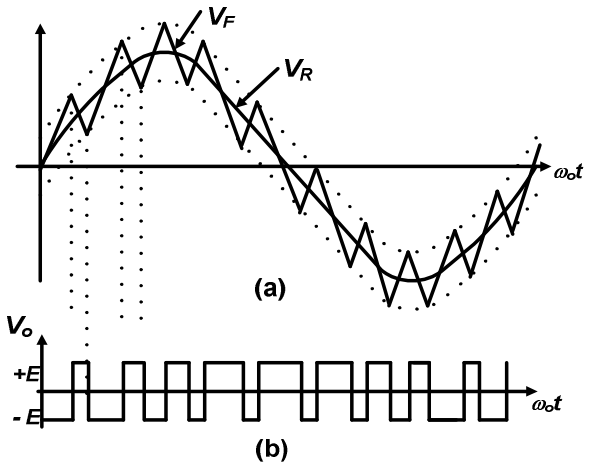


Fig. 4. Delta modulation technique. (a) Reference signal and carrier signal. (b) Delta modulated switching functions.

between two successive levels. The comparator output is regularly sampled by the signal f_c to produce the output binary pulses. Fig. 4(a) and 4(b) show the waveforms at various nodes in the modulator block diagram.

The closed loop arrangement of the modulator ensures that the integrated output faithfully tracks the reference signal within the upper and lower boundary levels. However, it is important to note that as V_R increases in frequency, the component of V_o at that frequency also increases in amplitude. Thus the amplitude transfer characteristic of the linear delta modulator demonstrates strong frequency dependence [26], which is often undesirable in power electronic applications where the demodulator, most frequently, is a simple low pass filter. Further examination of the operation of the linear delta modulator shows that in order to ensure that the feedback signal, V_F, tracks the reference, a slope overload condition must be satisfied. This requires that dV_R/dt should never exceed the maximum rate for the change of V_F. Let:

$$V_R = V_s \sin(\omega_o t) \tag{1}$$

$$\left[\frac{dV_R}{dt}\right]_{\max} = V_s \omega_o \tag{2}$$

$$\left[\frac{dV_F}{dt}\right]_{\max} = K_i V_o \tag{3}$$

where ω_o is the reference signal radian frequency, K_i is the integrator gain and V_o is the output switching level. From (2) and (3):

$$V_s \omega_o \le K_i V_o \tag{4}$$

From (4) it follows that a linear delta modulator cannot encode a high frequency sinusoidal signal without running into a slope overload condition, unless the input amplitude is restricted.

This interdependence of the amplitude and frequency of the reference signal in the slope overload condition can be eliminated [27] by integrating the reference as shown in Fig. 5. For V_F to track V_R, the maximum slope of $V_R \le$ maximum slope of V_F. Now:

$$V_R = K_i \int V_i dt = K_i \int V_s \sin(\omega_o t) dt = -\frac{K_i V_s}{\omega_o} Cos(\omega_o t) \tag{5}$$

Hence, from the slope overload condition:

$$V_s \le V_c \tag{6}$$

The slope overload condition is now independent of the reference frequency and the amplitude transfer gain is seen to be unity, which are very desirable attributes [28]. The same objective can be achieved by replacing the two integrators in Fig. 5 with one integrator placed after the summing junction. This leads to a unity feedback system with the integrator [29] in the forward path as shown in Fig. 6.

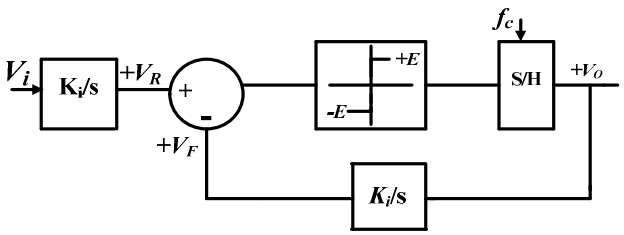


Fig. 5. Delta modulator with integrator at input.

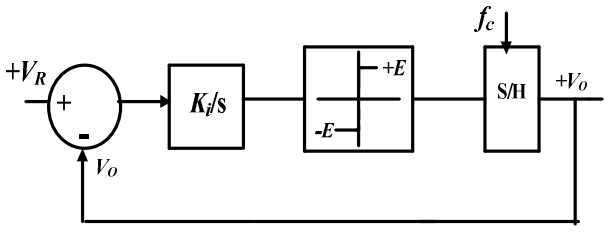


Fig. 6. Block diagram of sigma delta modulator.

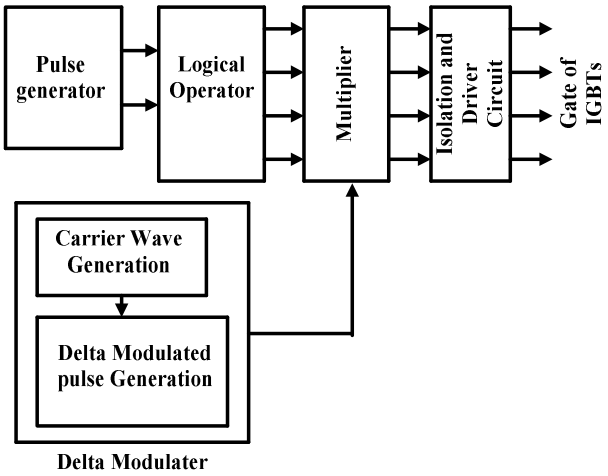


Fig. 7. Block diagram to generate the triggering pulses.

The integrator position results in substantially zero steady state error for any reference with a frequency that is much smaller than the sampling frequency, f_c. This delta modulation scheme is popularly known as sigma delta modulation [30]. For a single phase cyclo-inverter a sine wave having the desired output frequency, is the input to the modulator.

IV. Trigger Pulse Generation on a FPGA

Fig. 7 shows a block diagram to generate the delta modulated trigger signals for the proposed matrix converter. First, three basic signals X1 (at 50 Hz), X2 (at 50 × N_r Hz) and X3 (at 50/N_r Hz) are generated in the pulse generator block. Trigger signals are then generated in the logical operator block with the help of these basic signals. In the delta modulator block the delta modulated signal is generated by comparing a triangular carrier wave with the delta modulated sine reference wave. The output of the delta modulator block and the logical operator block are multiplied in the multiplier block and fed to the gates the IGBTs of the matrix converter through the isolation and driver circuits. A detail description of each block is illustrated in the following subsections.

A. Basic Signal Generation

In order to generate the basic signals on a FPGA, a Spartan-3E FPGA kit is used whose internal main clock frequency is 50 MHz. To get signal X1 at 50 Hz, from the input clock of 50 MHz, 500000 clocks are counted and then the output pulse is reset. Counting the same number of clocks again the output wave is set. This gives the desired frequency output. The formula used in the code is:

$$f_{out} = f_{clk} / 2N \tag{7}$$

where f_{out} = Desired output frequency pulse.
f_{clk} = Main clock of the FPGA.
N = No. of clocks to be counted.

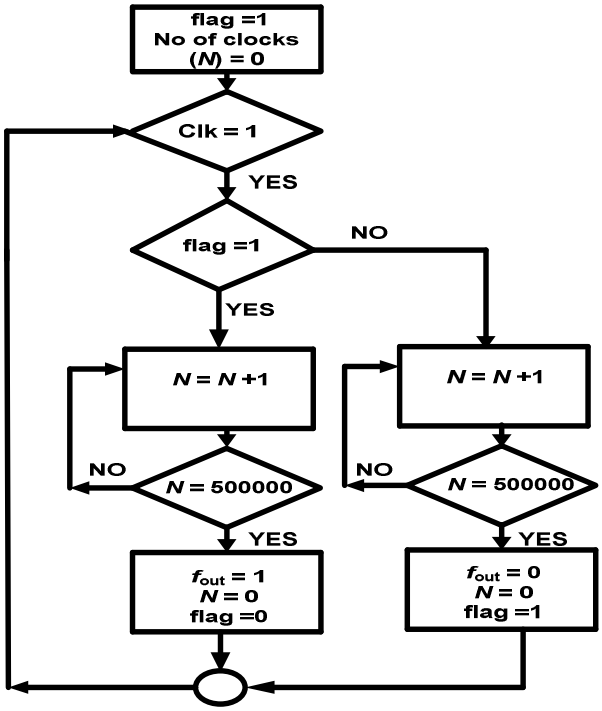


Fig. 8. Flowchart for 50 Hz signal generation.

A flowchart for the generation of the 50 Hz signal is shown in Fig. 8. In this flow chart the flag is taken as a Boolean variable which is initially one and becomes zero after counting 500000 pulses. The signals X2 and X3 at a desired output frequency may be generated in a similar manner. Once these basic signals are generated, the logical operation is performed on these signals according to Table 1. Thus the required trigger signals for either converter operation are obtained. Fig. 9 shows the basic signals and the trigger signals for the cyclo-inverter operation at an output frequency of 250 Hz.

B. Carrier Wave Generation

To generate a triangular carrier waveform, one n-bit counter is used. This counter moves up or down depending on the flag value "Temp". If Temp is set, the counter counts in the upward direction; otherwise it counts in the downward direction. In this paper a 4 bit up/down counter is used that generates an 'M' shape triangular waveform as shown in Fig. 10.

The counter value is digitally incremented from 0 to 15 and then subsequently decremented back to 0 over a period of time. Good accuracy requires high bit number.

The frequency of the carrier triangular wave, f_c, is related to the main clock frequency by (8):

$$f_c = f_{clk} /(2^n - 1)\times 2 \tag{8}$$

where f_c is the carrier wave frequencies and n is the bit size of the up-down counter. The flow chart shown in Fig. 11 illustrates the procedure for the generation of a carrier wave on a FPGA.

TABLE I
LOGICAL EXPRESSION OF TRIGGERING PULSE FOR TWO CONVERTER OPERATION

Converter	(Conducting Switches)	Logical Operation
Cyclo-Inverter	S1a, S4a	X2. X1
	S2a, S3a	X2'. X1
	S2b, S3b	X1'. X2
	S1b, S4b	X1'. X2'
Cyclo-Converter	S1a, S4a	X1. X3
	S2b, S3b	X1'. X3
	S2a, S3a	X1. X3'
	S1b, S4b	X1'. X3'

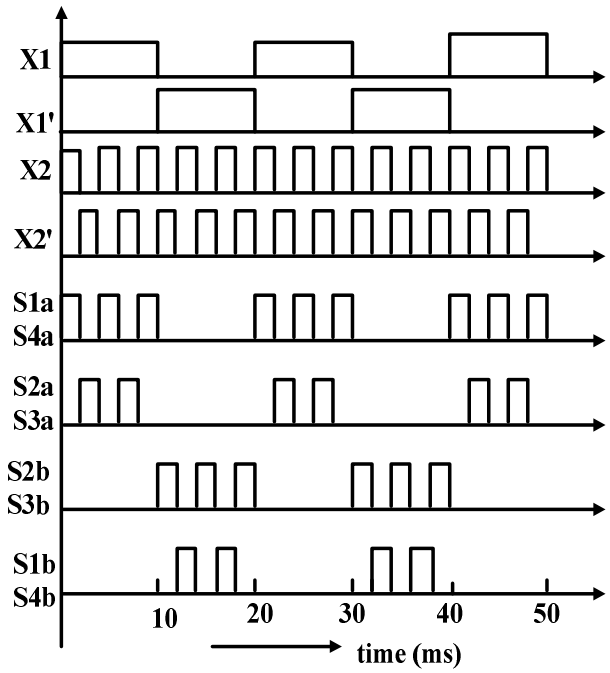


Fig. 9. Basic signals and trigger signals for cyclo-inverter operation.

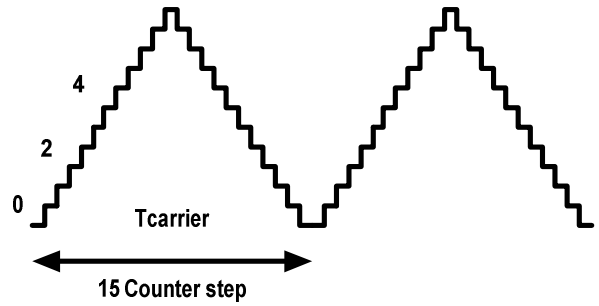


Fig. 10. Digitized triangular carrier waveform.

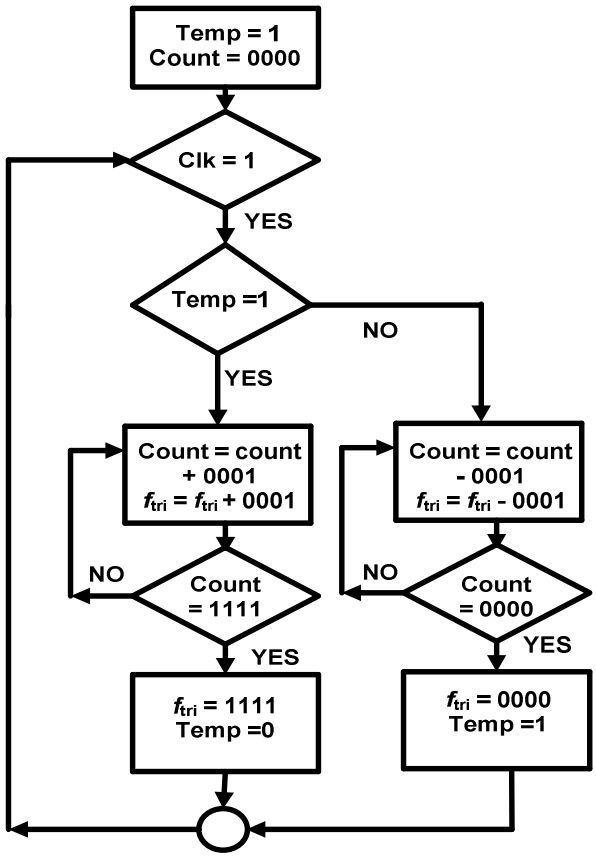


Fig. 11. Flowchart for triangular waveform.

C. Delta Modulated Signal Generation

A standard delta modulating signal is generated by using the look-up table technique. Samples of the sinusoidal reference wave are stored at sequential addresses in the ROM in look-up table form. A binary counter which acts as a memory counter then addressees the ROM and the sinusoidal samples are updated by clocking the counter as shown in Fig. 12. The modulating signals are generated by comparing the scaled sinusoidal signals from the look up table with a triangular wave generated from the up/down counter within the hysteresis band.

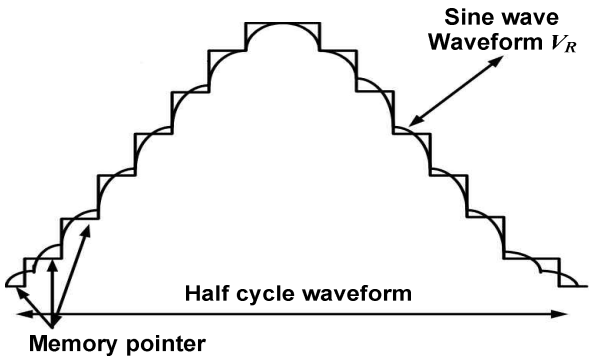


Fig. 12. Sine wave value at different memory location.

The comparator compares the up/down counter signal which is a triangular carrier wave with the ROM data output which generates a sinusoidal signal. The comparison is done for every clock pulse in every counting step for the carrier value as well as for the ROM data value. This process is continuous and repeats every 10 ms. In order to have a different modulation index the data from the look-up table i.e. the maximum values stored for the sinusoidal wave are modified. This is achieved simply by changing the maximum number of steps in the triangular waveform i.e. by modifying the number of counts in the up/down counter the modulation index can be changed.

The generated delta modulated pulse is then multiplied by the four switching pulses obtained in Fig. 9 to get the required delta modulated trigger signals. These signals are finally fed to the gates of the IGBTs of the matrix converter with the help of connector pins.

V. EXPERIMENTAL RESULTS

The principle of delta modulation is implemented on a FPGA using Xilinx. Fig. 13 shows a photograph of the experimental set-up. It consists of a Spartan-3E FPGA kit and eight IRG4PH40UD IGBTs, with an ultra fast soft recovery diode, a driver circuit and an opto coupler for isolation. A variable resistance-inductance is used as a load. The logical gating signals for a particular value of N_r are generated by VHDL programming in Xilinx ISE-9.2i. The resulting coding is then downloaded to the Spartan-3E FPGA kit. The experimental results are shown by interfacing DSO with the Spartan-3E.

Fig. 14 shows the signals X1 (50 Hz) and X2 (250 Hz) for the cyclo-inverter operation while Fig. 15 shows the signals X1 (50 Hz) and X3 (10 Hz) for the cyclo-converter operation. The triangular carrier wave at a frequency of 2 kHz is shown in Fig. 16. The switching pulses for an output frequency of 250 Hz and 10 Hz at a carrier frequency of 2 kHz are shown in Fig. 17 and Fig. 18, respectively. Fig. 19 shows the output voltage for an output frequency of 250 Hz for the RL load for a carrier frequency of 2 kHz. The output is almost symmetrical about the x axis. Fig. 20 shows the output voltage for an output frequency of 25 Hz at a carrier frequency of 2 kHz. Some spikes are observed in the voltage waveform because of the presence of an inductance in the load. These spikes are more persistent in case of a low frequency as shown in Fig. 20. Thus the output voltage becomes slightly distorted. The converter has been tested in the output frequency range of 1 Hz to 10 kHz but it can work for other frequencies by taking a high bit up/down counter.

Fig. 13. Power circuit of experimental setup.

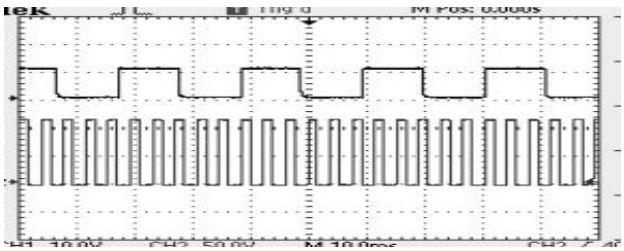


Fig. 14. Signal X1 (top trace: 5 V/div, 10 ms/div) at 50 Hz and signal X2 (bottom trace: 2.5 V/div, 10 ms/div) at 250 Hz.

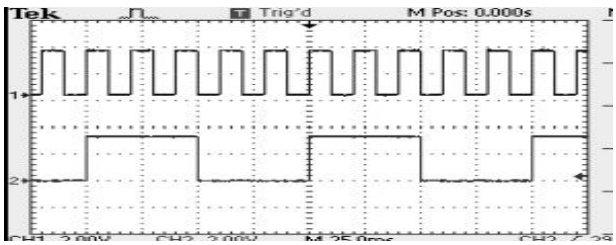


Fig. 15. Signal X1at 50 Hz (top trace: 2.5 V/div, 5 ms/div) and signal X3 (bottom trace: 2.5 V/div, 5 ms/div) at 10 Hz.

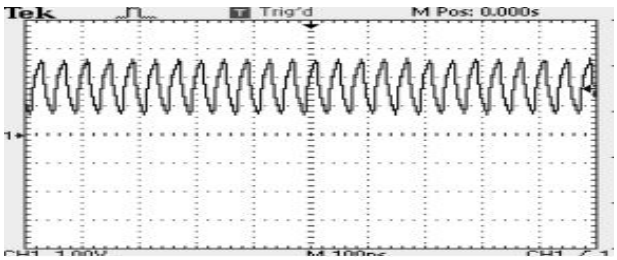


Fig. 16. Triangular wave generation (2.5 V/div, 10 ms/div) at frequency of 2 kHz.

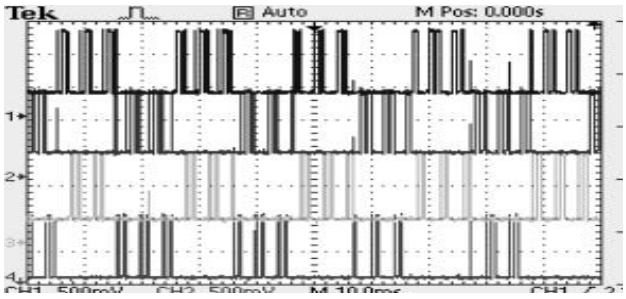


Fig. 17. Switching pulses (all trace: 2.5 V/div, 10 ms/div) at f_o = 250 Hz.

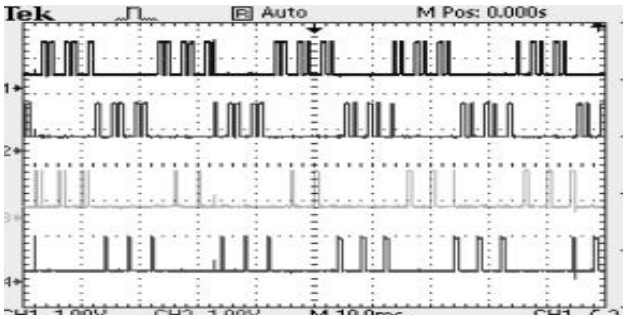


Fig. 18. Switching pulses (all trace: 5 V/div, 5 ms/div) at f_o = 10 Hz

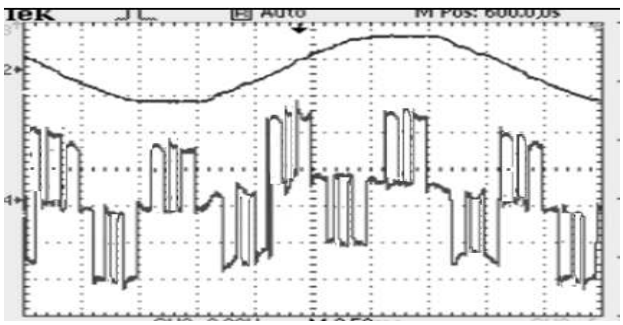


Fig. 19. Input voltage (upper trace: 100 V/div, 2 ms/div) & output voltage (lower trace: 50 V/div, 2 ms/div) of matrix converter in cyclo-inverter mode at f_o = 250 Hz.

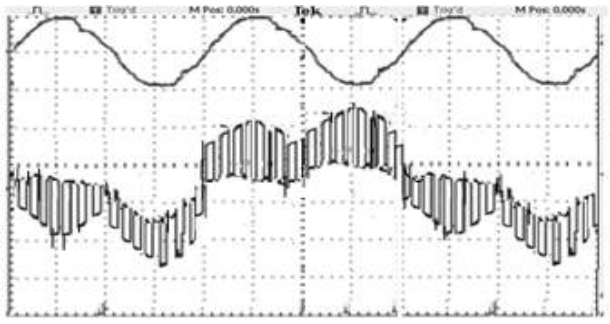


Fig. 20. Input voltage (upper trace: 50 V/div, 5 ms/div) & output voltage (lower trace: 50 V/div, 5 ms/div) of matrix converter in cyclo-converter mode at f_o = 25 Hz.

VI. CONCLUSIONS

A novel IGBT based matrix converter has been proposed on the web pack software of Xilinx 9.2i. The delta modulation technique is applied in the converter in order to improve its output. The technique is implemented on a FPGA Spartan-3E kit. Experimental results are shown by interfacing a digital storage oscilloscope with the Spartan-3E. The obtained switching pulses are applied to the power circuit of the matrix converter to obtain the required output voltage waveforms for the cyclo-inverter and cyclo-converter operations. The converter has been tested from 1 Hz to 10 kHz and the operation of the circuit has been found to be satisfactory.

REFERENCES

[1] Bin Wu Pontt, J. Rodriguez, S. Bernet, and S. Kouro "Current-source converter and cycloconverter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 7, pp. 2786-2797, Jul. 2008.

[2] R. K. Gupta, K. K Mohapatra, and A. Somani and N. Mohan, "Direct-matrix-converter-based drive for a three-phase open-end-winding ac machine with advanced features," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 12, pp. 4032-4042, Dec. 2010.

[3] P. W. Wheeler, J. Rodriguez, J.C. Clare, L. Empringham, and A. Weinstein, "Matrix converters: a technology review," *IEEE Trans. Ind. Electron.*, Vol. 49, No. 2, pp. 276-288, Apr. 2002.

[4] M. K. Hamzah, Z. Idris, A. Saparon, and M. S. Yunos, "FPGA design of single-phase matrix converter operating as a frequency changer," *in Proc. PECon,* pp. 1124-1129, 2008.

[5] S. Vazquez, J. I. Leon, L. G. Franquelo, J. J. Padilla, and J. M. Carrasco, "DC-voltage-ratio control strategy for multilevel cascaded converters fed with a single DC source," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 7, pp. 2513-2521, Jul. 2009.

[6] R. Orletti, M. A. Co, D. S. L. Simonetti, and J. L. F. Vieira, "HID lamp electronic ballast with reduced component number," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 3, pp. 718-725, Mar. 2009.

[7] V. Agrawal, A. K. Agarwal, and K. Kant, "A study of single phase to three phase cyclo-converter using PSPICE," *IEEE Trans. Ind. Electron.*, Vol. 39, No. 2, pp 141-148, Apr. 1992.

[8] A. Agarwal and V. Agarwal, "Design of delta modulated generalized frequency converter," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 11, pp. 3924-3729, Nov. 2010.

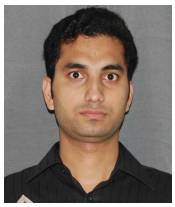
[9] D. Yonggui and X. Keming, "The SPWM inversion mode of suppressing harmonic waves based on genetic algorithm," in *Proc. ICEMS* , pp. 1304-1307, 2001.

[10] A. Mehrizi-Sani and S. Filizadeh, "An optimized space vector modulation sequence for improved harmonic performance," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 8, pp. 2894-2903, Aug. 2009.

[11] G. Narayanan, V. T. Ranganathan, D. Zhao, H. K. Krishnamurthy, and R. Ayyanar, "Space vector based hybrid PWM techniques for reduced current ripple," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 4, pp. 1614-1627, Apr. 2008.

[12] M. A. Rahman, J. E. Quaicoe, and M. A. Choudhury,

"Performance Analysis of delta PWM inverters," *IEEE Trans. Power Electron.*, Vol. PE-2, No. 3, pp. 227-233, Jul. 1987.
[13] A. Agarwal and V. Agarwal, "Delta modulated cyclo-inverters," in *Proc. INTELEC,* pp. 1-6, 2008.
[14] Y. M. Chen, Y. C. Chen, and T. F. Wu, "Feed forward Delta Modulation for Power Converters," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 12, pp. 4126-4136, Dec. 2010.
[15] S. R. Bowes and M. J. Mount, "Microprocessor control of PWM inverters," *IEE Proceedings B Electric Power Applications*, Vol. 128, No. 6, pp. 293-305, Nov. 1981.
[16] B. Kedjar and K. Al-Haddad, "DSP-based implementation of an LQR with integral action for a three-phase three-wire shunt active power filter," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 8, pp. 2821-2828, Aug. 2009.
[17] Y.-Y. Tzou, M.-F. Tsai, Y.-F. Lin, and H. Wu, "Dual-DSP fully digital control of an induction motor," in *Proc ISIE*, pp. 673-678, 1996.
[18] Y.-Y. Tzou and H.-J. Hsu, "FPGA realization of space-vector PWM control IC for three-phase PWM inverters," *IEEE Trans. Power Electron.*, Vol. 12, No. 6, pp. 953-963, Nov. 1997.
[19] N. A. Rahim and Z. Islam, "field programmable gate array-based pulse-width modulation for single phase active power filter," *American Journal of Applied Sciences*, Vol. 6, No. 9, pp. 1742-1747, 2009.
[20] E. J. Bueno, A. Hernandez, F. J. Rodriguez, C. Giron, R. Mateos, and S. Cobreces, "A DSP-and FPGA-based industrial control with high-speed communication interfaces for grid converters applied to distributed power generation systems," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 3, pp. 654-669, Mar. 2009.
[21] K. Sugahara, S. Oida, and T. Yokoyama, "High performance FPGA controller for digital control of power electronics applications," in *Proc. IPEMC*, pp. 1425-1429, 2009.
[22] L. Idkhajine, E. Monmasson, M. W. Naouar, A. Prata, and K. Bouallaga, "Fully Integrated FPGA-Based Controller for Synchronous Motor Drive," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 10, pp. 4006-4017, Oct. 2009.
[23] F. J. Azcondo, A. de Castro, and C. Brañas, "Course on digital electronics oriented to describing systems in VHDL" *IEEE Trans. Ind. Electron.*, Vol. 57, No. 10, pp. 3308-3316, Oct. 2010.
[24] S. McKeown and R. Woods, "Low power field programmable gate array implementation of fast digital signal processing algorithms: characterisation and manipulation of data locality," *IET Computers & Digital Techniques*, Vol. 5, No. 2, pp. 136-144, Mar. 2011.
[25] A. Myaing and V. Dinavahi, "FPGA-based real-time emulation of power electronic systems with detailed representation of device characteristics," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 1, pp. 358-368, Jan. 2011.
[26] C. Canudas-de-Wit, F. Gomez-Estern, and F. R Rubio, "Delta-modulation coding redesign for feedback-controlled systems," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 7, pp. 2684-2696, Jul. 2009.
[27] M. H Kheraluwala and D. M. Divan, "Delta modulation strategies for resonant link inverters," *IEEE Trans. Power Electron.*, Vol. 2, No. 5, pp. 220-228, Apr. 1990.
[28] C. F. Christiansen, M. I. Valla, and C. H. Rivetta, "A synchronization technique for static delta PWM inverter," *IEEE Trans. Ind. Electron.*, Vol. 35, No. 4, pp. 502-507, Nov. 1988.
[29] P. D. Ziogas, "The delta modulation technique in static PWM inverter," *IEEE Trans. Ind. Appl.*, Vol. IA-17, No. 2, pp.199-204, Mar./Apr. 1981.
[30] J. Paramesh and A. von Jouanne, "Use of sigma-delta modulation to control EMI from switch-mode power supplies," *IEEE Trans. Ind. Electron.*, Vol. 48, No. 1, pp. 111-117, Feb. 2001.



Anshul Agarwal was born in Mathura, India, on May 05, 1984. He received his B.Tech. in Electrical and Electronics Engineering, from the Uttar Pradesh Technical University, Lucknow, India, in 2007, and his M.Tech (Gold Medalist) in Power Electronics and ASIC Design from the Motilal Nehru National Institute of Technology (MNNIT), Allahabad, India, in July 2009. He is currently working as Assistant Professor in the Electrical Engineering Department, National Institute of Technology, Hamirpur (NIT Hamirpur), Himachal Pradesh, India. His current research interests include power electronic devices, converters, inverters and AC to AC converters.

Vineeta Agrawal received her B.E. and M.E. from Allahabad University, Allahabad, India, in 1980 and 1984, respectively. She joined the Electrical Engineering Department at the Motilal Nehru Regional Engineering College, Allahabad, India, as a Lecturer, in 1982. While teaching there, she obtained her Ph.D. in Power Electronics. At present she is a Professor in the Department of Electrical Engineering at the Motilal Nehru National Institute of Technology (MNNIT), Allahabad, India. She has taught numerous courses on Electrical Engineering and Electronics. Her current research interests include single phase to three-phase conversions and AC drives. She has a number of publications in journals and conferences in her field. She has attended and presented papers at both national and international conferences.