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A Dual-Output Integrated LLC Resonant Controller and LED Driver IC with PLL-Based Automatic Duty Control

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Abstract

This paper presents a secondary-side, dual-mode feedback LLC resonant controller IC with dynamic PWM dimming for LED backlight units. In order to reduce the cost, master and slave outputs can be generated simultaneously with a single LLC resonant core based on dual-mode feedback topologies. Pulse Frequency Modulation (PFM) and Pulse Width Modulation (PWM) schemes are used for the master stage and slave stage, respectively. In order to guarantee the correct dual feedback operation, Phased-Locked Loop (PLL)-based automatic duty control circuit is proposed in this paper. The chip is fabricated using 0.35 μm Bipolar-CMOS-DMOS (BCD) technology, and the die size is 2.5 mm × 2.5 mm. The frequency of the gate driver (GDA/GDB) in the clock generator ranges from 50 to 425 kHz. The current consumption of the LLC resonant controller IC is 40 mA for a 100 kHz operation frequency using a 15 V supply. The duty ratio of the slave stage can be controlled from 40% to 60% independent of the frequency of the master stage.

Key words: LLC resonant converter, Phase-Locked Loop, PWM dimming, Dual-mode feedback, Clock generator, Dead time, Duty ratio, Duty control, LED driver, Soft-start, PFM, PWM

I. INTRODUCTION

Recently, light-emitting diodes (LEDs) have become one of the most promising candidates for backlight units (BLUs) in LCD monitors or TVs and other lighting applications [1]-[3]. In order to reduce the cost and increase the efficiency of the LED TV, DC-DC converters are replaced with high efficiency LLC resonant converters, and discrete components in the printed circuit board (PCB) are integrated into ICs. LLC resonant converters are popularly adapted for consumer or industrial electronics due to their inherent advantages over contending topologies [4]-[7]. Such advantages enable a highly efficient operation over a wide input voltage range as a consequence of the very low switching losses found in zero voltage switching (ZVS) conditions. In addition, these converters are suitable for integration, since the two inductors required to form the LLC tank can be integrated into one magnetic core without the need for extra components [8]–[11].

The advantage of LLC resonant converters is that they can reduce the switching loss and noise since switching components are softly commutated based on the resonant technique. Also, they can detect the load variation efficiently since a large voltage gain can be obtained with a small switching frequency variation thanks to mutual inductance. Generally, resonant power transfer systems require galvanic isolation between the relatively high input voltage and the low output voltages. The most widely used devices employed to transfer signals across the isolation boundary are pulse transformers and opto-couplers, which are used in order to provide regulation for the output [12], [13]. Opto-couplers are typically used to isolate the secondary side power supply from the primary side PFM control. Primary side control of an LED back light unit causes the LED driver system to be complicated and bulky because of the need for op-amps, isolation, and discrete devices to be used for detecting the secondary side load variations and then to feed these back to the primary side.

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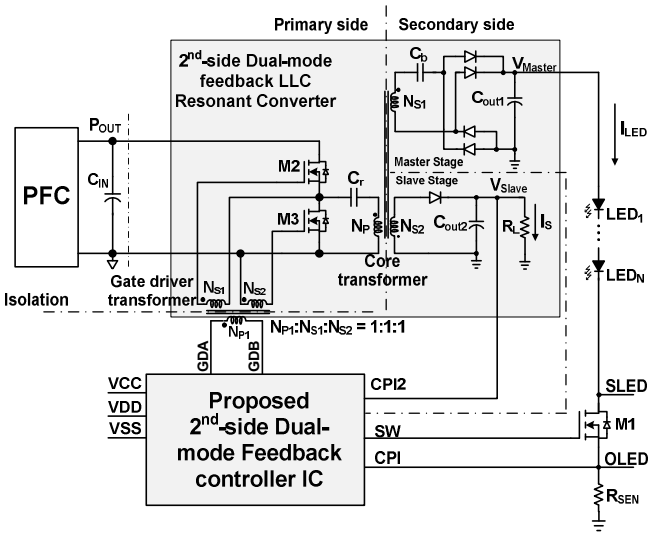

Fig. 1. Secondary side Dual-mode Feedback LLC Resonant Converter.

In order to remove the opto-coupler from the feedback loop and achieve fast dynamic performance, a secondary side output regulation method has been presented [14]. However, it requires an additional chopper circuit to regulate against line variations.

In this paper, a simple LED driving circuit and a secondary side LLC resonant controller IC is designed in order to reduce the complexity and the circuit dimensions. We propose a dual mode LLC resonant controller IC topology to provide two outputs with one LLC resonant core. Master and slave voltages are generated from the LLC resonant converter simultaneously. The master stage is controlled by the switching frequency of the clock and the slave stage is controlled by the duty ratio of the clock.

II. PROPOSED SECONDARY SIDE DUAL-MODE FEEDBACK LLC RESONANT CONTROLLER IC ARCHITECTURE

Fig. 1 shows the block diagram of the proposed secondary side dual-mode feedback LLC resonant converter. By moving the resonant controller IC from the primary side to the secondary side, the isolation components can be removed, resulting in reduced area and cost of the system. The power consumption can be reduced using the high side transformer for the master stage and low side transformer for the slave stage with the power MOSFETs (M2, M3).

This approach has advantages in terms of the area and cost thanks to the gate driver transformer and integration of the dimming circuits into the IC.

Fig. 2 shows the proposed dual-feedback secondary-side dual-mode feedback controller and LED driver IC. It is composed of a clock generator, dead time generator, gate driver, protection, current generator, dimming circuit, bandgap-reference, duty control circuit, and automatic min/max generator. When the voltage VCC is over the threshold under voltage lock out (UVLO) and the operating temperature is in the range of -40 °C ~ 135°C, the output of thermal shut down (TSD) is HIGH and the VDD is generated by the bandgap-reference (BGR).

The signal PWRONb is high for a certain duration in order to initialize the operation of the comparator and amplifier as well as the digital block after voltage VDD is saturated to the nominal voltage level. When it goes to low, all the internal circuits go to normal states. After the initialization, the power supply block provides the currents to all the sub-blocks. The frequency of the clock generator is determined by the current I_{CHARGE}.

The dead time is determined by the current $I_{DEADTIME}$. The dimming circuit controls the external dimming switch by a PWM signal. The internal feedback regulates the static current of the master stage LED by changing the resistor value and current of the current generator for stable LED control.

The min/max generator provides the V_{MIN} and V_{MAX}

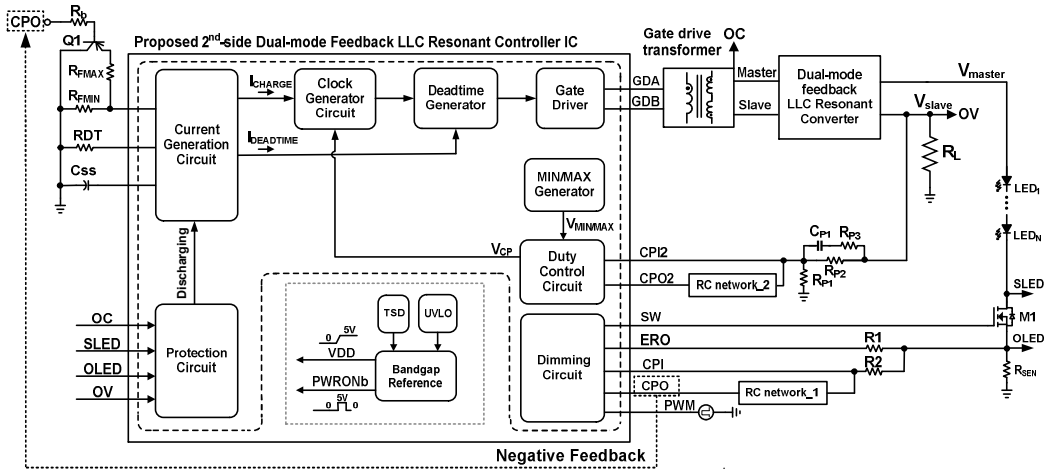

Fig. 2. Block diagram of secondary side dual-mode feedback LLC resonant controller IC.

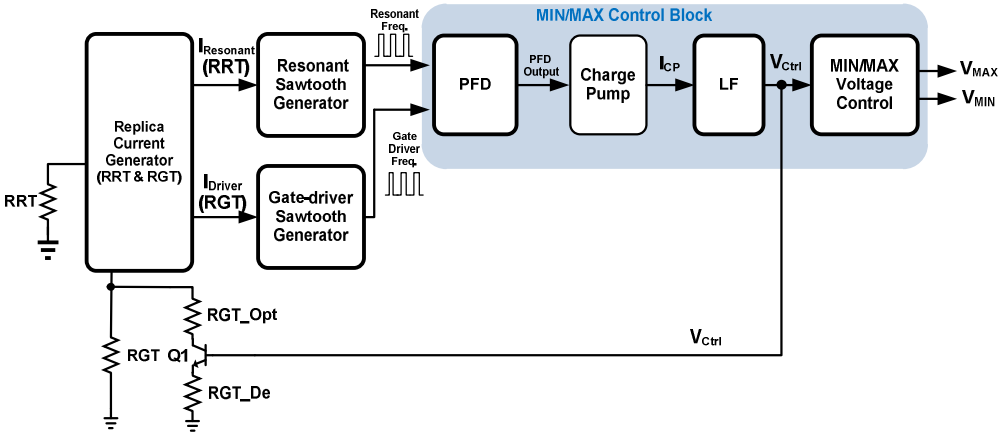

Fig. 3. Block diagram of MIN/MAX generator using the phase-locked loop.

voltages which are used as reference voltages in the duty control circuit to guarantee system stability through the internal PLL loop. The duty control circuit generates the voltage V_{CP} to regulate the static current of the slave stage. The clock generator utilizes this voltage for the feedback operation in the slave stage.

III. Building Blocks of 2nd-side Dual-mode Feedback LLC Resonant Controller IC

A. Min/Max Generator

The duty ratio of the gate driving signals (GDA, GDB) should be limited to certain ranges based on the load conditions of the master and slave stages in the proposed dual-feedback topology. Thus, the feedback voltage V_{CP} should be located between V_{MIN} and V_{MAX} to guarantee the stable operation. However, if V_{MIN} and V_{MAX} voltages are fixed, the slave stage of the dual feedback system cannot track the large frequency variation. To implement this operation, the min/max voltages of V_{CP} should track the frequency of the clock generator circuit to maintain the stable range of duty ratio regardless of the frequency.

Thus, an automatic min/max generator is proposed to control the duty ratio depending on the frequency of the gate driver and to guarantee the correct operation of the dual feedback system under large load current variation conditions.

This scheme can be easily adapted to other systems with different resonant frequencies with variations of the component values.

Fig. 3 shows the block diagram of the automatic min/max generator using the phase-locked loop. It is composed of a replica current generator (RRT&RGT), resonant sawtooth generator, gate-driver sawtooth generator, phase frequency detector (PFD), charge pump (CP), loop filter (LF), and min/max voltage control block.

Fig. 4 (a) and (b) show the block diagram of the current generator for RRT and RGT, respectively. Each is composed of

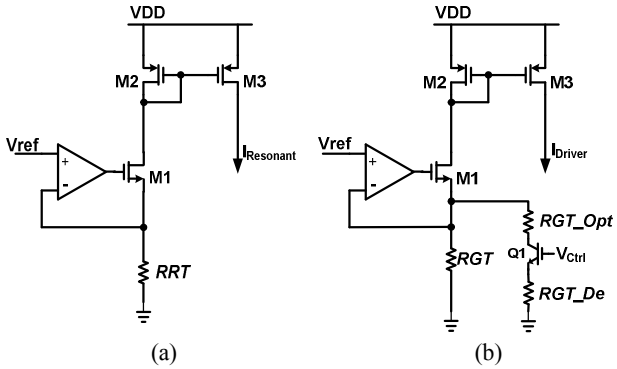

Fig. 4. (a) RRT (b) RGT current generator.

an error amplifier and a current mirror. The gate voltage of M1 is determined by the error amplifier and resistance values (RRT, RGT). In Fig. 4 (a), the drain current of M1 is duplicated to the output current, $I_{Resonant}$, through the current mirror composed of M2 and M3. In Fig. 4 (b), the current of the RGT current generator is controlled by the voltage V_{Ctrl} from the loop filter (LF) applied to the base of the BJT and resistors (*RGT_Opt* and *RGT_De*).

Fig. 5 shows the block diagram of the sawtooth generator resonant circuit and gate-driver. Capacitor C1 is charged by the current from the current generator and the voltage V_{SAW} rises. When the voltage V_{SAW} is equal to the voltage V_H, the comparator COMP1 is high, turning on M1 and discharging the voltage from C1. The sawtooth signal V_{SAW} is generated by repeating the above operation. The comparator COMP2 compares the sawtooth signal V_{SAW} with $V_{H/2}$ generating the pulse signal V_{FREQ}. V_H and $V_{H/2}$ are the reference voltages for COMP1 and COMP2, respectively.

Fig. 6 shows the Phase Frequency Detector (PFD). PFD detects the differences of phase and frequency between the input signal and feedback signal. When the phase difference is too small, PFD cannot detect the difference, which is called the dead-zone problem. In order to alleviate this problem, a delay block is added to the reset delay path as shown in Fig. 6.

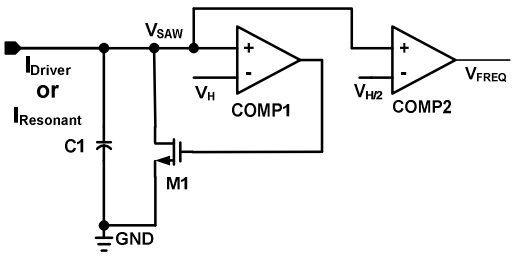

Fig. 5. Sawtooth generator for resonant circuit and gate-driver.

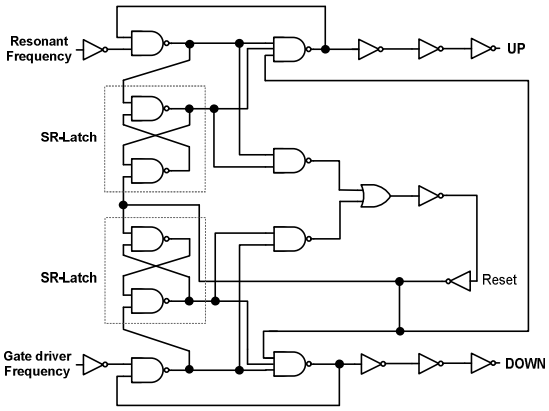

Fig. 6. Phase Frequency Detector (PFD).

Fig. 7 shows the architecture of the Charge Pump (CP) and Loop Filter (LF). The CP provides the current to the LF based on the output of the PFD.

A unity gain buffer is inserted to make the drains of M3 and M4 equal since the matching characteristics are important in the differential charge pump architecture. A 2nd order loop filter is adopted to reduce the die area.

PFD compares the resonant frequency and gate driver frequency. As shown in Fig. 8 (a), the signal UP is asserted when the frequency of the gate driver is slower than the resonant frequency. The duration of the signal UP is proportional to the phase frequency difference. When the signal DOWN goes to HIGH at the rising edge of the gate driver, the signals UP and DOWN reset to LOW after the reset delay.

On the other hand, the signal DOWN is asserted when the frequency of the gate driver is faster than the resonant frequency as shown in Fig. 8 (b). The duration of the signal DOWN is proportional to the phase frequency difference. When the signal UP goes to HIGH at the rising edge of the resonant frequency, the signals DOWN and UP reset to LOW after the reset delay.

Fig. 9 shows the min/max voltage control block. The min/max voltage control block generates the minimum voltage V_{Min} and maximum voltage V_{Max} from the control voltage V_{Ctrl} of phase-locked loop. The current I_{Ctrl} is determined by V_{Ctrl}, R_1, and R_2. It is duplicated to I_{Min} and I_{Max} through the current mirrors composed of M_1, M_2, M_3, M_5, and M_6. As a results, V_{Min} and V_{Max} are determined as I_{Min} x R_{Min} and $V_{DD} - I_{Max}$ x R_{Max}, respectively.

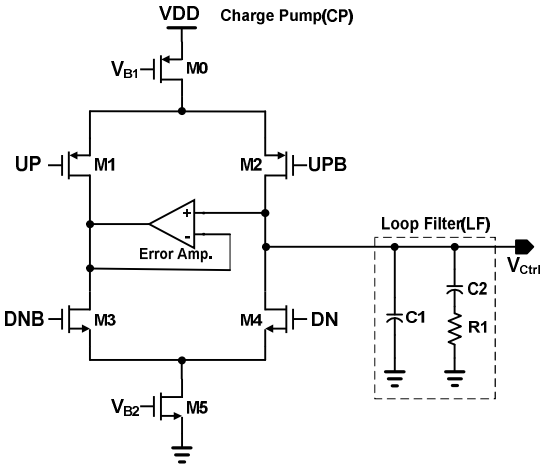

Fig. 7. Charge Pump (CP).

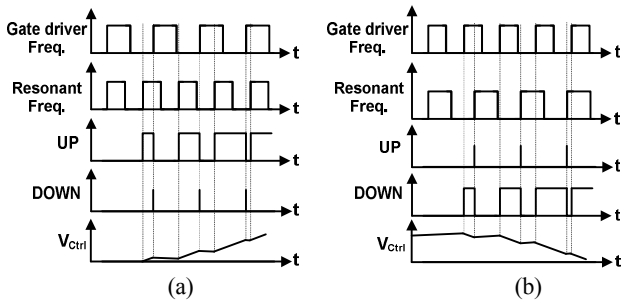

Fig. 8. The output waveforms of MIN/MAX generator (a) when the gate driver frequency is slower than the resonant frequency (b) when the gate driver frequency is faster than the resonant frequency.

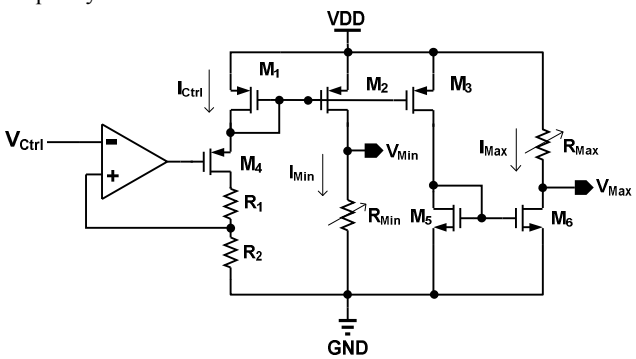

Fig. 9. MIN/MAX voltage control block.

Fig. 10 (a) and (b) show the output waveforms of min/max generator when V_{Ctrl} in the LLC resonant converter system is increased and decreased, respectively. In Fig. 10 (a), the maximum voltage increases and the minimum voltage decreases as the voltage V_{Ctrl} is increased due to the large frequency difference. On the other hand, the maximum voltage decreases and the minimum voltage increases as the voltage V_{Ctrl} is decreased due to the small frequency difference, as shown in Fig. 10 (b).

Minimum/maximum voltages guarantee stable system operation, although the duty ratio of the gate driver is changed. The minimum voltage V_{MIN} and maximum voltage V_{MAX} are

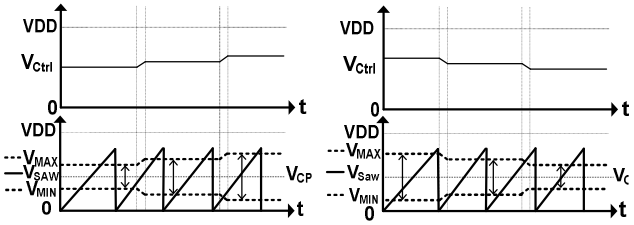

Fig. 10. The output waveforms of MIN/MAX generator (a) when V_{Ctrl} is increased (b) when V_{Ctrl} is decreased.

determined as in (1) and (2):

$$V_{MIN} = \frac{I_{Charge} \cdot T_s}{C_{SAW}} \quad (1)$$

$$V_{MAX} = V_H - \frac{I_{Charge} \cdot T_s}{C_{SAW}} \quad (2)$$

If the duty ratio of GDA/GDB is less than the minimum duty T_s, the current cannot be transferred to the secondary side because resonance requirements cannot be met. Thus, the duty control circuit is designed to limit the duty ratio of GDA and GDB.

Fig. 11 shows the duty control circuit. The error amplifier generates the error between the output of the slave stage CPI2 and V_{DREF}. It is compared with V_{MIN} and V_{MAX} voltages to control the clock frequency of the clock generator through the voltage V_{CP}. A Type-3 op-amp compensation network is adopted in the error amplifier for frequency compensation.

The two comparators in min/max limit block in Fig. 11 compare the voltage CPO2 with V_{MIN} and V_{MAX} from the min/max generator. Fig. 12 shows the waveforms of V_{CP} depending on the signal of CPO2 and the signals related to dead-time (D_{OUT}, GDA/GDB). As shown in Fig. 12, when the voltage CPO2 is smaller than the V_{MIN}, the output of the comparator is fixed to V_{MIN}. In the same manner, if voltage CPO2 is larger than V_{MAX}, the output of the comparator is fixed to V_{MAX} as in Fig. 12.

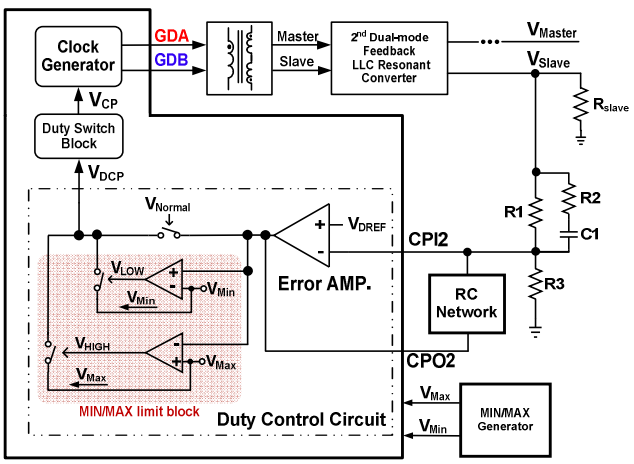

Fig. 11. Duty Control Circuit.

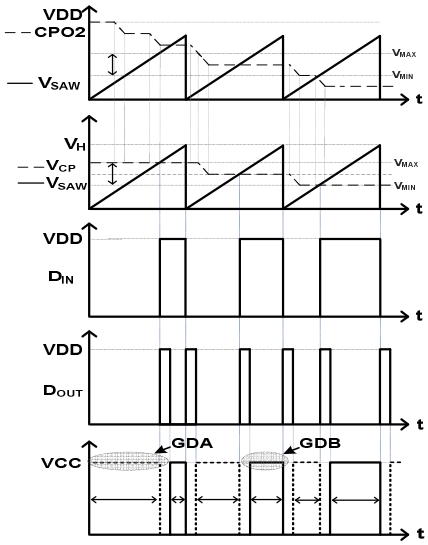

Fig. 12. The output waveforms of Duty Control Block.

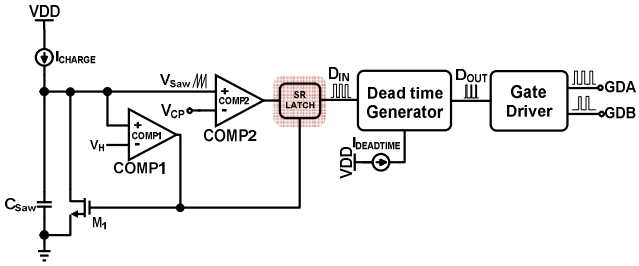

Fig. 13. Single-slope Sawtooth Clock Generator.

As shown in Fig. 12, the voltage V_{CP} is limited to pre-determined ranges by forcing the output of the error amplifier to be located between V_{MIN} and V_{MAX}.

The error amplifier utilizes Type-3 op-amp compensation with an RC network to guarantee system stability. The voltage V_{CP} from the duty control block is applied to the reference voltage of COMP2 in the single-slope sawtooth clock generator. It is used to control the duty ratios of GDA and GDB, which are the outputs of the gate driver.

B. Single- Slope Sawtooth Clock Generator

Fig. 13 shows the single-slope sawtooth clock generator. The voltage across the C_{saw} is charged by the current I_{CHARGE}. When the voltage reaches V_H, the charge in C_{saw} will be discharged through the transistor M_1 generating the sawtooth waveform [5],[6]. The frequency of the clock generator is determined by (3).

$$f_{OUT} = \frac{1}{T} = \frac{I_{CHARGE}}{C_{SAW} \cdot V_H} \quad (3)$$

In addition, the duty ratio of the clock generator is determined by the voltage V_{CP} applied to the comparator COMP2.

C. Dimming Circuit

Dimming is one of the important design issues to control

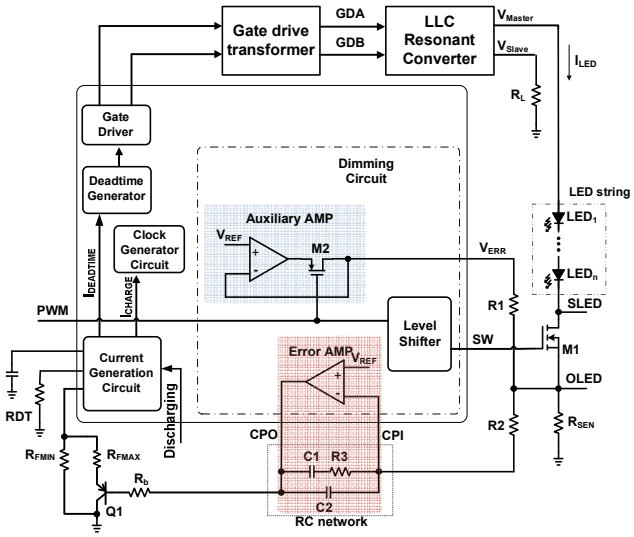

Fig. 14. PWM Dimming Circuit.

LED brightness through the current along with the current balancing function of an LED channel [3][7][8].

Fig. 14 shows the PWM dimming. In Fig. 14, the LED current is blocked by the switch, M1, when the dimming control signal SW is LOW. This will cause a transient over voltage problem of the output voltage in the un-loaded condition in the LED driving stage, which will result in large in-rush current to the LED channel at the instant when the dimming control signal SW goes from LOW to HIGH.

In order to alleviate this problem, an auxiliary amplifier is added as shown in Fig. 14. V_{SEN} is the voltage detecting the LED current through the resistor R_{SEN}. When the dimming control signal is HIGH, the switch M2 is turned off and V_{SEN} is applied to the negative terminal of the error amplifier, which results in the correct operation of the LED driving circuits.

On the other hand, when dimming control signal is LOW, the switch M2 is turned on and V_{SEN} is applied to the negative terminal of the error amplifier, which reduces the rising time of the LED current at the instant of dimming on. When an LED short occurs during the dimming on and the voltage ERO is over V_{REF}, the voltage CPO is saturated to the minimum voltage and the current I_{CHARGE} will be increased through the resistor R_{FMAX}. Thus, the output frequency of the LED Driver IC is increase to the maximum frequency set by RFMAX and the voltage gain of the LLC resonant converter is decreased to compensate for the over voltage of the output due to the LED short.

IV. MEASUREMENT RESULTS

This chip is implemented in a 0.35 μm BCD 2poly 3metal process. The die area is 2500 ㎛ x 2500 ㎛ including the pads, and the 48-TQFP package is used. Fig. 15 shows the chip layout pattern of the secondary-side dual-mode feedback LLC resonant controller IC.

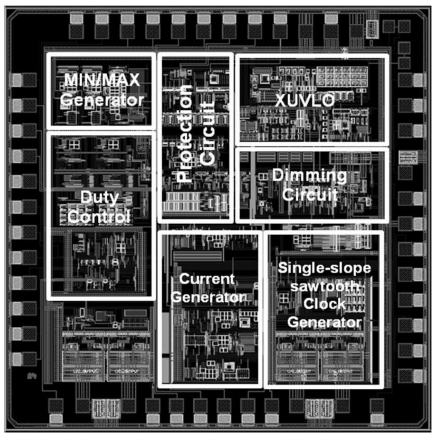

Fig. 15. Chip layout pattern.

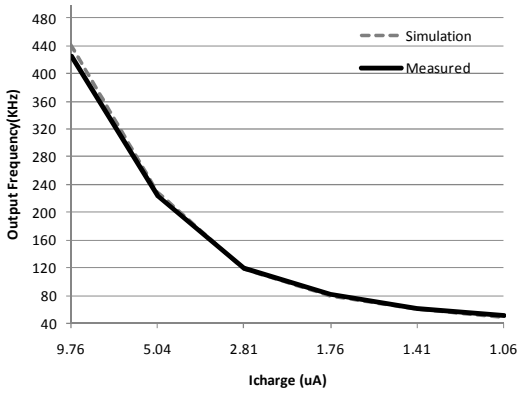

Fig. 16. Measured frequency control range with respect to charging current variation.

The input and output voltages of the LLC resonant converter is 385 V and 32 V, respectively. The LED current is 500 mA at 100% of PWM dimming condition. The PWM dimming frequency is 200 Hz for this experiment. Since the input power is 35 W and the output power is 32 W, measured power efficiency of the LED driving circuit is about 91 %.

The conduction loss, turn-off switching loss, power consumption of the control circuit, inductor loss, and transformer loss degrade the power efficiency of the LLC resonant converter [15],[16].

Fig. 16 shows the frequency control range of the single-slope clock generator with respect to the charge current I_{charge} variation. The frequency control range of the gate driver is from 425 kHz to 50 kHz when I_{charge} is swept from 9.76 μA to 1.06 μA. They show good agreement with the calculated results from (3).

Fig. 17 shows the measured waveforms of the duty ratio variation of GDA and GDB with respect to voltages V_{Slave}. The duty ratios of GDA and GDB are controlled from 60 % to

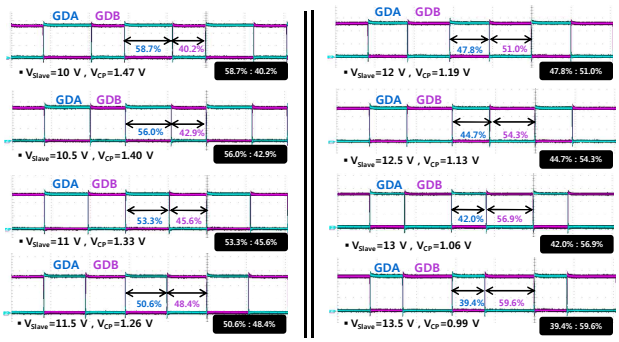

Fig. 17. Measured waveforms of the duty ratio variation with respect to V_{Slave}.

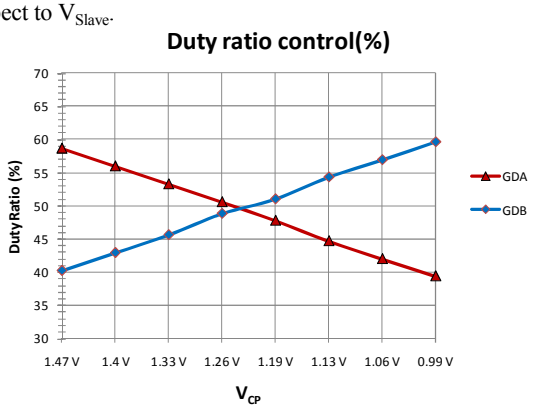

Fig. 18. Measured graph showing the relationship between the duty ratio of GDA/GDB and V_{CP}.

40 % and from 40 % to 60 % as voltage V_{Slave} is changed from 10 V to 13.5 V at the resonant frequency of 100 kHz.

Fig. 18 is the measured graph showing the relationship between the duty ratio of GDA/GDB and V_{CP}. The duty ratios of GDA and GDB are controlled from 60 % to 40 % and from 40 % to 60 % as the voltage V_{CP} is changed from 1.47 V to 0.99 V at the resonant frequency of 100 kHz.

Fig. 19 shows the top simulation result of a min/max generator block using PLL. The settling time of the PLL is about 5 ms. In the locked state, V_{MAX} and V_{MIN} are determined as 1.9 V and 0.778 V, respectively.

Fig. 20 shows the measurement result of V_{Ctrl} and V_{MIN}/V_{MAX} voltage variation with respect to resistor RG. V_{Ctrl} and V_{MAX} are increased as the resistor RG is increased from 40 kΩ to 124 kΩ. On the contrary, V_{MIN} is decreased as the resistor RG is increased from 40 kΩ to 124 kΩ.

Fig. 21 shows the measured duty ratio variations with respect to the PWM dimming ratio. It shows the waveforms corresponding to PWM dimming ratio of 10%, 30%, 50%, and 90 % from the top.

V. CONCLUSIONS

In this paper, a dual-feedback LED driver IC that can control the secondary-side dual-mode feedback LLC resonant converter and regulates the secondary-side LED current is presented.

A dual feedback architecture is also proposed to generate dual DC outputs with one transformer core to reduce the system complexity. In the proposed architecture, the master stage is controlled by PFM and the slave stage is controlled by PWM. The duty ratio of GDA and GDB is controlled by the feedback voltage from the slave stage. In order to guarantee the correct system operation and control the duty ratio of GDA and GDB, the automatic min/max generator using the PLL is proposed.

This chip is implemented in 0.35 μm BCD 2 poly 3 metal

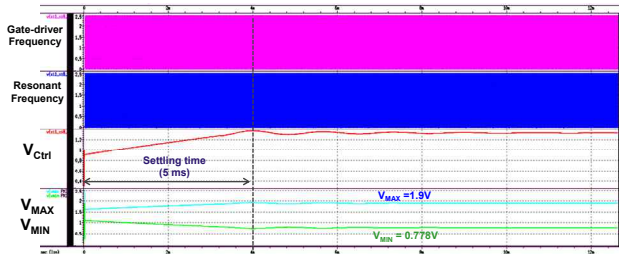

Fig. 19. Top simulation result of MIN/MAX Generator block using PLL.

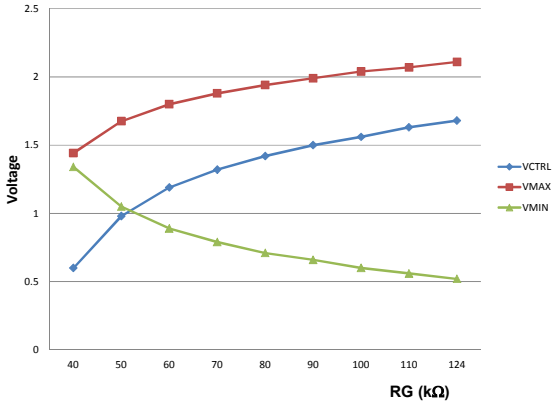

Fig. 20. Measurement result of V_{Ctrl} and VMIN/VMAX voltage variation with respect to RG.

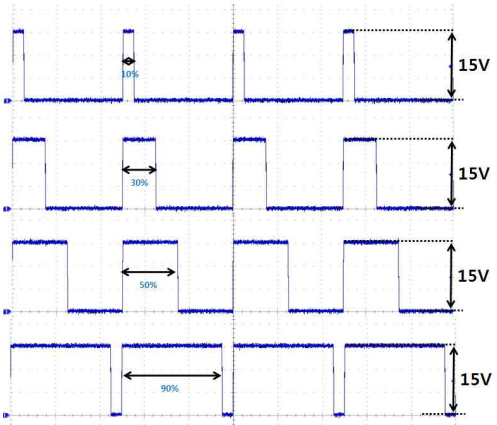

Fig. 21. Measured duty ratio variations with respect to the PWM dimming ratio.

process and the die area is 2500 μm x 2500 μm including pads. The range of the single-slope sawtooth clock generator is from 50 kHz to 425 kHz. The output range of the dead time generator is from 35 ns to 2.2 μs. The stable range of the duty ratio for the secondary side is from 40% to 60% when the resonant frequency is 100 kHz.

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