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Integrated DC-DC Converter Based Energy Recovery Sustainer Circuit for AC-PDP

Jae-Sung Park*, Yong-Saeng Shin*, Sung-Soo Hong*, Sang-Kyoo Han*, and Chung-Wook Roh†

*†Dept. of Electrical Engineering, Kookmin University, Seoul, Korea

Abstract

A new sustainer with primary-side integration of DC/DC converters and energy recovery(SPIDER) circuits is proposed. The proposed circuit operates as a DC-DC converter during address period and energy recovery circuit during sustain period. Therefore, the conventional three electronic circuits composed of the power supply, X-driver, and Y-driver can be reduced to one circuit. As a result, it has desirable advantages such as a simple structure, less mass, fewer devices and cost reduction. Moreover, since the Zero Voltage Switching (ZVS) of all power switches can be guaranteed, a switching loss can be considerably decreased. To confirm the operation, validity, and features of the proposed circuit, experimental results from a prototype for 42-inch PDP are presented.

Keywords: ADS(Address Display-period Separation) method, Energy Recovery Circuit, Plasma Display Panel, Sustain driver

I. INTRODUCTION

As high-definition digital broadcasting era comes, the flat panel display market is fulfilled by the two main axes of the liquid crystal display (LCD) and plasma display panel (PDP) TV.The PDP has many advantages such as large screen size, self-luminous display, high contrast, and fast response compared with the LCD [1], [2].However, due to the rapid progress of the large size LCD and LED TV, the PDP is losing competitiveness in flat panel display market. To overcome these kinds of situations, various researches and developments to minimize the cost have been done.

Fig. 1 shows the configuration of the conventional PDP driver. The conventional PDP driver is composedof a panel part and a driver part. The driver part is made up of electronic circuits such as a power supply, X driver, Y driver, logic board, and etc. To drive the PDP, the X and Y drivers require many kinds of power sources such as a sustain voltage (V_S), address voltage (V_a), and so forth. To generate these voltage sources, the LLconverter is usually used due to its desirable merits such as the high power conversion efficiency, low cost, and excellent dynamic characteristics.

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†CorrespondingAuthor:drno@kookmin.ac.kr
Tel: +82-2-910-4947, Fax: +82-2-910-4449,Kookmin University
*Dept. of Electrical Engineering, Kookmin University, Korea

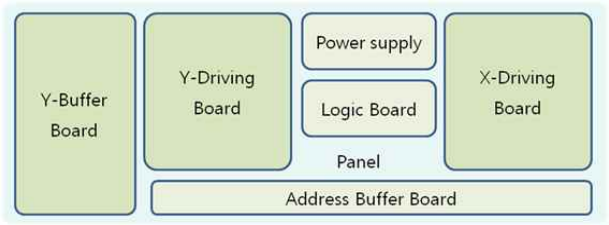


Fig. 1.Construction of Conventional PDP driver.

Generally, the PDP needs a high-voltage and high-frequency switching power circuit called X and Y drivers to ignite the gas discharge of the PDP. The X and Y drivers have a full-bridge configurationto convert to convert a DC high voltage to an AC high-voltage high-frequency square-wave pulses. Since the X and Y electrodes of the PDP are covered by the dielectric layer, the PDP is regarded as a capacitive load C_P. Therefore, when we apply AC high-voltage high-frequency square-wave pulses with the amplitude of V_S between X and Y electrodes, the undesirable energy loss of $2C_PV_S^2$ is generated during charging and discharging intervals without an energy recovery circuit. Moreover, the excessive surge charging and discharging currents will give rise to EMI noises and increase the surge current ratings of switches. To relieve these problems, several previous X and Y drivers called energy recovery circuits (ERCs) have been proposed [3]-[8].

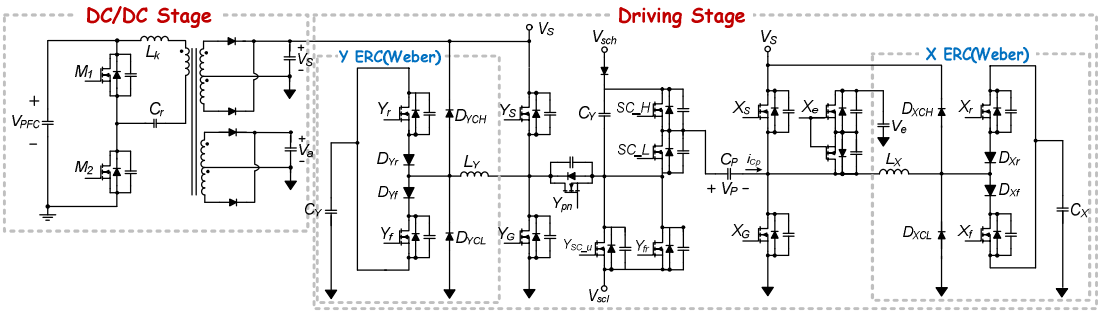


Fig. 2. Block diagram of conventional PDP system – Weber and Wood energy recovery circuit.

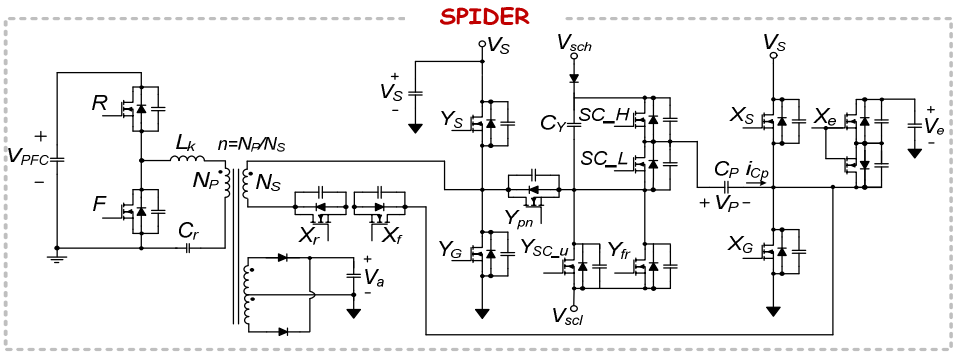


Fig. 3. Block diagram of the proposed PDP system– SPIDER circuit.

Among hitherto developed ERCs, the Weber and Wood energy recovery circuit shown in Fig. 2 is most frequently used thanks to the high efficiency and good circuit flexibility [5], [9], [10]. Although it can recover most of the lost energy, it still has several drawbacks. Its two identical large auxiliary ERCs on both sides of the PDP are composed of four active power switches, eight power diodes, two inductors and two external capacitors. Also the conventional PDP system consists of cascaded two power stages that are the DC/DC power stage and the driving stage. Therefore, theconventional PDP system has several disadvantages such as its bulky size, poor efficiency, and high production cost. The sustain drivers proposed in [4], [5] and [6] reduce two switches and several diodes. Although they can achieve cost-effective sustain driver, they still have bulky inductors and several external capacitors. Therefore, the peak values and r.m.s. values of the inductor currents are high [6]. A sustain driver using the voltage stress reduction technique is proposed in [7]. Its circuit reduces two clamp diodes and voltage stress of the main switches by half, i.e., V_S, compared with a conventional single sustain driver. However, the voltage stress of the auxiliary switches is same as the conventional sustain driver. The sustain driving method proposed in [8] reduces the peak values and rms values of the inductor currents, which then leads to the conduction loss of the inductors to be reduced. However, its circuit has two external inductors and four external capacitors, thus the proposed circuit in [8] is still bulky.

To overcome these drawbacks, a sustainer with primary-side integration of DC-DC converters and energy recovery (SPIDER) circuits for AC PDP is proposed as shown in Fig. 3. The proposed circuit integrates the DC/DC power stage and driving stage into one circuit. Not only the proposed circuit can supply the energy to the PDP driver, but also it recovers the energy stored in the PDP, which means it has very desirable advantages such as a simpler structure, less mass, fewer power devices, and lower cost. Moreover, the ZVS of primary side switches (*R, F*) and secondary side switches can always be guaranteed by the magnetizing and energy recovery currents, respectively.

II. PROPOSED CIRCUIT

Generally, PDPs are driven by the address display-period separation (ADS) method. Fig. 4 shows the conventional key driving waveforms of the PDP with the ADS driving method[4], [11], [12].A 1TV-field is the time it takes to display one image, typically 16.7 msec, i.e., 60 Hz in NTSC (National Television System Committee) mode. It is divided into 8~11 sub-fields. A sub-field is a group of the light information and partitioned into three periods as reset, address and sustain periods. During the reset period, all of the PDP cells are erased and prepared to carry out the address-operation by forming adequate wall charges. Then, during the address period, selectivewritedischarges to form an image are ignited by applying data and scan pulses to the addressing and scanning electrodes, respectively.Since address-discharge itself emits aninsufficient visible light, AC high-voltage square-wave pulses generated by the X and Y driver are continuously

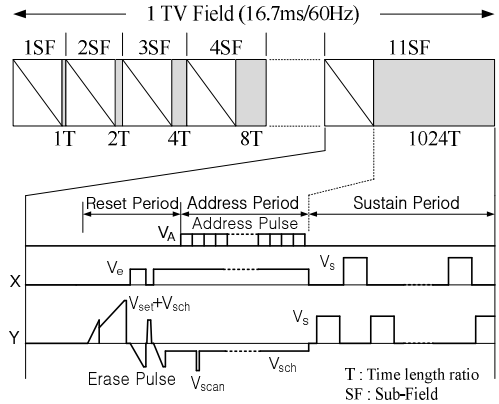


Fig. 4. Voltage waveforms applied to X and Y electrodes in ADS method during 1TV-field (NTSC mode).

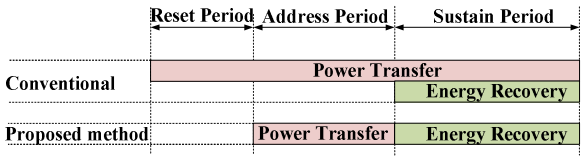
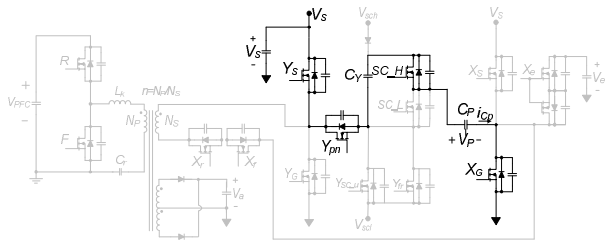


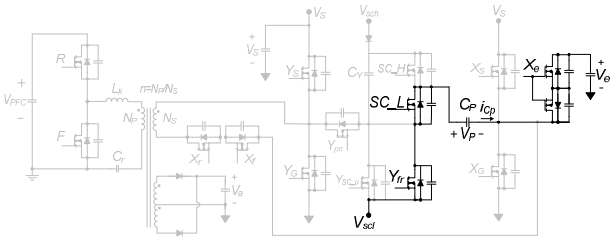
Fig. 5. Comparison of the conventional driving method and the proposed driving method.

applied between sustaining and scanning electrodes for the strong light emission of selective cells.

As shown in Fig. 5, the conventional PDP system is provided with the driving energy during whole periods and the energy stored in the PDP is recovered by ERCs during sustain period. On the other hand, the proposed system is provided with the driving energy only during address period and the energy stored in the PDP is recovered by ERCs during sustain period like the conventional system.



(a) Conductive path for the rising ramp.



(b) Conductive path for the falling ramp.

Fig. 6. The equivalent circuit diagram during reset period.

Namely, while the conventional system requires the power supply circuit and ERC separately, the proposed system can supply the driving power and recover the energy stored in the PDP by using one combined power conversion circuit at the same time. To achieve these operation, the pulse frequency modulation (PFM) method during an address period and the pulse width modulation (PWM) method duringan sustain period are used to control the proposed circuit.

A. Reset Period

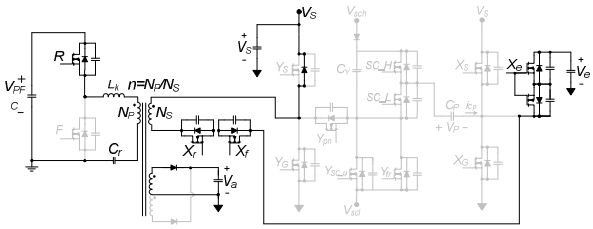
In reset period, rising and falling ramp waveforms are applied to Y electrodes to initialize the PDP as shown in Fig. 4. Fig. 6(a) shows the conductive path for the rising ramp waveform. Y_{pn} and SC_H are turned on and Y_S is operated in the linear region by the low gate-to-source voltage. Therefore, Y_S is operated as the current source and the current through Y_S is linearly increased as follows,

$$I_{D,Y_S} = K_n(V_{GS} - V_{TN})^2 \tag{1}$$

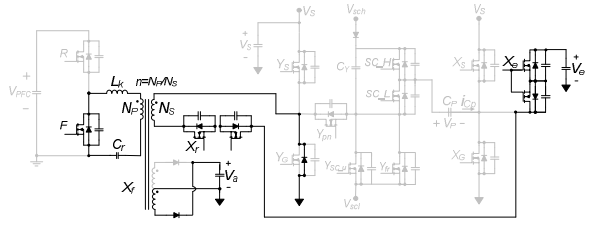
where,K_n is the conduction parameter of the N-channel device and is given by $K_n = W\mu C_{ox}/2L$, V_{GS} is the voltage between gate and source of the switch and V_{TN} is the threshold voltage of the N-channel MOSFET.

Therefore, the voltage V_{Cp} across the panel capacitor C_P is linearly increased by $I_{D,Ys}$ and the rising ramp waveform is applied to Y electrodes. At this point, when two path switches X_r and $X_f$are turned off, the undesirable resonance between the transformer and C_P does not occur and the ramp waveform is linearly increased. Moreover, due to the fact thatX_G is turned on, 0V is applied to X electrodes.

Fig. 6(b) shows the conductive path for the falling ramp waveform. When SC_L is turned on and Y_{fr} is operated in the linear region, the falling ramp waveform is applied to Y electrodes. Also, if X_e is turned on, V_e is applied to X electrodes.



(a) Conductive path when *R* is on.



(b) Conductive path when *F* is on.

Fig. 7. The equivalent circuit diagram during address period.

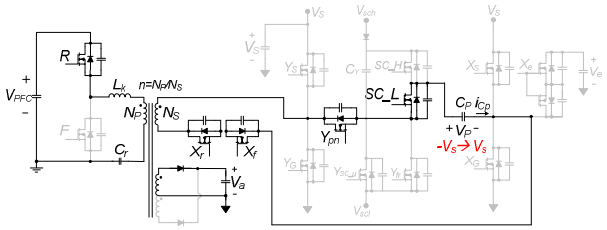
B. Address Period

In address period, as shown in Fig. 4, the selective cells are ignited to form a desired image by applying data and scan pulses to the X and Y electrodes, respectively. Fig. 7 shows the conductive path during address period. The LLC half bridge resonant converter of the proposed circuit supplies the power through the resonance among the leakage and magnetizing inductors of the transformer and series resonant capacitor C_r[13]. In this period, since Y_{pn} is turned off, the resonant tank is not affected by the panel capacitor C_P. When X_r, X_f and X_e are turned on, the secondary side of the LLC half bridge resonant converter is operated as a voltage doubler rectifier composed of Y_S, Y_G and V_e. Therefore, V_e becomes almost equal to $0.5V_S$ and additional devices such as rectifier diodes are not required.

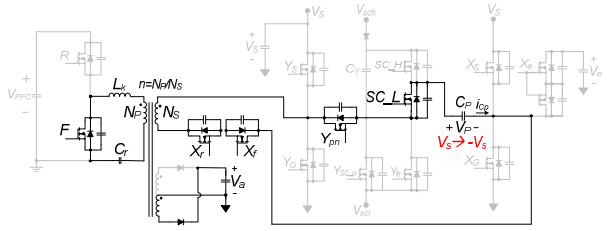
In the meantime, the output voltage V_S of the proposed circuit can be tightly regulated by a PFM method which varies the switching frequency of *R*and *F* according to load condition. Especially, although the number of sustain pulses are small during the full black image, V_S can be tightly controlled because this period accounts for more than 30 percent of one sub-field.

C. Sustain Period

Fig. 8 shows the equivalent circuit of the proposed circuit during sustain period. In this period, the proposed circuit operates as the power supply and ERC. Also it recovers the energy stored in PDP by the resonance between leakage inductor L_k of the transformer and the panel capacitor C_P. Namely, as shown in Fig. 9(g), the proposed circuit builds up i_{Lk} by turning on Y_G and X_G before t_0. Then, if Y_G and X_G are turned off after t_0, the energy stored in C_P is recovered and atthe same time, the voltage across C_P is increased from $-V_S$ to V_S in the manner of the resonance between C_P and L_k with the initial current $i_{Lk}(t_0)$, where the initial current $i_{Lk}(t_0)$ can be adjusted by DT_S. At the same time, the output voltage V_S can be regulated by the difference between *Area I* and *II*, which is varied by the initial current $i_{Lk}(t0)$.



(a) Rising energy recovery transient when *R* is on.



(b) Falling energy recovery transient when *F* is on.

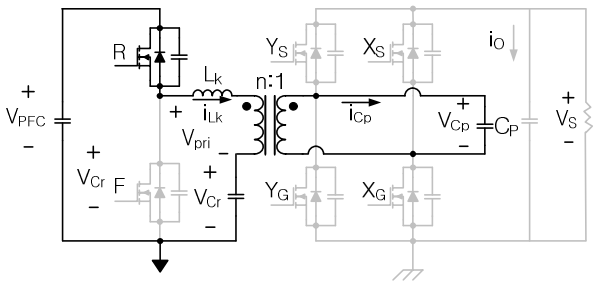
Fig. 8.The equivalent circuit diagram during sustain period.

D. Mode Analysis during Sustain Period

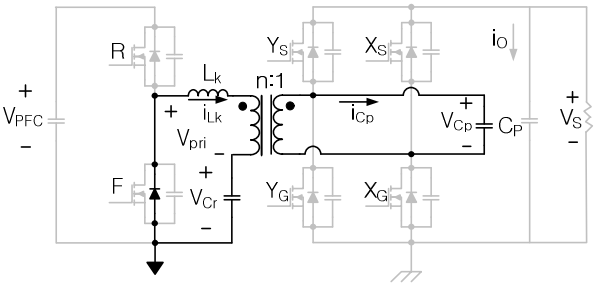
For the convenience of the mode analysis at steady state, several assumptions are made as follows:

- All parasitic components except those specified in Fig. 9 are neglected.
- The input voltage V_{PFC} and sustain voltage V_S are constant.
- The voltage across the series resonant capacitor V_{Cr} is constant as $V_{PFC}/2$.

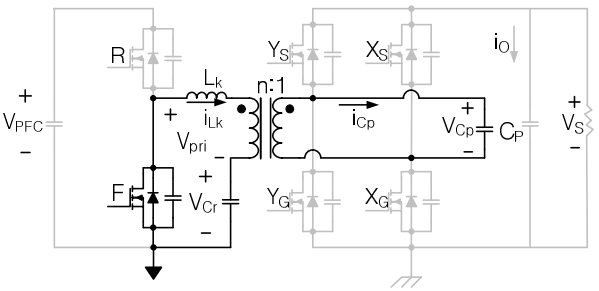
Fig. 9 shows the equivalent circuit diagrams and key waveforms of the proposed circuit at each operation mode during sustain period. One switching cycle can be divided into two half cycles, t_0~t_6 and t_6~t_{12}. Furthermore, since the operations of two half cycles are symmetric, only the first half cycle is explained. Before t_0, the voltage V_{Cp} across C_P is maintained at $-V_S$ with Y_G and X_S conducting. Therefore, the current i_{Lk} is linearly increased.



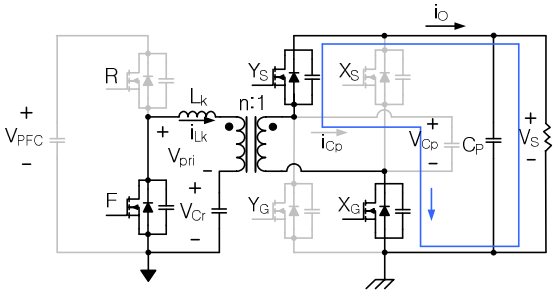
(a) Mode 1.



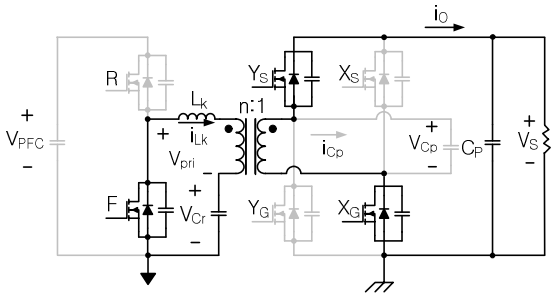
(b) Mode 2.



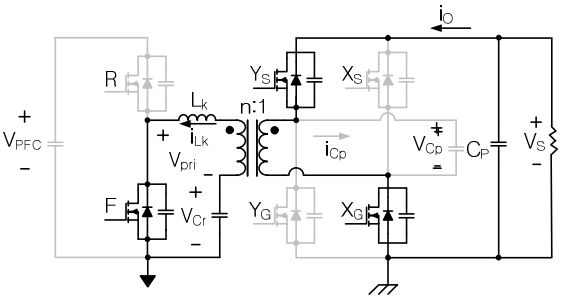
(c) Mode 3.



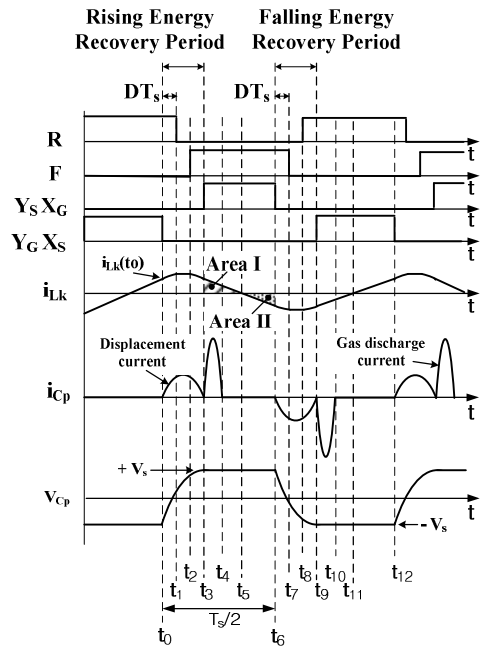
(d) Mode 4.



(e) Mode 5.



(f) Mode 6.



(g) Key waveforms of the proposed circuit during sustain period.

Fig. 9. The equivalent circuit diagrams and key waveforms during sustain period.

Mode 1(t_0-t_1): When Y_G and X_S are turned off at t_0, mode 1 begins and the voltage V_{PFC}–V_{Cr} is applied to the primary side of the transformer (i.e.,V_{pri}) with R conducting as shown in Fig. 9(a). Thus, the voltage V_{Cp} increases by the resonance between C_{eq} (C_{eq}=C_P||C_{YS}||C_{YG}||C_{XS}||C_{XG}) and L_k with the initial condition i_{Lk}=$i_{Lk}(t_0)$. Therefore, the voltage $V_{Cp}(t)$ and the current $i_{Lk}(t)$ can be obtained as follows:

$$V_{Cp}(t) = \frac{n}{L_k C_{eq}}(V_{PFC} + nV_S - V_{Cr}(t_0))(1+\cos At) + \frac{n}{AC_{eq}}\sin At - V_S \quad (2)$$

$$i_{Lk}(t) = \frac{1}{AL_k}(-V_{PFC} + V_{Cr}(t_0) - nV_S)\sin At - i_{Lk}(t_0)\cos At \quad (3)$$

where,

$$n = N_P / N_S,\ A = \sqrt{\frac{n^2 C_r + n^2 C_r C_{eq} + C_{eq}}{L_k C_r C_{eq}}}$$

Mode 2 (t_1-t_2): When R is turned off at t_1, mode 2 begins. As shown in Fig. 9(b), the voltage across F is decreased toward 0V by the resonance between L_k ,C_{eq} and equivalent switch output capacitor $2C_{ds}$. When the voltage across F becomes 0V, F can be turned on with ZVS as shown in Fig. 9(b). At the same time, V_{Cp} is continuously increasing by the resonance between C_{eq} and $L_k$like previous mode 1.

Mode 3 (t_2-t_3): When F is turned on at t_2, mode 3 begins. Since F is turned on, the voltage V_{pri} is maintained at $-V_{Cr}$ as shown in Fig. 9(c). The voltage V_{Cp} is increased by resonance of C_{eq} and L_k. This mode ends at t_3 when V_{Cp} becomes equal to V_S. $V_{Cp}(t)$ and $i_{Lk}(t)$ can be expressed as follows:

$$V_{Cp}(t) = V_S \quad (4)$$

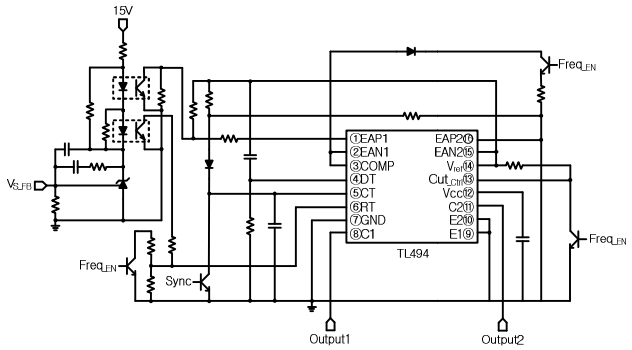
$$i_{Lk}(t) = \frac{1}{BL_k}(V_{Cr}(t_2) + nV_S)\sin Bt - i_{Lk}(t_2)\cos Bt \quad (5)$$

where,

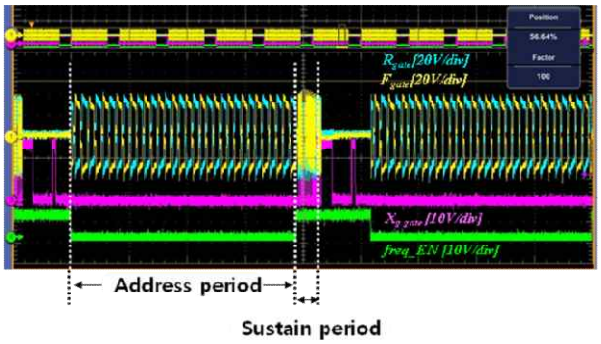
$$n = N_P / N_S,\ A = \sqrt{\frac{1+n^2 C_r}{L_k C_r}}$$

Mode 4 (t_3-t_4): When V_{Cp} is clamped at V_S, the body-diodes of Y_S and X_G are conducted as shown in Fig. 9(d). Since the voltages across Y_S and X_G are 0V, Y_S and X_G can be turned on with ZVS and the voltage across the PDP is sustained at V_S. Therefore, the gas discharge of the PDP is ignited at this point. BecauseV_{pri} is maintained at $-V_{Cr}$, the current i_{Lk} of leakage inductor begins to linearly decrease with the slope of $-(V_{Cr}+nV_S)/L_k$.

Mode 5(t_4-t_5): At this mode, the input power is transferred to the output side as a powering phase. Since Y_S and X_G are conducting as shown in Fig. 9(e), the voltage across C_P is



(a) Control block diagram.



(b) Waveforms of gate signal of *R* and *F*.

Fig. 10.Control block diagram of the proposed circuit and waveforms of gate signal of R and F.

maintained at V_S. Like mode 4, i_{Lk} is linearly decreased with the slope of $-(V_{Cr}+nV_S)/L_k$.

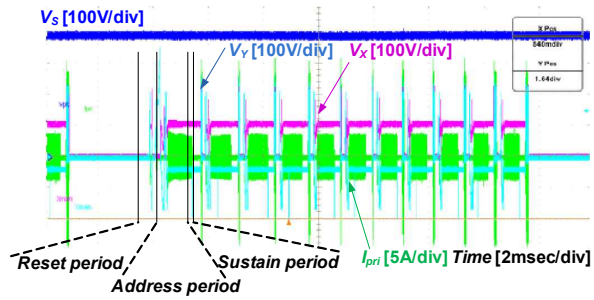
Mode 6 (t_5-t_6): When the direction of i_{Lk} is reversed, mode 6 begins as shown in Fig. 9(f). At this mode, the current i_{Lk} through L_k is built-up to recover the energy stored in the PDP at next half cycle. This mode ends at t_6 when Y_S and X_G are turned off.

The circuit operation of t_6-t_{12} is similar to that of t_0-t_6. Subsequently, the operation from t_0 to t_{12} is repeated.

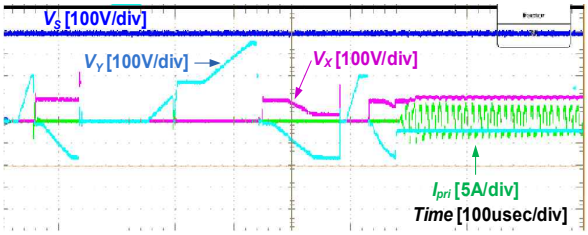
III. EXPERIMENTAL RESULTS

To confirm the operation validity and features of the proposed circuit, a prototype for 42-inch PDP is implemented with following specifications.

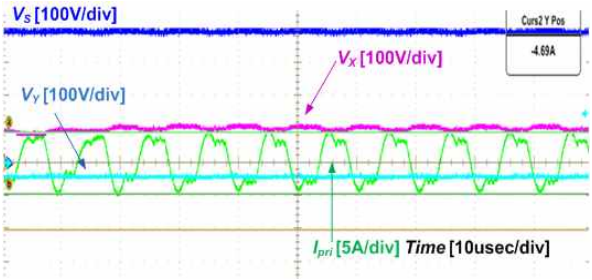
- V_{PFC} : $390V_{dc}$
- Display condition : Full White Pattern
- Number of turns : N_P:N_S=36:12
- Resonant tank : L_m - 160uH, L_k- 20uH, C_r - 12nF
- Switching frequency during address period : 90kHz
- Switching frequency during sustain period : 250kHz
- Rising and falling time for ERC : 700nsec
- Sustain voltage V_S : $207V_{dc}$
- Address voltage V_a : $55V_{dc}$
- V_e : $91V_{dc}$



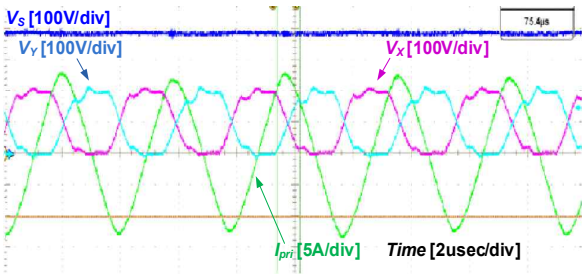
(a) 1TV-field.



(b) During Reset Period.



(c) During Address Period.



(d) During Sustain Period.

Fig. 11.Experimental waveforms of the proposed circuit.

- V_{set} : $150V_{dc}$
- V_{scl} : $-190V_{dc}$
- V_{sch} : $-36V_{dc}$

As shown in Fig. 10(a), the PFM during address period and PWM during sustain period are implemented with one PWM IC TL494, where switching frequency of *R* and *F* can be varied by sourcing and sinking current of R_T terminal (pin 6). TL494 operates as push-pull mode by applying V_{ref} to CTRL terminal pin (pin 13) during address period. On the other hand, it operates as single-ended mode by applying 0V to CTRLterminal during sustain period. From the above-mentioned configurations, as shown in Fig. 10(b), each gate signal can be generated. Fig. 11(a) shows that the 1-TV field is composed of 11 sub-fields and each sub-field consists

TABLE I

COMPARISONS OF MEASURED INPUT POWER CONSUMPTION

Items	Conventional system	Proposed system
Input power	207W	203W

(Test conditions V_{in}=220V_{ac}(*60Hz*), full white pattern, measured after 1hour aging)

TABLE II

COMPARISONS BETWEEN CONVENTIONAL AND PROPOSED PDP SYSTEM IN THE ASPECT OF THE NUMBER OF DEVICES

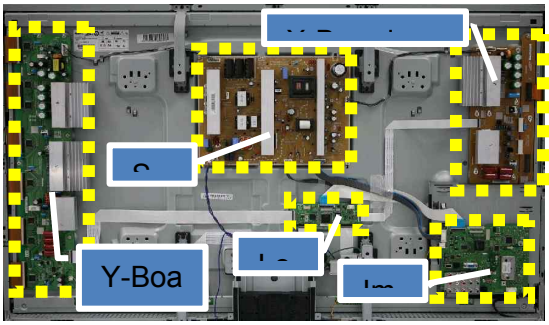
Items		Conventional system	Proposed system
Primary Switch	M1 & M2 (R & F)	2EA (FDPF16N50)	2EA (FDPF16N50)
Secondary Switch	Y_S, Y_G X_S, X_G	4EA (RJH30A3)	4EA (RJH30E2)
	Y_r, Y_f	2EA (FGPF50N33)	-
	X_r, X_f	2EA (FGPF50N33)	2EA(FGA70N33)
Diode	D_{YCH}, D_{YCL}	2EA (FCU10CU30)	-
	D_{XCH}, D_{XCL}	2EA (FCU10CU30)	
	D_{Yr}, D_{Yf}	2EA (FSU5A40)	
	$D_{Xr}D_{Xf}$	2EA (FSU5A40)	
energy recovery inductor		2EA	-
energy recovery capacitor	C_{Yerc}, C_{Xerc}	2EA (1kV)	-

of the reset, address, and sustain periods.Fig. 11(b) and (c) show the key waveformsduring reset and address period, respectively. As shown in this figure, the proposed circuit transfers the input power to each output side by resonance between L_k and C_r and each output voltage can be well regulated. Fig. 11(d) shows the key waveforms during sustain period. As shown in this figure, the proposed circuit can successfully recover the energy stored in the PDP without hard switching operation.

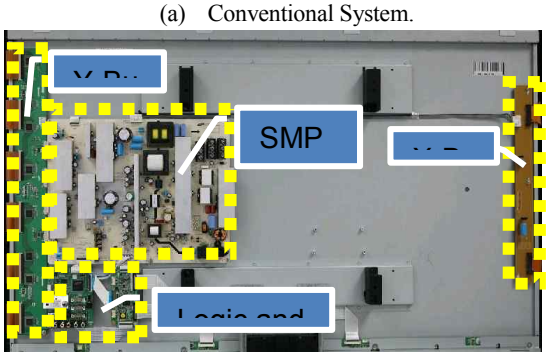
Table I, II and Fig 12 show the comparison of the conventional system and the proposed system. Also Fig. 12 shows advantages such as a simple structure, less mass, fewer devices.

Table I shows the comparative results of the measured input power consumption. As shown in this table, the proposed PDP system has smaller power consumption than the conventional system by about 4W under the same conditions. As mentioned above, the conventional PDP system consists of two-stages as DC/DC and driving stages. On the other hand, since the proposed circuit is composed of only one power conversion stage. Therefore, the proposed PDP system features better efficiency than the conventional system.

Table II shows a comparison between conventional and the proposed circuit in terms of the number of devices. As shown in this table, since the proposed circuit can remove the largenumber of expensive devices such as power switches, diodes, inductors and energy recovery capacitors, it features a simpler structure, less mass and lower cost of production.



(a) Conventional System.



(b) Proposed System.

Fig. 12.SMPS and Sustain Drivers for 42-inch PDP.

IV. CONCLUSIONS

A new sustainer with primary sided integration of DC-DC converters and energy recovery (SPIDER) circuits for AC PDP has been presented to overcome the drawbacks of conventional circuits. Since the removal of rectifier diodes and auxiliary X and Y ERCs of the conventional PDP system is possible, it features a much simpler structure and lower cost. Moreover, the ZVS of primary side switches (*R*, *F*) cannot only be guaranteed by a large leakage inductor, but those of secondary side switches can also be ensured by energy recovery operation. Nevertheless, the proposed circuit can satisfactorily recover the energy stored in the PDP and regulate each output voltage at the same time. To control the proposed circuit, the PFM and PWM are implemented with only one control IC during address and sustain periods, respectively. To confirm the validity and superiority of the proposed circuit, a prototype for 42-inch PDP is implemented. As a result, the proposed system has smaller power consumption than the conventional system by about 4W with the less number of devices. Therefore, the proposed circuit is expected to enhance competitiveness in flat panel display market.

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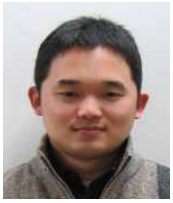
Jae-Sung Park received the B.S. and M.S. degrees in electrical engineering from Kookmin University,Seoul, Korea, in 2009 and 2011, respectively, wherehe is currently working toward the Ph.D. degree. His current research interests include light-emitting diode drivers, analysis, design, and digital control of power converters.



Yong-Saeng Shin received the B.S. and M.S. degrees in electrical engineering from Kookmin University, Seoul, Korea, in 2007 and 2009, respectively, where he is currently working toward the Ph.D. degree. His current research interests include analysis, modeling, design, and control of power converters.

Sung-Soo Hong(S'88-M'94) received the B.S. degree in electrical engineering from Seoul National University, Seoul, Korea, in 1980, and the M.S. and Ph.D. degrees in electrical and electronics engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1986 and 1992, respectively. From 1984 to 1998, he was an electronics engineer with Hyundai Electronics Company. In 1993, he was with Virginia Polytechnic Institute and State University, Blacksburg, as a Research Scientist. Since 1999, he has been a Professor in the Department of Electrical Engineering, Kookmin University, Seoul, Korea, and has worked for Samsung Power Electronics Center and Samsung Network Power Center as a Research Fellow. His current research interests include modeling and control techniques for power converters, power conditioning system for the renewable energy, and EMI analysis and reduction techniques for power electronics circuits.

Sang-Kyoo Han(S'04-M'10) received the B.S. degree in electrical engineering from Pusan National University, Pusan, Korea, in 1999, and the M.S. and Ph.D. degrees in electrical engineering and computer science from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2001 and 2005, respectively. For the next six months, he was a Postdoctoral Fellow with KAIST, where he developed digital display power circuits and performed several research activities. Since 2005, he has been an Associate Professor in the Department of Electrical Engineering, Kookmin University, Seoul, Korea, and has worked for Samsung Power Electronics Center and Samsung Network Power Center as a Research Fellow. His current research interests include power converter topologies, power factor contention converters, light-emitting diode drivers, renewable energy system, and battery charger for electric vehicle. Dr. Han is a member of the Korean Institute of Power Electronics.

Chung-Wook Roh(S'98-M'01) received the B.S., M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1993, 1995 and 2000, respectively. In 2000, he joined the Digital Media Network Division, Samsung Electronics Company, Suwon, Korea, where he was a Project Leader of the Plasma Display Driver Development Team. Since 2004, he has beenan Associate Professor in the Department of Electrical Engineering, Kookmin University, Seoul, Korea, and has worked for Samsung Power Electronics Center as a Research Fellow and for Samsung Electronics Company as a consultant. His current research interests include driver circuits for plasma display panels, modeling, design and control of power conversion circuits, soft-switching power converters, resonant inverters and electric drive systems. Dr. Roh is a member of the Korean Institute of Power Electronics.