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Process Considerations for 80-GHz High-Performance *p-i-n* Silicon Photodetector for Optical Interconnect

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Abstract—**In this work, design considerations for high-performance silicon photodetector are thoroughly investi- gated. Besides the critical dimensions of device, guidelines for process architecture are suggested. Abiding by those criteria for improving both direct-current (DC) and alternating-current (AC) perfor- mances, a high-speed low-operation power silicon photodetector based on *p-i-n* structure for optical interconnect has been designed by device simulation. An f_{-3dB} of 80 GHz at an operating voltage of 1 V was obtained.**

Index Terms—**Silicon photodetector, *p-i-n* structure, optical interconnect, device simulation**

I. INTRODUCTION

Optical interconnect is gaining more popularity as a next-generation interconnect technology for the highly integrated circuits (ICs) due to its capability of minimizing *RC*-delay, power consumption, and heat dissipation [1]. It has a very wide range of applications from device/chip/board-level interconnects up to teleco- mmunication systems. Optical interconnect includes not only the waveguide itself but also light-emitting diode (LED) or laser as the light source, modulator, and photodetector. Integration on silicon (Si) substrate is strongly pursued owing to cost-effectiveness and complementary metal-oxide-semiconductor (CMOS) process compatibility [2-6], which makes it essential to exploit Si-compatible materials, structures, and process architecture highly suitable to integration with Si ICs.

In this work, a high-performance *p-i-n* photodetector for optical interconnect is designed to have 80-giga hertz (GHz) cut-off frequency (f_{-3dB}) and device performance dependence on process parameters are closely investigated.

II. DEVICE STRUCTURE AND SIMULATION

Fig. 1(a) and (b) schematically show the ways that photodetectors are coupled to the waveguides in the optoelectronic integrated circuits (OEICs) eventually.

The pass-through type operated by evanescent wave coupling is known to have higher responsivity compared with butt-coupled type [1, 7, 8]. The former type is more strategic to achieve highly-scaled OEICs, especi- ally when it comes to a design for cooperating with processor and memory cores at a comparable integration level or a large number of interaction routes. Also, the responsivity of the former can be enhanced by design as a function of device length (in the waveguide direction), which is another merit of the vertically coupled photode- tector.

Being initiated by a couple of motivations above, two-dimensional (2-D) simulation works have been performed to design and characterize *p-i-n* Si photode- tector [9], aiming the vertical integration. For convenience in the simulation and evaluation, beam line with a power of 1 W/cm^2 incident from the top has been assumed throughout the simulation works. The effects of anode junction depth (X_{aj}), cathode junction depth (X_{cj}), width and thickness of device cross-section (shown in

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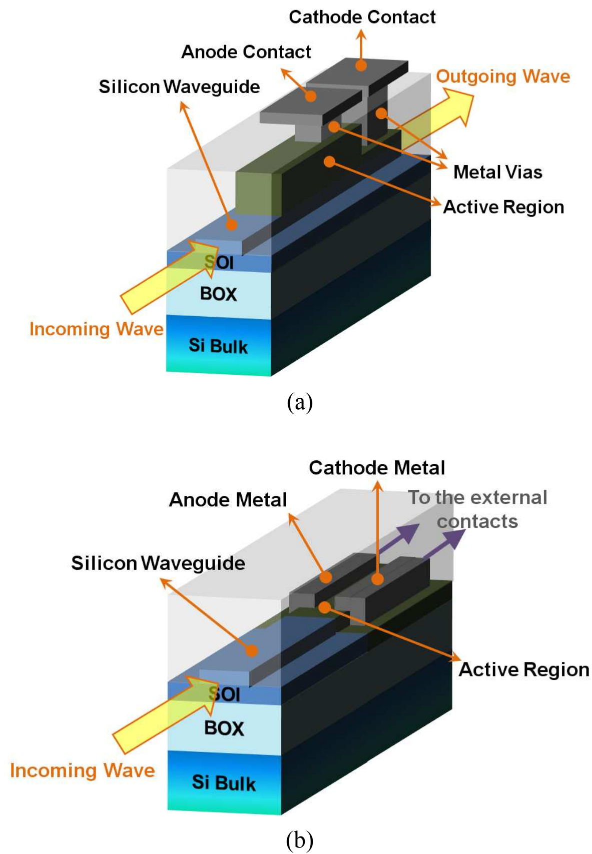


Fig. 1. Waveguide-coupled photodetectors (a) Evanescent-coupling (vertical), (b) butt-coupling type (in-plane).

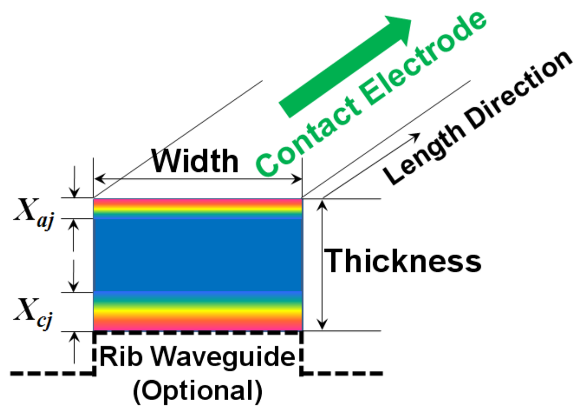


Fig. 2. Design parameters in the 2-D simulation works.

Fig. 2) on direct-current (DC) and alternating-current (AC) performances – largely on photocurrent and speed – have been investigated. The length in the 2-D simulations was invariable and fixed to a unit value of 1 μm. Total photocurrent can be simply scaled up according to the actual device length. *p-i-n* diode photodetector has a response time of 10^{-10}–10^{-8} s, which is suitable for high-speed photodetector [10]. Also, device performances can be easily controlled by adjusting the thickness of intrinsic region, with securing robustness against other process fluctuations.

For higher simulation accuracy and reliability, multiple models including Shockley-Read-Hall recombination model, Auger recombination model, concentration and field-dependent mobility models, band-to-band tunneling model, and quantum-effect model were combined in use.

III. SIMULATION RESULTS

1. DC Characteristics

It was assumed that p^+ anode, intrinsic region, and n^+ cathode were epitaxially grown in order to minimize unrecovered lattice damages by ion implantation and to predict the doping profile more tangibly. Thus, more strictly speaking, anode junction depth (X_{aj}) consists of two parts: thickness of epitaxial Si layer with constant n^+ *in situ* doping and doping gradient length. The epitaxial layer thickness is termed as anode thickness in Fig. 3, where its effect on cathode current (I_C) can be studied. The doping of the layer was arsenic (As) 1×10^{20} cm^{-3} and the doping gradient length (distance from As 1×10^{20} cm^{-3} to 1×10^{12} cm^{-3} in the Gaussian distribution) was kept to be 100 nm. The effect of anode thickness on I_C was not significant. As the epitaxial layer gets thick, increases in the currents were observed since there was increase in the number of optically generated electrons in the

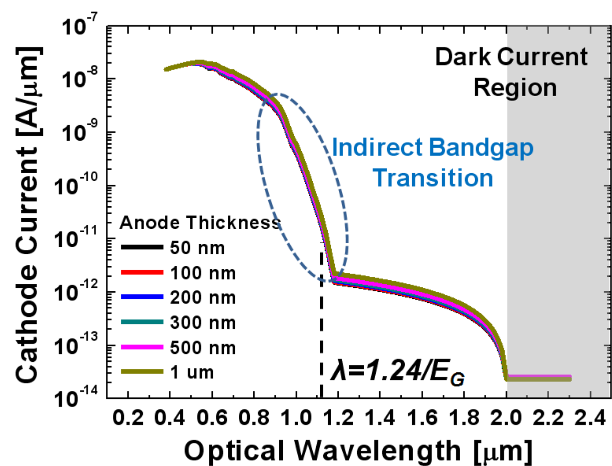


Fig. 3. Cathode current (I_C) versus optical wavelength (λ) at different anode thicknesses (gradient length=100 nm).

thickened layer, but the amount was negligibly small as shown in Fig. 3. The cathode thickness and its doping gradient length were kept to be constant as 200 nm and 100 nm (X_{cj} = 300 nm).

For the following simulation results, anode and cathode thicknesses were made 50 nm and 200 nm, respectively. While an external contact can be directly made on anode, there should be an accompanying isotropic etch to form the cathode contact, as could be predicted by Fig. 1(a). Since there is no significant effect of junction thickness on photocurrent (Fig. 3), the anode can be made thin to reduce material growth time, but the cathode was made thick enough (200 nm) including a margin for the etching.

It is confirmed from Fig. 3 that a large amount of photocurrent occurs by a light with energy higher that the bandgap energy (E_G) of Si (=1.12 eV), or equivalently, a light with optical wavelength shorter than λ=1.24/E_G = 1.11 μm. Dark current of a photodetector is defined as the leakage diode current under an operating reverse bias with no optical source. It can be also checked in Fig. 3 at the region of very long wavelength, which is about 10 fA/μm. There is small amount of current starting from λ = 2 μm down to λ=1.2 μm. A wavelength of 2 μm does not have a specific meaning that can be inferred from energy-band structure of Si. The current is resulted from instantaneous excitation by an optical energy smaller than 1.12 eV and simultaneous tunneling into the conduction band of n^+ Si region by a high electric field, which is called optically-assisted band-to-band tunneling. The reverse bias (V_R) was 2 V and the thickness of intrinsic Si was 1 μm for all cases in Fig. 3. Thus, the resulting electric field is 2×10^4 V/cm. If well-designed peripheral circuits for amplifying the photocurrent are accompanied, Si light source and Si detector can be paired. However, due to the slow increase in photogeneration near the energy bandgap of Si, an indirect bandgap material, a light source with energy larger than E_G of Si, can be desirable to be targeted.

Fig. 4(a) and (b) show the cathode current as a function of optical wavelength under different bias conditions. The cathode currents in the regions governed by the optical excitation (below λ=2 μm) are not dependent on V_R. Only the dark current is increased with V_R since it is mainly composed of reverse current of *p-i-n* diode when there is no photogeneration, as shown in Fig.

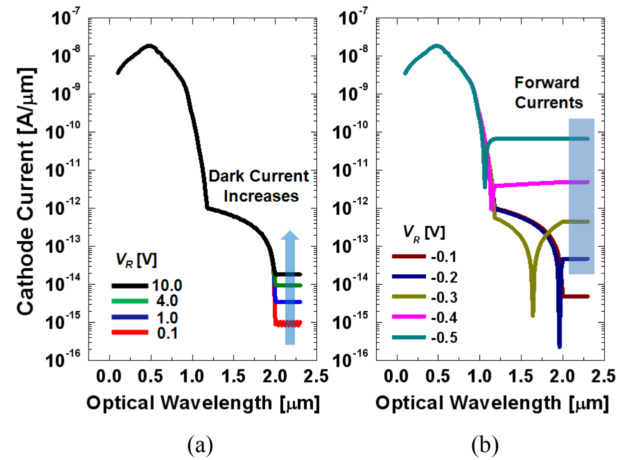


Fig. 4. I_C-λ curves under (a) reverse, (b) forward biases (Thickness of intrinsic Si=1 μm, doping gradient length=50 nm).

4(a). When a negative V_R (forward bias, V_F) is applied, forward current becomes prominent, which is represented by the flat regions in I_C-λ curves shown in Fig. 4(b). The change in current polarity occurs at the dips. The larger the V_F (-V_R=|V_R|) is, the less sensitive the device becomes for longer wavelength lights: narrower window of sensible wavelengths is opened as the V_F is increased while the photocurrent is buried in the forward current and is not observable any more. However, it is noticeable that V_F smaller than 0.3 V is in a permissible range since the forward current does not exceed the photocurrent near λ=1.2 μm and the Si photodetector is still distinguishably responsive to the lights of energies larger than Si E_G.

It is confirmed that *p-i-n* Si photodetector has a wide operation voltage window, including even a small forward bias, and its DC characteristics are not dependent on voltage magnitude under reverse bias conditions. The merit is secured by controlling the thickness of intrinsic Si layer and potentially leads to low-power operation.

As previously mentioned, it is desirable to grow the layers epitaxially with *in situ* doping to minimize lattice damages by ion implantation and unwanted dopant diffusions distorting the junction locations by a following rapid thermal annealing (RTA) process. Fig. 5 shows the effect of doping gradient length on I_C. The doping gradient lengths were assumed to be the same for anode and cathode junctions. For a device with abrupt junctions, a significant amount of leakage current by band-to-band

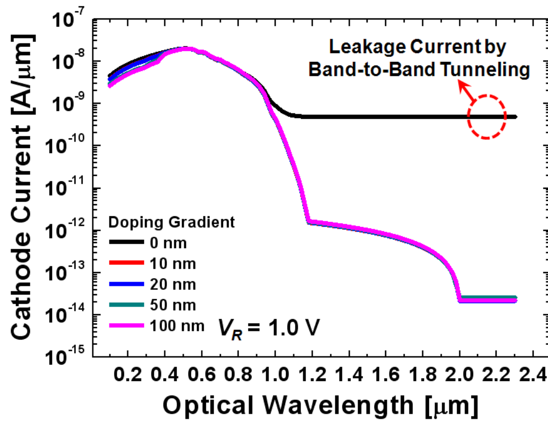


Fig. 5. Cathode currents at different doping gradient lengths (Thickness of intrinsic Si=1 μm, V_R=1 V).

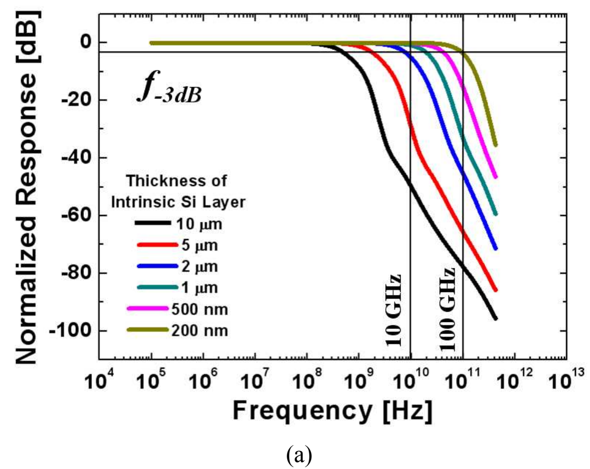
tunneling is observed. Even a doping gradient length as short as 10 nm is effectual in suppressing the leakage current by widening the effective tunneling length. Dependence of I_C on doping gradient length is not so prominent but I_C is slightly reduced as the length gets wider due to the resistance of the elongated region. Although the layers are assumed to be grown by epitaxy, it should be valuable to take the effects of doping gradient length into account when designing thermal budgets either in the material growth or the additional annealing process.

2. AC Characteristics

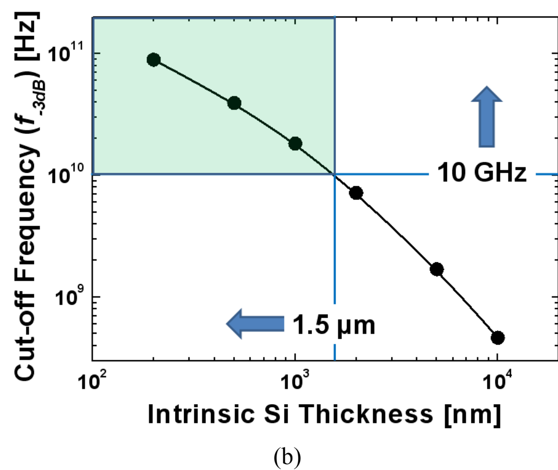
In the previous section, DC characteristics of the *p-i-n* Si photodetector depending on several critical dimensions were investigated. Since the carriers require a finite time to traverse the intrinsic layer, a phase difference between the photon flux and the photocurrent will appear when the incident light intensity is modulated rapidly. Some critical dimensions of device affects the AC characteristics.

Among the parameters that can be taken into consideration, thickness of the Si intrinsic layer was omitted by intent. It physically appears as the distance between anode and cathode electrodes, which is closely related with transit time of the photo-generated electrons. Thus, optimizing process in terms of AC performances rather than DC characteristics would be more decisive if the device is intended for high-speed application in the optical interconnect. For DC characteristics, it is predictable that photocurrent would decrease as the intrinsic layer gets thinner due to volume reduction for photogeneration since the layers are assumed to be grown vertically and the two electrodes are also stacked.

Fig. 6(a) and (b) demonstrate the AC characteristics of the photodetector with different thicknesses of intrinsic Si layers. Each simulation was performed under a condition with V_R=2.0 V, DC and AC beam powers = 1 W/cm^2 and 2 mW/cm^2, respectively. The wavelength of incident light, λ=1 μm, was arbitrarily selected from a sensible wavelength range. The thickness was varied from 10 μm down to 200 nm with a doping gradient length of 50 nm. The cut-off frequency (f_{-3dB}) increased monotonically as the intrinsic layer got thinner, as shown in Fig. 6(a). The frequency response of the photodetector reveals that it shows characteristics of low-pass filter (LPF), so f_{-3dB} can be equivalently understood as its bandwidth (BW). Fig. 6(b) depicts f_{-3dB}'s as a function of



(a)



(b)

Fig. 6. Frequency response of the *p-i-n* Si photodetector (a) Normalized response, (b) f_{-3dB} versus intrinsic Si thickness.

the thickness, from which it is revealed that the intrinsic layer should be 1.5 μm or thinner to have a BW wider than 10 GHz. For an ultrafast operation of near-100 GHz, the intrinsic Si layer should not be thicker than 200 nm. Reduction in photo-current is expected in a thin device but it can be enhanced by scaling-up in the length direction keeping the thickness as designed for achieving a specific speed.

Fig. 7 demonstrates the dependence of f_{-3dB} on V_R and doping gradient length simultaneously. Higher V_R results in higher electric field and electron drift velocity ($\boldsymbol{v}_d$), by which the response of the photodetector becomes faster. The thickness of intrinsic Si layer was 2 μm in Fig. 7, so 5.0-V V_R is equivalent to an electric field of 2.5×10^4 V/cm, where $\boldsymbol{v}_d$ reaches 90% of the saturation velocity ($\boldsymbol{v}_{sat}$). From a viewpoint of AC performance, a doping gradient length needs to be 20 nm or longer. With a doping gradient length shorter than this value, negative currents were induced in the high-frequency region, which means that the photocurrent lags behind the photo-flux by π rad.

This complements the results that a nonnegative doping profile is necessary for prevent band-to-band tunneling leakage from occurring in the DC performance. The influence of doping gradient length is not predominant to f_{-3dB} as can be confirmed in Fig. 7. However, it should be reminded that an upper limit is indispensible for minimizing the loss of DC photocurrent. Table 1 summarizes the specifications of a high-speed low-operation power Si photodetector designed by the criteria.

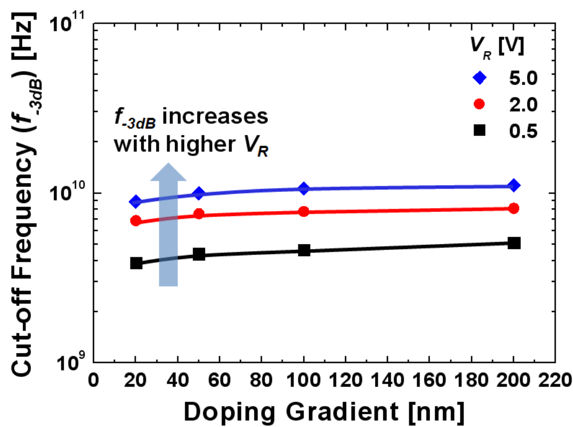


Fig. 7. Bias and doping gradient length effects on AC performance.

Table 1. Specifications of the designed *p-i-n* Si photodetector

Design Parameters	Values
Process Parameters	
Anode Layer Thickness	50 nm
Anode Doping Gradient Length	20 nm
Intrinsic Layer Thickness	200 nm
Cathode Doping Gradient Length	20 nm
Cathode Layer Thickness	200 nm
Device Width	5 μm
Device Length (Unit Length)	1 μm
DC and AC Performances	
Operation Voltage	1 V
Photocurrent (Unit Length)	17 nA
Bandwidth (1 V)	80.1 GHz
Bandwidth (5 V)	84.9 GHz
Responsivity (Unit Length)	0.34 A/W
Dark Current (Unit Length)	1.39 fA

IV. CONCLUSIONS

Photodetector is one of the core components for optical interconnect. Silicon-on-insulator (SOI) is a good platform for Si photonics by virtue of the efficient optical confinement by the large difference in refractive indices of Si and SiO_2. For this reason, we assumed the SOI platform to carry out this study. However, exploiting new material systems adoptable for its realization on bulk-silicon for cost-effective technologies and more viable integration with complementary metal-semiconductor-oxide (CMOS)-based circuits needs to be pursued in parallel. Process parameters and critical dimensions for high-performance *p-i-n* Si photodetector and their effects have been thoroughly investigated. Abiding by the design rules, a high-speed low-power operating device has been designed by series of device simulations. f_{-3dB} of 80.1 GHz and responsivity of 0.34 A/W (which is converted to a quantum efficiency of 0.81) obtained from the designed photodetector with unit length at 1-V operating voltage.

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