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A Subthreshold Slope and Low-frequency Noise Characteristics in Charge Trap Flash Memories with Gate-All-Around and Planar Structure

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Abstract—**The causes of showing different subthreshold slopes (SS) in programmed and erased states for two different charge trap flash (CTF) memory devices, SONOS type flash memory with gate-all-around (GAA) structure and TANOS type NAND flash memory with planar structure were investigated. To analyze the difference in SSs, TCAD simulation and low-frequency noise (LFN) measurement were fulfilled. The device simulation was performed to compare SSs considering the gate electric field effect to the channel and to check the localized trapped charge distribution effect in nitride layer while the comparison of noise power spectrum was carried out to inspect the generation of interface traps (N_{IT}). When each cell in the measured two memory devices is erased, the normalized LFN power is increased by one order of magnitude, which is attributed to the generation of N_{IT} originated by the movement of hydrogen species (h^*) from the interface. As a result, the SS is degraded for the GAA SONOS memory device when erased where the N_{IT} generation is a prominent factor. However, the TANOS memory cell is relatively immune to the SS degradation effect induced by the generated N_{IT}.**

Index Terms—**Subthreshold slope (SS), charge trap flash (CTF) memory, gate-all-around (GAA), low-frequency noise, interface trap (N_{IT})**

I. INTRODUCTION

The differential demands for high density non-volatile memories with low-cost process have strongly increased in the last decade. However, today the scaling of standard planar flash structures having floating gate seems to face serious limitations, due to the loss of memory cell electrostatic integrity and the appearance of parasitic inter-coupling between adjacent cells in the arrays [1]. In addition, since the tunneling oxide thickness in floating gate memory devices is relatively thick to suppress the stress induced leakage current (SILC), the high voltages are required for the write and erase operations [2].

In order to overcome these issues, charge trap flash (CTF) memories have been proposed as one of the most promising candidates for the next generation NAND flash technology. As an example, SONOS type flash memory based on a gate–all-around (GAA) structure has strong gate controllability and suppressed short channel effect due the merits of GAA structure even in the ultimately scaled regime [3, 4]. TANOS CTF memory with planar channel structure has a better program/erase speed and it is enable to decrease a backward tunneling current by using high-k dielectric material (Al_2O_3) and metal gate (TaN) compared to SONOS based CTF memories [5]. They are examples as substitutes for floating gate type flash memory while still have a

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reliability issue such as the data retention.

On the other hand, subthreshold slope (SS) of a read current in a NAND flash memory cell is different depending on the cell state. In other words, the SS is changed when the cell is programmed or erased and cycled. In addition, overlap length between the source/drain and the gate affects the SS variation. Several authors have reported about the causes of the SS changes in the NAND flash memories, but comprehensive understanding of them are still missing [6-8]. Thus, more detailed analysis should be made for clear understanding.

In this paper, we investigate SS characteristics in the I_D-V_G (or I_{BL}-V_{read}) curves of the SONOS GAA and the TANOS planar CTF devices to analyze of their SS variation when they are programmed and causes. To analyze the cause clearly, 2-D device simulation [16] and measurement of low-frequency noise (LFN) power were performed. Since the LFN characteristic reflects generated interface traps (N_{IT}) near the interface between the channel and the tunneling oxide, we can improve accuracy in the analysis of the SS variation.

II. Experimental Procedure

Fig. 1(a) and (b) show the cross sectional SEM image of Si-nanowire stacked array cells having GAA structure [9] and the cross sectional profiles with bit-line (BL) and word-line (WL) directions for TANOS based CTF cells [10], respectively. I-V measurement of the devices was carried out with 4155C (Agilent) for comparing SSs. The systematic setups for noise measurement are presented in Fig. 2(a) and (b) for each device. The noise measurement was performed with an arbitrary unit cell for the SONOS GAA CTF memory while for the TANOS planar CTF memory a cell in a string was randomly selected where all of the unselected (or pass) cells were erased. In the case of the TANOS based NAND flash memory devices, the read voltages and pass voltages were applied to a selected cell and unselected cells, respectively. Since the selected cell determines the bit-line current in a cell string, the noise in the current attributes to the selected cell [11]. The low-frequency noise measurement was carried out with the low noise current amplifier (SR570) and dynamic signal analyzer (Agilent 35670A). The devices were measured in a shield chamber at room temperature.

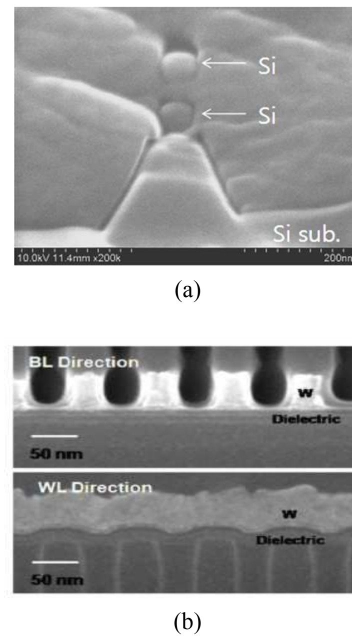


Fig. 1. (a) Cross sectional FESEM image of the SONOS GAA nanowire flash memory, (b) cross sectional TEM profiles of the TANOS based CTF memory with BL and WL directions.

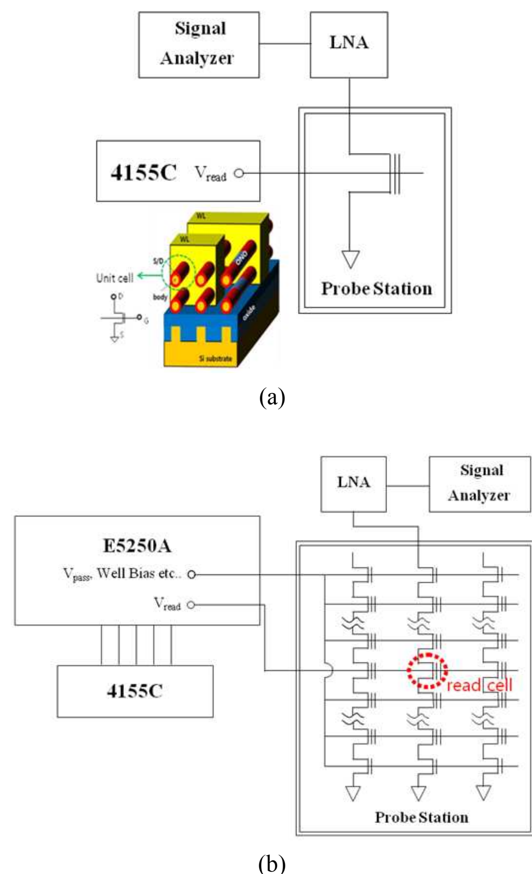


Fig. 2. Schematic view of noise measurement setup for (a) GAA nanowire flash memory unit cell, (b) TANOS based CTF memory cell in a string.

III. RESULTS AND DISCUSSION

The representative I_D-V_G characteristics in initial, programmed and erased states are depicted for two different kinds of the flash memories, SONOS GAA and TANOS planar CTF memories as shown in Fig. 3(a) and (b), respectively. For program and erase operations, 9 V for 1μs and -10 V for 10 μs were applied to the former while 14 V for 100 μs and -16 V for 1ms were applied to the latter. In addition, each value of the subthreshold slopes $[SS=(d\log I_D/dV_G)^{-1}]$ in programmed and erased states was extracted as denoted next to each I_D-V_G lines as shown in Fig. 3(a) and (b).

Comparing the SSs in programmed and erased states in each device, the SS in erased state is larger than that in programmed state in the GAA SONOS CTF memory unit

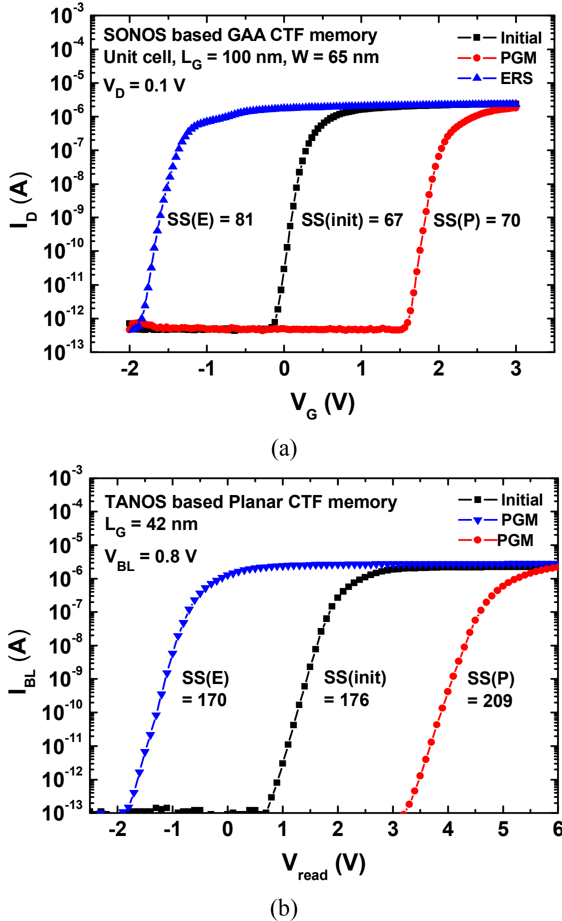


Fig. 3. I_D-V_G curves in initial, programmed and erased states for (a) the SONOS based GAA nanowire CTF memory, (b) the TANOS based planar CTF flash memory. The SSs (mV/dec) shown next to each I_D-V_G curve are extracted by linear fit in subthreshold region.

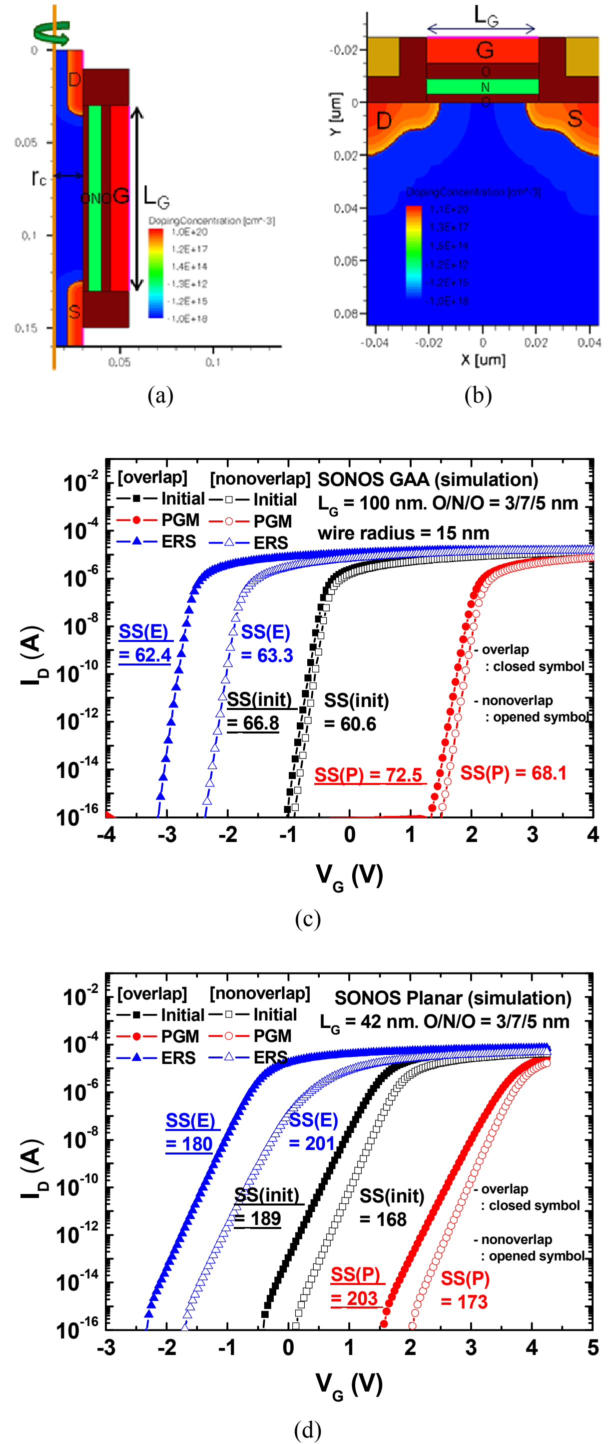


Fig. 4. 2D simulated device structures of SONOS memory cells with (a) GAA, (b) planar architecture, and their I_D-V_G curves are presented according to the cell state and 5 nm of S/D overlap condition in (c) and (d), respectively. SSs (mV/dec) are extracted from the simulated I_D-V_G curves as shown beside each plot. SSs of the S/D overlap (5 nm) structure are underlined for classification.

cell as exhibited in Fig. 3(a), whereas the opposite characteristics are displayed in the TANOS CTF memory device. The reported I-V characteristics for CTF memories adopting GAA and planar structures show more degraded SSs in programmed state [12, 13].

For detailed analysis, SSs in the programmed and erased states were compared in GAA and planar SONOS cells by utilizing TCAD simulation tool [14]. Fig. 4(a) and (b) show simulated device structures and their I_D-V_G characteristics with extracted SSs depending on the cell state and source/drain overlap condition are depicted in Fig. 4(c) and (d). The trap densities in nitride layer were defined as 4×10^{19} cm^{-3} for the planar SONOS device and 1×10^{20} cm^{-3} for the GAA SONOS device with uniform trap distributions which are in a proper range of values [15-17]. The tunnel-oxide, nitride, blocking-oxide thickness are 3, 7 and 5 nm, respectively. The body doping concentration is 1×10^{18} ions/cm^3 in common for the two devices. The gate length is 42 nm for the planar SONOS cell but 100 nm for GAA SONOS cell. The silicon radius of the GAA SONOS device is 15 nm [9]. Here, the nonoverlap length is 5 nm for both devices. The I_D-V_G curves of the devices with source/drain overlapped structure are given by solid symbols. From the simulated I_D-V_G plots, the SSs in programmed state are larger compared to those in erased state for both devices except for the planar SONOS device with source/drain nonoverlap structure. It can be explained by a short channel effect induced by a nonuniformly trapped charge distribution in nitride layer. The programmed charge density in the nitride layer shows a peak near the center region of the channel and decreases going to the both edges. This kind of nonuniform distribution comes from normal program operation in which the electric field responsible for the FN (Fowler Nordheim) tunneling is weaker near both edges due to a fringing electric field. Thus, the V_{th} near the center region of the channel is a bit higher than those in the channel edges. This means that an effective channel length of the device is shorter than the physical gate length. For this reason, the I_D (or I_{BL}) is affected more easily by the drain (or bit-line) bias, which is called DIBL (drain-induced barrier-lowering). This explanation was confirmed by the simulation result which was obtained from the SONOS devices with gate lengths of 42 nm and 1 μm. SS degradation of the 1 μm device is negligible as shown in Fig. 5. The gate bias

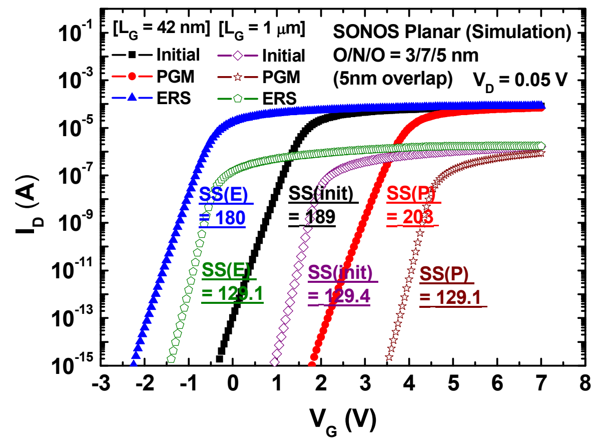
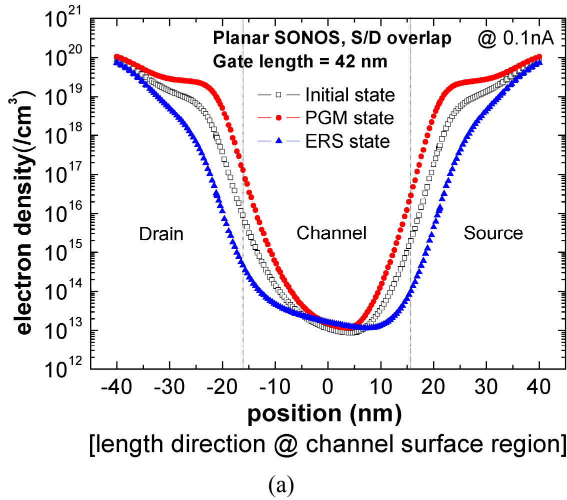


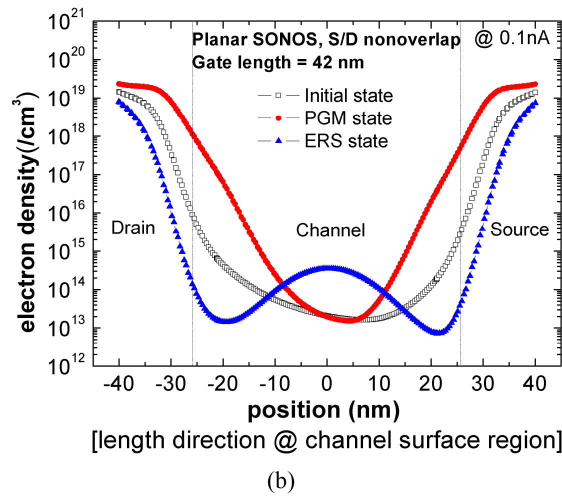
Fig. 5. 2D TCAD simulated I_D-V_G curves in initial, programmed and erased states for the planar SONOS devices with 42 nm and 1μm. SSs are extracted in each plot.

applied to read I_D-V_G curves of a cell makes the electric field in the channel, and the field intensity is different for different cell states (program and erase). The electric field in the programmed cell is stronger near the edge parts of the channel than that of the erased cell due to the lower charge near the edge regions at a fixed channel current. The distribution of the electric field is reflected in that of the electron charge density, and the distributions for two different cells along the channel are shown in Fig. 6 and 7. As shown in these figures, effective channel length is shorter when programmed than when erased, which gives SS degradation due to DIBL. In addition, SS even at initial state is more degraded than that in erased state owing to the same reason.

This channel length variation effect is more significant for the source/drain nonoverlap structure compared to that in the source/drain overlap structure because the fringing electric field from the gate influences more effectively electron density in the S/D nonoverlap region. This results in remarkable electron density distribution difference between programmed and erased states as presented in Fig. 6(b) and 7(b). This effect is more serious in the planar structure since the simulated GAA SONOS device has a smaller channel length variation from the longer gate length and stronger gate controllability. Moreover, the fringing field can induce a side wall channel inversion before the main channel is turned on leading to the degradation of SS for a programmed device with planar structure while it does

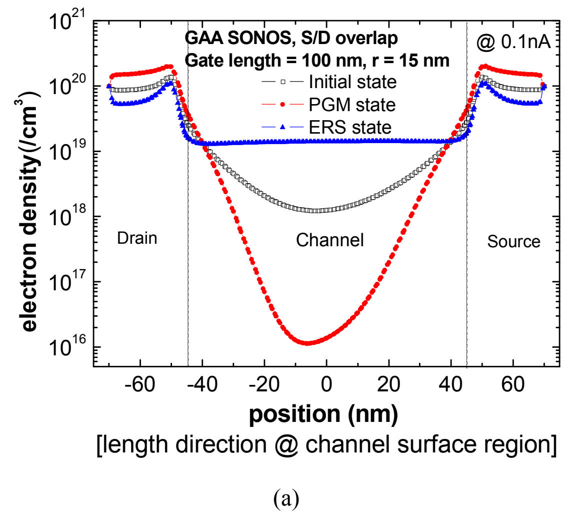


(a)

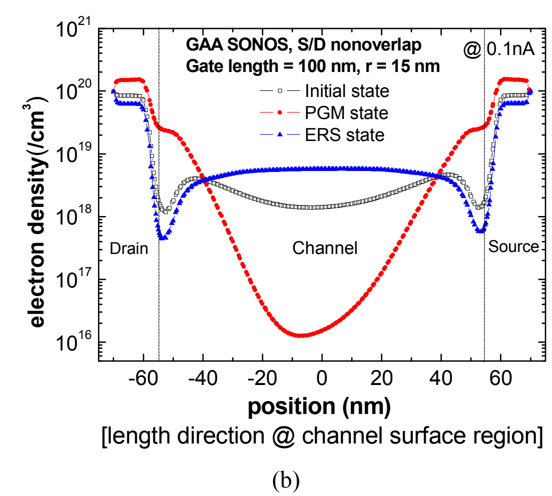


(b)

Fig. 6. Electron densities in initial, programmed and erased states at 0.1 nA of read current along the surface of silicon channel with a length direction for (a) the S/D overlap, (b) S/D nonoverlap structure for the planar SONOS device.



(a)



(b)

Fig. 7. Electron densities in initial, programmed and erased states at 0.1 nA of read current along the surface of silicon channel with a length direction for (a) the S/D overlap, (b) S/D nonoverlap structure for the GAA SONOS device.

not happen in a device with GAA structure of surrounding the channel [8]. Therefore, more remarkable SS degradation is observed in the measured planar TANOS memory cell in programmed state as shown in Fig. 3(b).

On the other hand, during programming procedure, more electrons are trapped in the center of nitride layer in the two simulated devices. After that, when they are erased, the electrons trapped at the edges of nitride layer are not detrapped easily and the remained charge can have an effect on I-V characteristics as shown in Fig. 8(a) and (b). Lancher *et al*. reported that localized electron charge over source/drain (S/D) region in nitride layer not only influence V_{th} but also SS [7]. SS increases as the charge is getting closer to the bottom side of the nitride layer or the density of the charge increases. Similarly, oxide charges over the vicinity of the S/D region have an effect on the SS [6]. The crowded oxide charges located on the relatively small S/D overlap region can repulse the electrons in the S/D and channel region. It is followed by SS degradation owing to the decrease of subthreshold current in the channel surface and degradation of gate controllability.

In the analogous way, the more increased subthreshold slope is represented for the planar device with 5 nm of S/D nonoverlap structure in erased state compared to that in programmed state where it has the dense trapped electron charge of about 2×10^{18} cm^{-3} at the bottom edges of nitride layer as shown in Fig. 8(a). Comparing the both structures, the GAA structure is immune to the SS

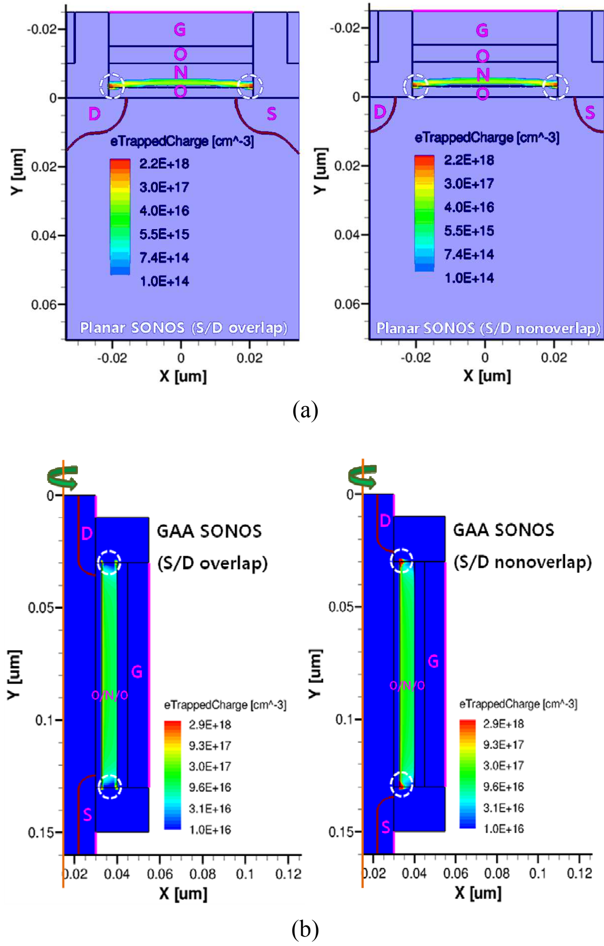
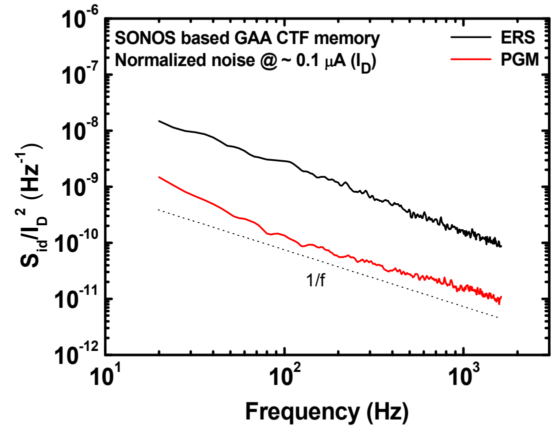
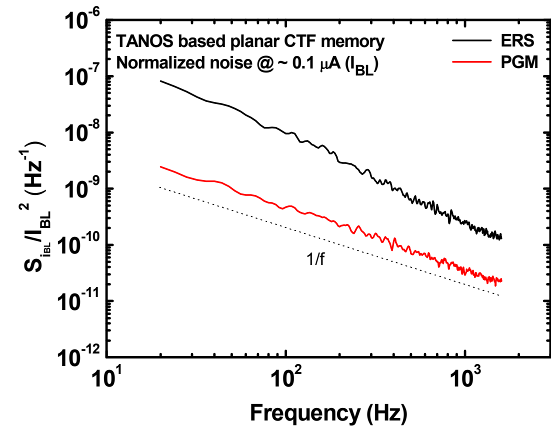


Fig. 8. Electron trapped charge distributions for the (a) planar SONOS, (b) GAA SONOS devices after erase operation where the both devices were programmed previously.

degradation effect induced by the charge at the edges because of its strong gate controllability to the channel region as shown in Fig. 4(c). However, the I_D-V_G curve of the measured GAA SONOS device represents an opposite way from the simulation results as shown in Fig. 3(a). It shows remarkably more degraded SS in erased state compared to that in programmed state. This can be elucidated by the interface states generation due to diffused h^* species from the Si/SiO$_2$ interface after erase operation which results in the subthreshold degradation [18].

To investigate the generation of interface traps in erased state, we measured low frequency noise of the GAA SONOS and planar TANOS devices. The normalized current power spectral densities [S_{id}/I_D^2 (or S_{iBL}/I_{read}^2)] at about 0.1 μA of the read current in the ohmic regime for randomly selected flash memory cells are compared in both erased and programmed states for each device as shown in Fig. 9(a) and (b). The magnitude of S_{id}/I_D^2 in erased state is about 1 order higher than that in programmed state for both the CTF memories which





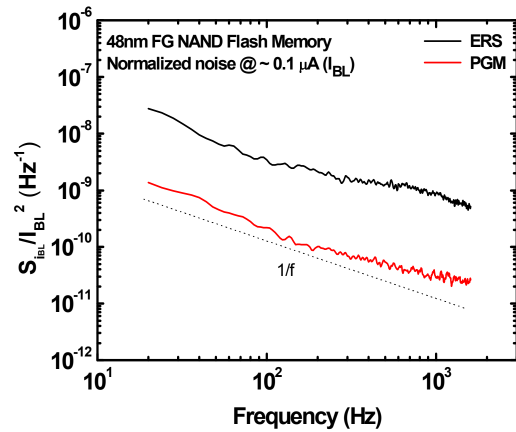


Fig. 9. Normalized current power spectral densities [S_{id}/I_D^2 (S_{iBL}/I_{read}^2)] measured at a read current of 0.1 μA in both programmed and erased states for the (a) GAA SONOS, (b) planar TANOS, (c) 48 nm FG flash memory cells.

means that more interface traps exist in erased state comparing to that in programmed state. Villa *et al.* proved correlation between interface trap density and 1/*f* noise in metal-oxide semiconductor field effect transistors (MOSFETs) through experiment [19]. The N_{IT} derived from the suggested 1/*f* noise numerical model equation considering both carrier number and mobility fluctuations are also quite consistent with that of C-V measurement. It indicates that the flicker noise measurement is a useful technique to characterize interface and oxide traps in the MOSFETs with charge pumping method. The traps in nitride layer may also have an effect on the flicker noise spectrum in the SONOS and TANOS memory devices. However, we can understand that the generation of traps is a negligible factor for 1/*f* noise since the magnitude of S_{id}/I_D^2 in a cell of 48 nm floating-gate (FG) NAND flash memory as shown in Fig. 9(c) is comparable with those of the two CTF memory devices. The tunnel oxide thickness of the measured FG NAND flash memory is about 7 nm which is much thicker than the measured two CTF memory devices, and the charge storage layer is not nitride layer but floating gate. Therefore, it indicates that the main noise source is originated from the interface between Si and tunnel oxide.

N_{IT} generation induced by the movement of h^* species occurred in both of the two CTF memory devices and FG memory device as well after erase operation as demonstrated by noise measurement. It is noted that the induced interface states of the measured GAA SONOS memory cell in erased state function as a more prominent source for determining the subthreshold current properties than those in the planar TANOS and FG memory devices. This is because the measured cylindrical GAA SONOS devices have longer channel length and is not influenced by the channel side wall turn-on effect because the gate surrounds the channel.

IV. CONCLUSIONS

We have studied which makes SSs of memory cells in between programmed and erased states different for TANOS based NAND flash memory cell and GAA SONOS based flash memory unit cell each by employing TACD simulation and noise measurement. The deteriorated SS comes from the short channel effect induced by nonuniform charge distribution in nitride layer for both of the programmed devices. In addition, the remained localized trapped electron charge in nitride edge after erase operation is shown for both devices and it has an effect on SS degradation particularly in the simulated planar SONOS device with S/D nonoverlap structure while it is negligible in the GAA structure. On the other hand, N_{IT} generation originated from released h^* species from the Si/SiO_2 interface after erase operation can be explained by the low frequency noise measurement. The increased S_{id}/I_D^2 after erase operation indicates the interface states generation and it is a critical factor for degrading SS of the measured GAA SONOS memory cell.

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