Improved Charge Pump with Reduced Reverse Current

Kiuk Gwak, Sang-Gug Lee, and Seung-Tak Ryu

Abstract—**A highly efficient charge pump that minimizes the reverse charge sharing current (in short, reverse current) is proposed. The charge pump employs auxiliary capacitors and diode-connected MOSFET along with an early clock to drive the charge transfer switches; this new method provides better isolation between stages. As a result, the amount of reverse current is reduced greatly and the clock driver can be designed with reduced transition slope. As a proof of the concept, a 1.1V-to-9.8 V charge pump was designed in a 0.35 μm 18 V CMOS technology. The proposed architecture shows 1.6 V ~ 3.5 V higher output voltage compared with the previously reported architecture.**

Index Terms—**Charge pump, Reverse current, DC-DC converter, MEMS microphone**

I. INTRODUCTION

Charge pump is one type of DC-DC converter that is often used to produce higher DC voltage from a given supply. The simple structure of it makes charge pump popular in applications such as read/write operation of EEPROM and MEMS MIC, which have relatively low load current with moderate ripple requirements [1-8]. Especially for the applications that require extremely low load current such as for capacitive load (e.g. MEMS microphone which consumes only few nA), charge pump is an ideal candidate for supply generation because of its compactness and low power consumption.

Among various designs, Wu and Chang's architecture [2], based on Dickson's charge pump [1], is a representative one. They developed a charge pump that replaces diodes with switches to achieve higher voltage conversion ratio. However, the reverse current in that structure, caused by the finite rising time of the clock, limits the voltage conversion gain and makes it difficult to predict the output voltage. Thus, for higher output voltage, more stages than the theoretically expected is required.

Several advanced designs with focuses on CMOS reliability, higher load current driving ability, and small chip area [3-5] have been published. Nevertheless, those designs are not suitable for the applications where low input voltage is given and when transistors have relatively high threshold voltages. For example, in Ker's design [5], the maximum gate-source voltage was restricted under VDD. Hence, unless VDD is over the threshold voltage of a given transistor, the charge pump is not able to perform properly. Further modifications [6, 7] show the higher power efficiency and smaller chip area, but they require a complicated timing control of the clock signal.

In this work, we suggest an improved structure of [2] by eliminating the reverse current path with a modified switch control circuit.

II. PREVIOUS CHARGE PUMP

Three consecutive stages of the charge pump of [2] are shown in Fig. 1. Assume the circuit is in steady-state. When CLK changes from 0 to V_{DD} (when CLKB, the inverse of CLK, falls), the n^{th} stage output, V_n, increases by ΔV and the voltages of neighboring stages reduce by the same amount. Consequently, the auxiliary NMOS switch, SW_{auxN}, for the control of n^{th} charge transfer

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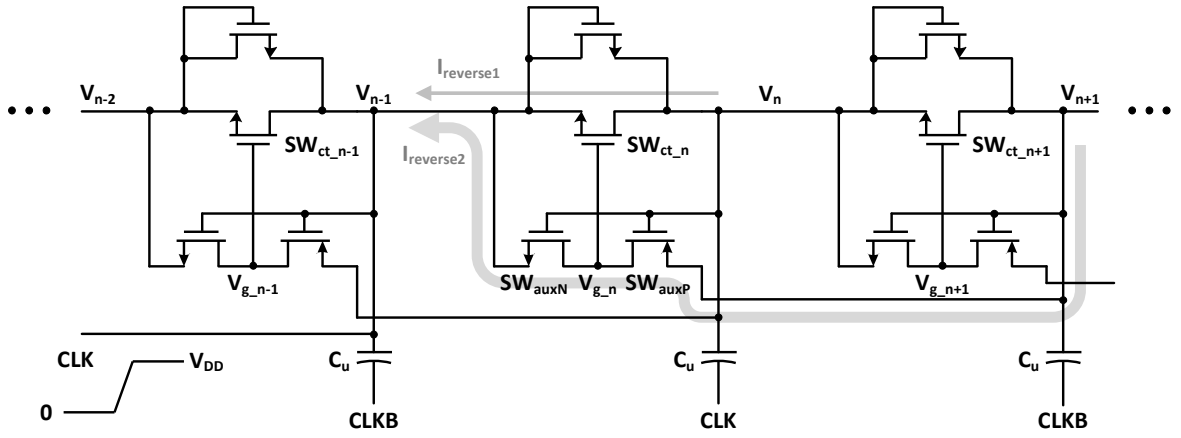

Fig. 1. Circuit diagram of Wu and Chang's charge pump [2].

switch, SW_{ct_n}, turns on by V_n-V_{n-1} = 2ΔV and the PMOS switch, SW_{auxP}, turns off. Thus, V_{g_n} falls from V_{n+1} to V_{n-1} and turns off SW_{ct_n}, and V_{g_n-1} and V_{g_n+1} rise to turn on the $(n-1)^{th}$ and $(n+1)^{th}$ charge transfer switches, SW_{ct_n-1} and SW_{ct_n+1}. Hence, the $(n+1)^{th}$ stage is charged up to the peak voltage of V_n. Similarly, when CLK falls (CLKB rises), V_{n+1} is charged by ΔV. Thus, the output voltage of the charge pump with n stages is determined as

$$V_{out} = V_{DD} - V_d + n\Delta V \quad (1)$$

where V_d is the voltage drop of diode, which is required at the output stage [2]. Ideally, ΔV should be close to V_{DD}. However, the parasitic capacitance at each node and the unwanted reverse currents cause ΔV to be smaller than V_{DD}. Since the parasitic capacitance effect is not significant and can be overcome with ease by increasing unit capacitance C_u, the reverse current effect becomes the dominant loss factor.

Fig. 2 shows detailed voltage waveform of each node of the circuit in Fig. 1 when CLK changes from 0 to V_{DD}. At $t=t_0$, V_n and V_{n-1} have the same value due to the closed SW_{ct_n} with $V_{g\_n}=V_{n+1}$, and V_{n+1} is higher than V_n by 2ΔV. As CLK rises (CLKB falls), V_n increases, and V_{n+1} and V_{n-1} deviate from each other via the finite resistance of SW_{ct_n}. Ideally, SW_{ct_n} must be turned off completely as soon as CLK changes to high in order to prevent the reverse current from V_n to V_{n-1}, which reduces the charge pumping efficiency. This is the reverse current, $I_{reverse1}$ in Fig. 1. However, SW_{auxN} does not turn on until V_n–V_{n-1} (=V_{GS} of SW_{auxN}) reaches the

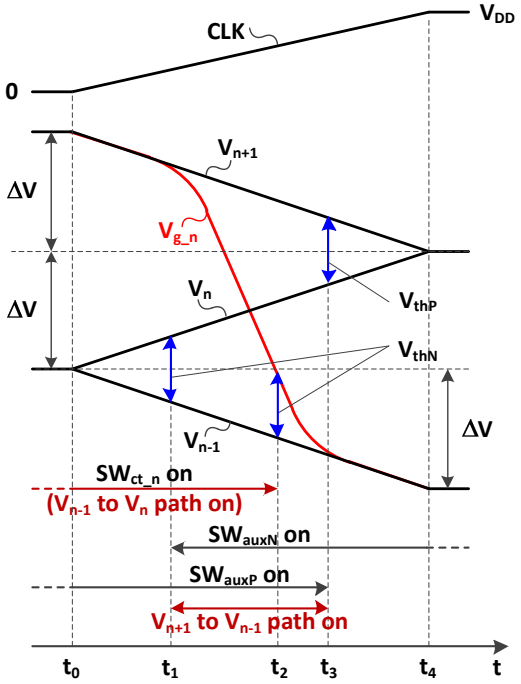

Fig. 2. Operation of the charge pump in Fig. 1.

NMOS threshold, V_{thN}, and, thus, V_{g_n} is tied to V_{n+1} and, thus, SW_{ct_n} stays on. As time passes $t=t_1$, V_n–V_{n-1} becomes larger than V_{thN} and SW_{auxN} turns on. Since SW_{auxP} is still on strongly, this makes another reverse current, $I_{reverse2}$, from V_{n+1} to V_{n-1} via SW_{auxP} and SW_{auxN} while $I_{reverse1}$ still exists. After $t=t_2$, SW_{ct_n} turns off (V_{g_n}–$V_{n-1} < V_{thN}$) and $I_{reverse1}$ becomes zero. When $t > t_3$, SW_{auxP} turns off (V_{n+1}–$V_n < V_{thP}$) and $I_{reverse2}$ becomes zero. Here, V_{thP} is the threshold voltage of PMOS. To sum up, the charge pumping stages work ideally only after $t=t_3$ with no reverse current.

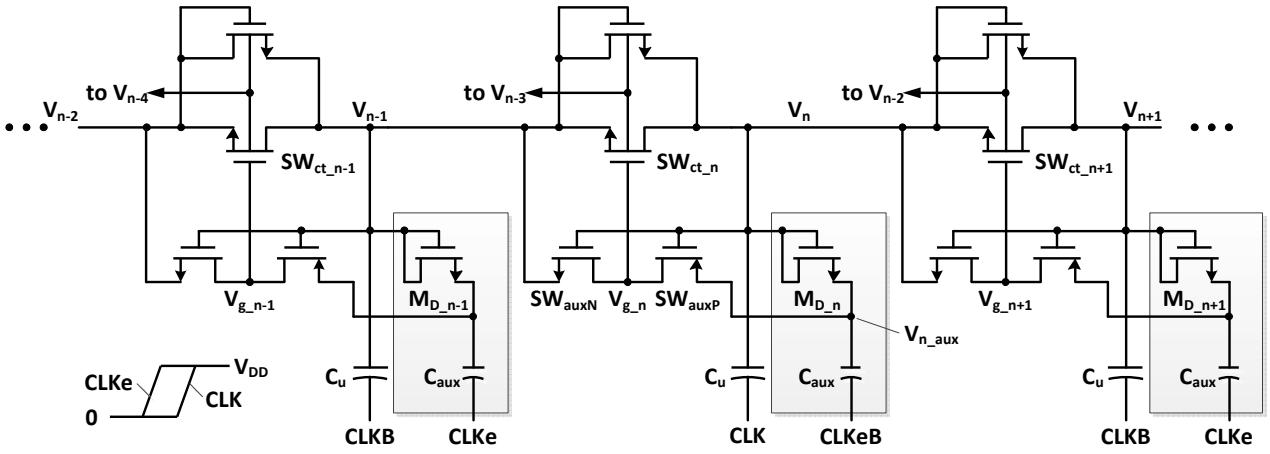

Fig. 3. Circuit diagram of the proposed charge pump.

Note that $I_{reverse2}$ is the most serious problem in Wu and Chang's structure because it makes a short circuit current through the stages driven by CLKB (…, V_{n-3}, V_{n-1}, V_{n+1}, V_{n+3}, …) and degrades the charge pumping gain seriously. Likewise, stages driven by CLK (…, V_{n-2}, V_n, V_{n+2}, …) are found to short each other during the clock transition periods. Hence, to reduce the amount of the reverse current, the rising time, t_r, of the clock should be minimized by employing large clock buffers, which increases the dynamic power consumption and circuit noise.

III. Proposed Charge Pump

In this work, in order to reduce the reverse currents in Wu and Chang's structure, a modified architecture is proposed as shown in Fig. 3. In order to break the long short-circuit current ($I_{reverse2}$) path driven by CLK and CLKB, control signals from the next stages, the proposed circuit employs an additional clock signal, CLKe, which is an early-time version of CLK. In addition, in the circuit, a diode-connected transistor, M_{D_k}, and an auxiliary capacitor, C_{aux}, are added in each stage. Note that C_{aux} can be designed to be much smaller than C_u because the parasitic capacitance at every node driven by C_{aux} is small and C_{aux} does not provide current to the load.

The operation of the proposed architecture is illustrated in Fig. 4. In steady-state, V_{n_aux} (refere to Fig. 3) has the same value as $V_{n+1}-V_{thN}$ because of the diode-connected NMOS, M_{D_n} and the clock configurations.

For $t < t_0$, CLK=0 and the inverse of the early clock,

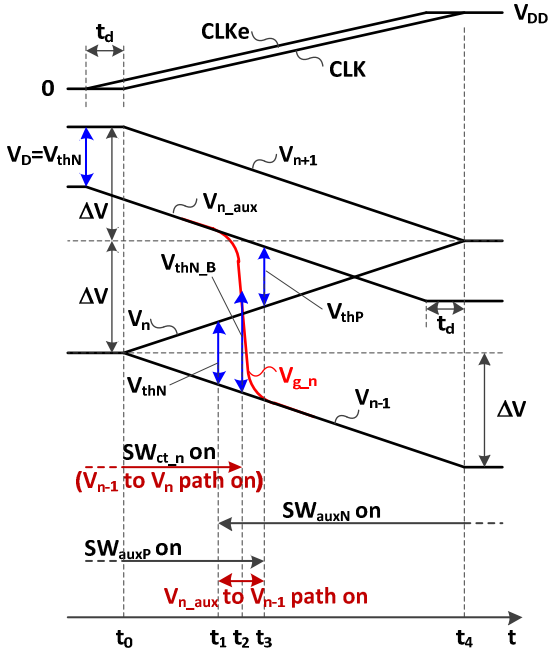

Fig. 4. Operation of the charge pump in Fig. 3.

CLKeB, starts to fall and, thus, V_{g_n} decreases. After a delay of t_d (at $t=t_0$) CLK starts to rise and, thus, V_n and V_{n-1} begins to increase and decrease, respectively. As long as ($V_{g\_n}-V_{n-1}$) is higher than the threshold of SW_{ct_n} (V_{thN_B}), SW_{ct_n} stays on and the reverse current flows from V_n to V_{n-1} ($I_{reverse1}$ as in Fig. 1). However, unlike the previous work [2] in this work, intentionally generated body effect reduces the reverse current through SW_{ct_n} by increasing its threshold voltage from V_{thN} to V_{thN_B}. Note that this design uses a deep n-well process and the body terminal of SW_{ct_n} is connected to V_{n_3} for the increased

threshold and to guarantee a constant body-to-source voltage of 2ΔV. This choice has been made so that the on-resistance of SW_{ct_n} increases to reduce the reverse current while guaranteeing that V_{thN_B} is smaller than 2ΔV. This approach also solves the increasing threshold problem of SW_{ct_n} as stage goes to the output in [2].

When $t=t_1$, SW_{auxN} starts to turn on, similarly to the case in Figs. 1 and 2, because its V_{GS} exceeds the threshold, V_{thN}. However, since stages are not connected to each other via the auxiliary switches, the reverse current through them ($I_{revers2}$ in Fig. 1) is completely eliminated. Even though some amount of charge can be shared between V_{n_aux} and V_{n-1}, the effect is negligible because V_{n_aux} always has higher voltage than V_{n-1} and their capacitance difference is huge ($C_u > C_{aux}$). Actually, this helps turning off SW_{ct_n} by dropping V_{g_n} earlier than the ideal case. Furthermore, if t_d becomes sufficiently long, SW_{auxP} turns off earlier than SW_{auxN}'s turn-on, which removes the charge sharing between C_u and C_{aux}.

When t passes t_2, V_{g_n}–V_{n-1} becomes smaller than V_{thN_B} and SW_{ct_n} turns off. Note that the time for $I_{reverse1}$ is shorter than that in [2] not only because the threshold voltage of SW_{ct_n} is increased from V_{thN} to V_{thN_B} but also because the starting level of V_{g_n} (i.e. V_{n_aux} when CLKeB goes low) is lowered by the diode voltage drop $V_D=V_{thN}$ and CLKeB starts to decrease earlier. As t passes t_3, SW_{auxP} turns off due to V_{g_n}–$V_{n-1} < V_{thN\_B}$. For the remaining time until CLK reaches V_{DD}, the charge pump works ideally.

Consequently, compared to Wu and Chang's architecture the reverse currents through all the paths are reduced significantly in the proposed work.

IV. RESULTS

The proposed charge pump was designed for a 0.35 μm 1P4M 18 V CMOS technology. Typical threshold voltage of NMOS is 0.8 V and that of PMOS is 1.1 V. For all designs, 18V PIP capacitors are used. For both charge pumps, [2] and the proposed one, the total capacitance was kept the same for fair comparison.

To verify the effect of the reduced reverse currents, rising time of CLK, t_r, was varied. At zero load current (assumed capacitive load driving such as MEMS microphone), the output voltages after the last stage diode are plotted in Figs. 5 and 6 under a 1.1 V input (V_{DD}) condition and 5 MHz clock frequency.

Fig. 5 shows the simulated outputs of 10-stage charge pumps with the structure in [2] and the proposed one. Solid and dotted lines represent the proposed and Wu and Chang's architecture, respectively. As the unit capacitance increases, the effect of the parasitic capacitance at each node is reduced and thus the output voltage increases.

For the proposed architecture, the output voltage variation is less than 1% when the rising/falling time of the clock varies from 0 s to 4 ns. On the other hand, for Wu and Chang's architecture, the output voltage varies over 30% of the expected value due to the reverse current caused by the finite clock rising time of the clock. The unit capacitance (C_u) and auxiliary capacitance (C_{aux}) of the proposed architecture is chosen to be 294 fF and 48 fF, respectively. Consequently, the unit capacitance of 344 fF is used for the architecture of [2].

Fig. 6 compares the output voltages of the two designs for different number of stages. Apparently, ΔV of the proposed architecture stays near V_{DD} in all conditions. On the other hand, ΔV of [2] is quite smaller than V_{DD} and seriously decreases as t_r increases. Note that t_d is set to be half of t_r in this simulation. As long as t_d is over half of t_r, the accuracy of t_d barely affects the performance of the charge pump.

Layout of the proposed and Wu and Chang's are shown in Fig. 7. Although the unit capacitance of the proposed architecture(top) is smaller, total area including auxiliary capacitors is similar for both the proposed and Wu and Chang's architecture (bottom), 182 x 125 μm^2.

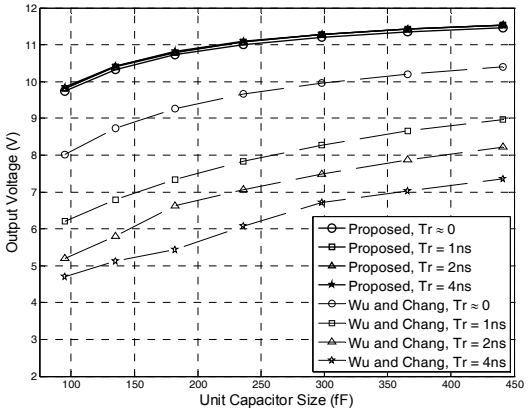

Fig. 5. Simulated output voltages of 10-stage of Wu and Chang's charge pump and the proposed charge pump with varying unit capacitance and 1.1V V_{DD} and 1 pF capacitive load.

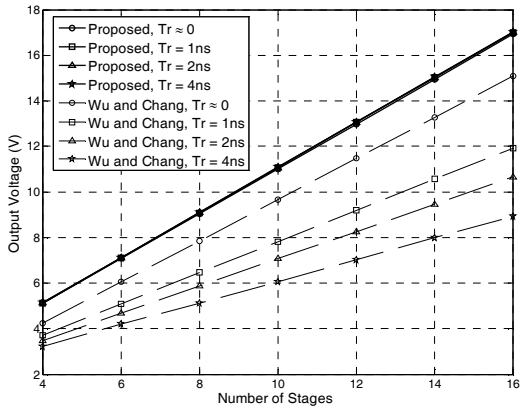

Fig. 6. Simulation results for Wu and Chang's and the proposed charge pump with various t_r and the number of stages when 1 pF capacitive load is used.

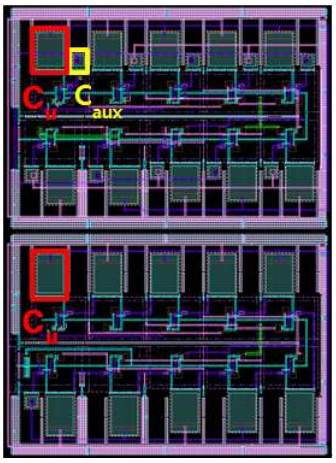

Fig. 7. Layout of the proposed charge pump (top) and Wu and Chang's charge pump (bottom). The sizes of outlines for both layout are about 182 x 125 μm^2.

Fig. 8 shows the post-simulation results of both charge pumps with 10 stages with 5 MHz clock. When the load current is zero, compared to the pre-simulation results in Fig. 5, the output voltage is degraded approximately by 1.3 V due to the parasitic capacitance of the body connections of NMOS and PMOS. Because small unit capacitance is employed, the output voltage degrades rapidly as the load current increases. However, the proposed architecture shows higher output voltages than [2] in all cases. Note that, as shown in Fig. 5, 6, 7, and 8, the performance of the proposed architecture is not limited by the small unit capacitance and no load condition.

Consequently, it is verified that the proposed architecture outperforms the conventional charge pump

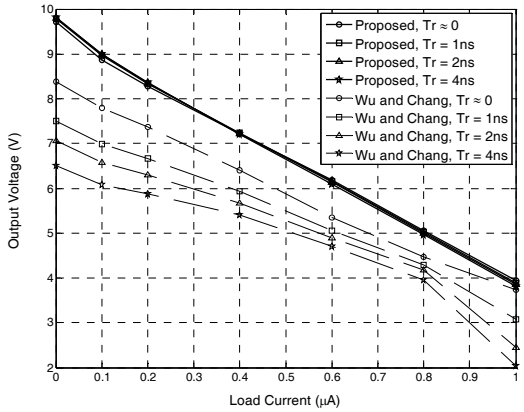

Fig. 8. Post-simulation results for 10 stages of Wu and Chang's charge pump and the proposed charge pump with various t_r and load current with 1 pF capacitor in parallel. 5 MHz clock frequency is used, and t_d is set to the half of t_r.

owing to the reduced reverse current. This advantage allows the designer to use a smaller clock buffer and less number of stages for lower power consumption and small area. Since the proposed architecture is insensitive to the slope of the clock edge, the discrepancy between the design and measurement results is decreased. Unfortunately, however, we could not measure the fabricated chip because of the error in I/O design.

V. CONCLUSIONS

A new charge pump architecture for reduced reverse current is presented. Based on Wu and Chang's architecture, the proposed architecture employs an additional diode and capacitor to isolate each stage. In addition, intentional body bias and an early clock are employed to further reduce the reverse current. As a result, the proposed charge pump has higher output voltage and robustness to the variation of the clock with a chance of lower power design.

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