Power Integrity and Shielding Effectiveness Modeling of Grid Structured Interconnects on PCBs

SangKeun Kwak, YoungSic Jo, JeongMin Jo, and SoYoung Kim

Abstract—**In this paper, we investigate the power integrity of grid structures for power and ground distribution on printed circuit board (PCB). We propose the 2D transmission line method (TLM)-based model for efficient frequency-dependent impedance characterization and PCB-package-integrated circuit (IC) co-simulation. The model includes an equivalent circuit model of fringing capacitance and probing ports. The accuracy of the proposed grid model is verified with test structure measurements and 3D electromagnetic (EM) simulations. If the grid structures replace the plane structures in PCBs, they should provide effective shielding of the electromagnetic interference in mobile systems. An analytical model to predict the shielding effectiveness (SE) of the grid structures is proposed and verified with EM simulations.**

Index Terms—**Power delivery network, impedance, segmentation method, PCB, fringe capacitance, decoupling capacitor, shielding effectiveness**

I. INTRODUCTION

In modern digital systems, mobile systems, and high-density system on packages (SOP), simultaneous switching noise (SSN) becomes a limiting factor for proper operation of the systems as the clock operating frequency increases. SSN occurs when the signal going through the via suffers return current interruption caused by change of the reference plane. To reduce the amount of unwanted SSN, the impedance of the power delivery network (PDN) has to be kept low over a wide range of frequencies [1, 2].

In the PCBs of digital systems, plane structures are often used for power distribution. Plane structures provide a stable power supply over a wide area, minimize impedance, and reduce SSN [3]. The analysis of a plane structure can be performed using electromagnetic (EM) simulators based on the method of moments (MOM), the finite element method (FEM), and the finite difference time domain method (FDTD). The 3D full-wave EM method usually requires a lot of computation time and a large memory resource [4, 5]. Consequently, to reduce the time and memory of simulation, a two-dimensional transmission line method (TLM)-based circuit model was proposed [6, 7]. The TLM-based equivalent circuit model for rectangular plane structures, which can be operated by SPICE, consists of a unit cell composed of RLC elements, transmission line elements, or W-elements [8]. The advantage of the TLM-based circuit model for PCB power distribution is seen, when the PCB model can be included in designing and simulating integrated circuits. Cavity resonator method is an analytical modeling technique to characterize the impedance matrix at port locations on a rectangular parallel-plane pair structure [9, 10]. For arbitrary shaped parallel-plane structure, an integral-equation equivalent circuit method is proposed [11]. As the structures of the power delivery network become more complex, the concept of the segmentation method can be used [12]. Another approach to analyze a multi-layer PCB is to decompose the chip-package

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hierarchical PDN into several structures, calculate the impedance of the decomposed structures independently, and merge the results to get the impedance of the entire structure [13, 14].

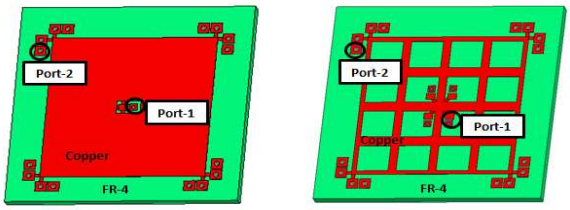
As the complexity of the interconnections in the PCB design increases, it is likely that the grid structures can be used in the PCBs. This type of structure is often used for on-chip power and ground distribution. In the grid structures, a via can pass through the area without metal, hence making possible complicated signal routing. The resonance frequency can be optimized by controlling the metal portion of the grid structure. In this study, we investigate the power integrity of the grid structure using 2D TLM with the unit cell. The grid model for the PCBs needs to take into account a fringing electric field that occurs at the edges and the effect of the probing port. We verify the proposed modeling method with measurement of the test grid structures on the PCB and 3D EM simulations. The 2D TLM-based equivalent circuit model enables co-simulation of a PCB-package-integrated circuit.

This paper is organized as follows. Section II describes the modeling of the grid test structures. Section III gives the simulated and measured Z-parameter results to validate the proposed model and presents the optimization of the impedance of the grid structure based on the proposed model. Section IV discusses the SE for the grid structures. In Section V, the conclusion of this paper is presented.

II. EQUIVALENT CIRCUIT MODEL FOR THE GRID STRCUTURE ON A PCB

1. 2D TLM-Based Equivalent Circuit Model

Fig. 1(a) shows the traditional power and ground plane structure used in PCBs, and Fig. 1(b) shows the grid structure consisting of two layers, one for power distribution and the other for ground distribution, which has been modeled and analyzed in this work. As the signal routings in PCBs become more complicated, the grid structure, which is commonly used in ICs, will allow more space for routing. However, the impedance property and shielding effectiveness may not be as good as those in the plane. The probing ports are defined at the center (port 1) and at the edge (port 2) for S-parameter measurement. The dielectric material of this PCB is FR-4,



(a) (b)

Fig. 1. The plane and grid structures on a PCB (a) Plane structure, (b) grid structure.

which has a relative permittivity of 4.4 and a dielectric loss tangent ($\tan(\delta)$) of 0.02.

The 2D TLM-based equivalent circuit model is used for power integrity analysis of the plane structure because a circuit simulator like SPICE can be used to analyze the impedance of the network. To develop a 2D TLM-based equivalent circuit model, the power and ground plane structure can be divided into unit cells as shown in Fig. 2(a). The number of unit cells for a given plane structure can be determined by the following relation (1) [15].

$$N \geq 14.14 d \sqrt{LC} f \,, \tag{1}$$

where N is the minimum number of unit cells in the x or y direction needed to meet the accuracy requirements at a specified frequency f, d represents the size of the plane in the x or y direction, and L and C are the inductance and capacitance per unit area, respectively. Once N is determined by the width of the unit cell, w, can be determined by

$$w = d / N \,. \tag{2}$$

The equivalent circuit model for the unit cell based on the lumped circuit elements is shown in Fig. 2(b) [3, 6]. Based on the width of a unit cell (w), separation between planes (d), dielectric constant (ε), loss tangent of the dielectric ($\tan(\delta)$), metal thickness (t), metal conductivity (σ_c), permittivity of free space (ε_0), permeability of free space (μ_0), relative permittivity of the dielectric (ε_r), and frequency (f), the equivalent circuits values, C, G, R, and L of the unit cell can be computed as in (3) [6].

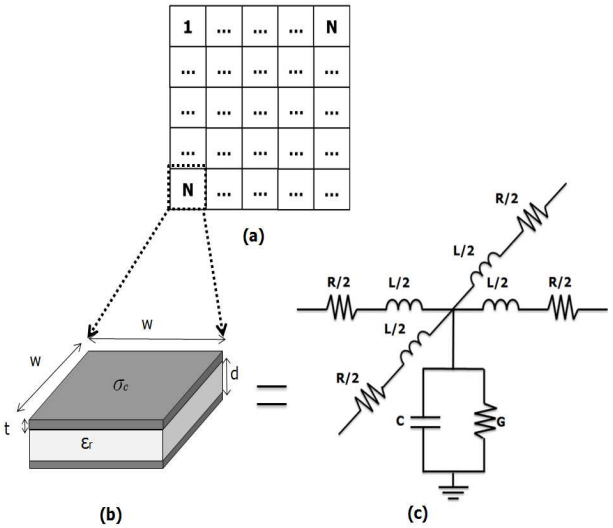


Fig. 2. Equivalent circuit of a plane structure using the 2D transmission line method (a) Plane structure, (b) unit cell, (c) equivalent circuit.

$$C = K_C \varepsilon_0 \varepsilon_r \frac{w^2}{d},\ L = K_L \mu_0 d,\ G = 2\pi f C \tan(\delta)$$

$$R = R_{dc} + R_{ac} = \frac{2}{\sigma_c t} + 2\sqrt{\frac{\pi f \mu_0}{\sigma_c}}\ . \qquad (3)$$

Two fitting parameters, K_C and K_L are empirically determined by comparing the Z-parameters obtained from vector network analyzer (VNA) measurements of the plane structure fabricated on PCB and 2D TLM based equivalent circuit model simulation. The fitted values of K_C and K_L are found to be 1.5 and 0.5, respectively, for the plane structure. The grid structure shown in Fig. 1(b) can be analyzed by dividing the structure into unit cells and using K_C and K_L obtained from the plane structure to determine L and C for the equivalent circuit model. However, due to the difference of fringing effects, three types of unit cells will be defined and an equivalent circuit model will be proposed in the next section.

2. Unit Cells Model for the Grid Structure Considering Fringe Capacitance

We decompose the grid structure into unit cells to capture the 2D transmission line property. Depending on the location within the grid, there is an additional fringing capacitance, so we define three types of unit cells as shown in Fig. 3. Unit cell 0 is located within the grid structure, so it has only parallel plate capacitance. In

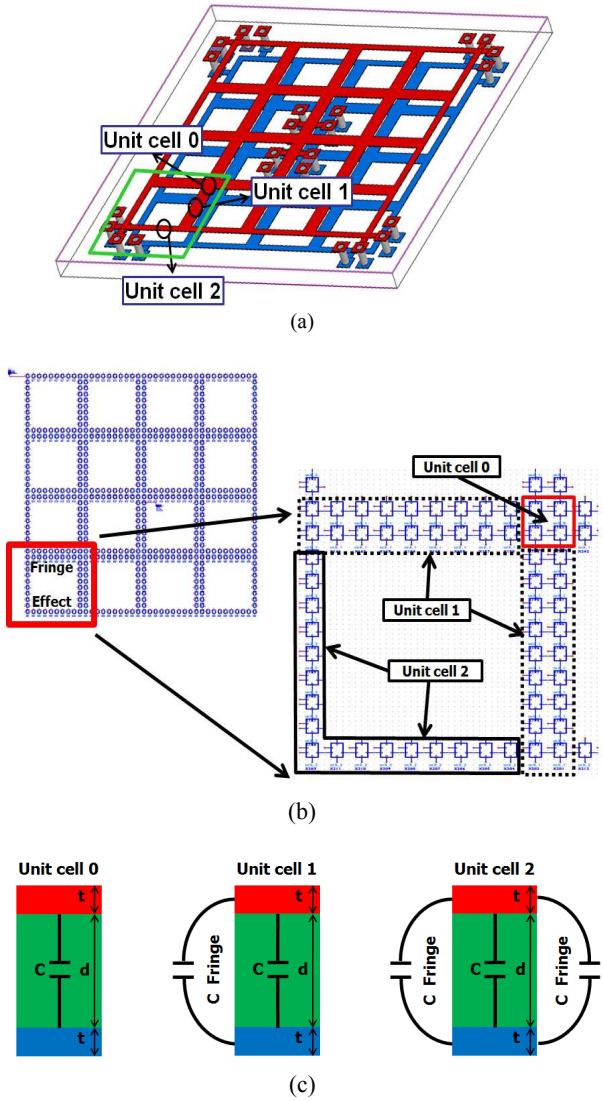


Fig. 3. Three types of unit cells (a) Location of the unit cells model in the grid structure, (b) location of the unit cells shown with the equivalent circuit model of the grid structure, (c) unit cell models shown with fringe capacitance.

unit cell 1, one side is located at the metal edge, so there is fringing capacitance term on that edge. In unit cell 2, two sides are located at the edge, so the equivalent circuit model includes two fringing capacitances.

The fringe capacitance and the parallel plate capacitance based on the geometry parameters shown in Fig. 4 can be obtained from the following Eq. (4) [16].

$$C_{fringe} = \frac{w\varepsilon_0\varepsilon_r t e^{\left(-\frac{s+w}{d+t}\right)}\left(\ln\left(1+\frac{2t}{d}\right)+e^{\left(-\frac{d+w}{3d}\right)}\right)}{t\pi e^{\left(-\frac{s+w}{d+t}\right)}+(s+w)\left(\ln\left(1+\frac{2t}{d}\right)+e^{\left(-\frac{d+w}{3d}\right)}\right)}$$

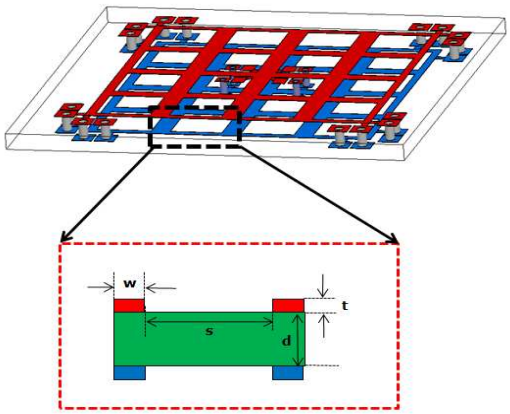
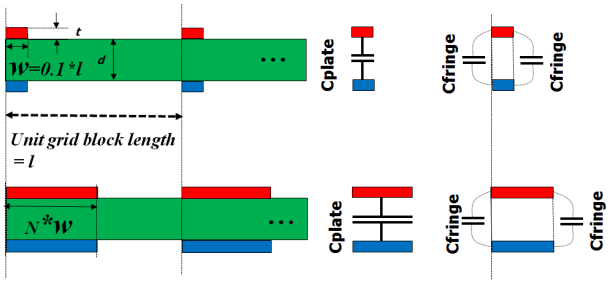
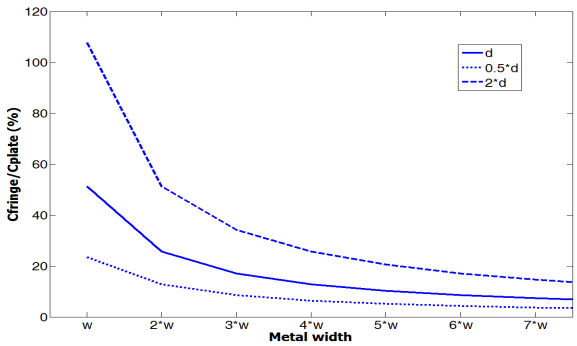


Fig. 4. The definition of the parameter for the fringe capacitance on the grid structures.



(a)



(b)

Fig. 5. The significance of the fringing capacitor versus parallel plate capacitor (a) Cross sectional view of the PCB grid with different metal widths, (b) the percentage of the fringing capacitor versus parallel plate capacitor as the metal width is swept.

$$C_{parallel\_plate} = \varepsilon_0 \varepsilon_r \frac{w^2}{d} \tag{4}$$

The parameter w is the width of the grid metal line, s is the distance between metal lines, d is the separation between the metal lines, and t is the thickness of the line.

Fig. 5 shows the percentage of the fringing capacitor versus the parallel plate capacitor in the grid structure as the metal width changes. The final unit cell model of three types of unit cells defined in Fig. 3 are shown in Fig. 6.

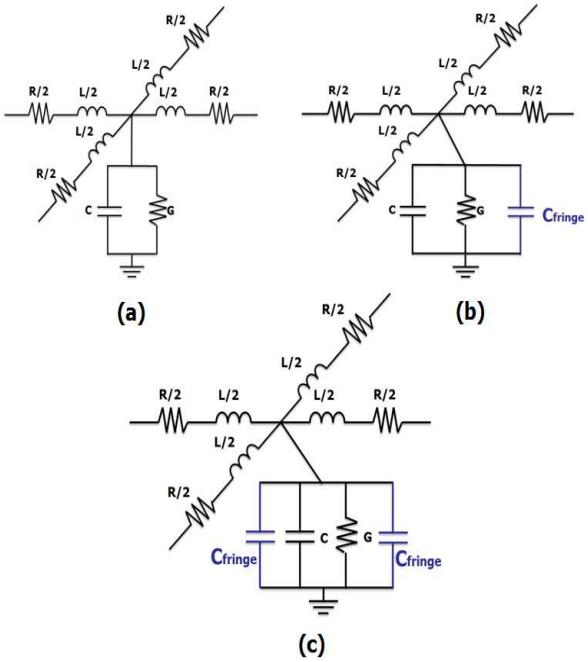
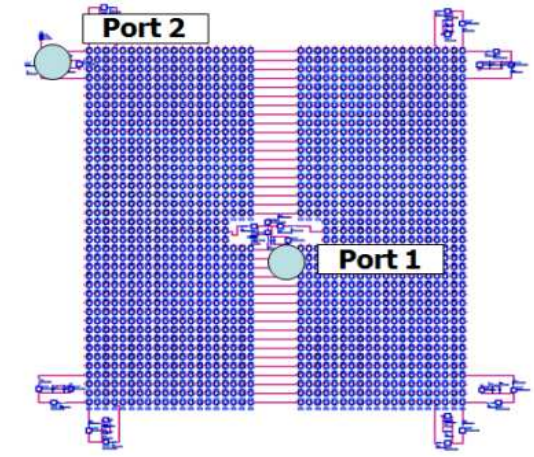


Fig. 6. The equivalent circuit model of the three types of unit cells for modeling a grid structure (a) Unit cell 0, (b) unit cell 1, (c) unit cell 2.

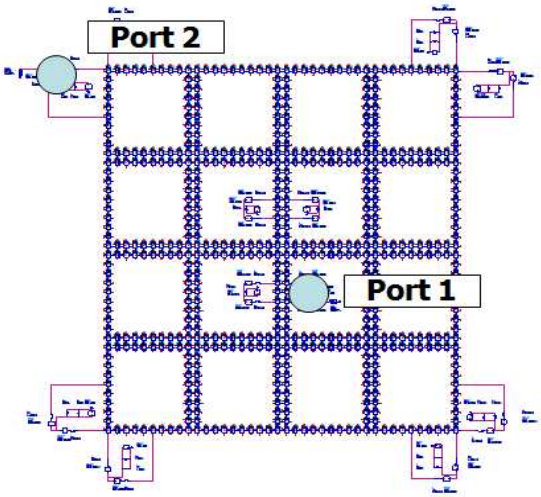
The equivalent circuit model for the plane and grid structures on a PCB are constructed by connecting unit cells in the SPICE simulator as shown in Fig. 7. Agilent's Advanced Design System (ADS) is used to characterize the impedance characteristics. The number of unit cells was 40 in each x and y direction, guaranteeing 2D TLM model accuracy up to 15 GHz according to Eq. (1).

3. Equivalent Circuit Model for the Probing Ports

In order to match the simulation results with the measurement results, the equivalent circuit model is developed for the probing ports. The details of the structure of the center probing port, port 1, and the edge probing port, port 2, are shown in Fig. 8(a) and (b). The equivalent circuit model is based on π model as shown in Fig. 8(c) [15]. The total capacitance, C_{Port}, between Vdd and Gnd are divided in half and connected at two ends, and the R_{Port} and L_{Port} are lumped to the Vdd. The model values derived for the center port structure,



(a)



(b)

Fig. 7. Equivalent circuit model for (a) the plane structure, (b) the grid structure.

port 1, are showed in Eq. (5) based on the analytical equations proposed in [17, 18] for rectangular ports and cylindrical via structures.

$$
\begin{aligned}
R_{port1} &= \frac{t}{\sigma_c b^2} + \frac{1}{\sigma_c 2\pi h}\ln\left(\frac{r}{r-t}\right) + \left(\frac{t}{b}+\frac{h}{2\pi r}\right)\sqrt{\frac{\pi f \mu_0}{\sigma_c}} \\
C_{port1} &= \varepsilon_0 \varepsilon_r \frac{bt}{d} \\
L_{port1} &= \frac{\mu_0}{2\pi} h\left(\ln\left(\frac{2h}{r}\right)-1\right) \\
G_{port1} &= 2\pi f C_{port1}\tan(\delta)
\end{aligned}
\tag{5}
$$

The values of lumped elements for the edge probing port, port 2, are derived and shown in Eq. (6).

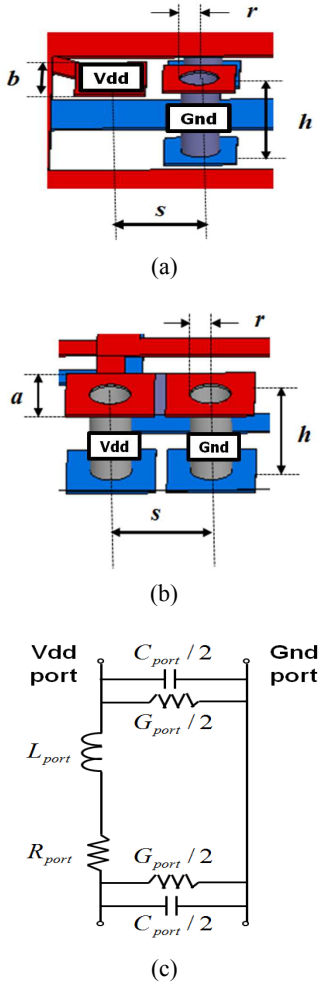


Fig. 8. The probing port at the center (port 1) and at the edge (port 2) (a) Structure of the center port (port 1), (b) structure of the edge port (port 2), (c) equivalent circuit model of the ports.

$$
\begin{aligned}
R_{port2} &= \frac{1}{\sigma_c \pi h}\ln\left(\frac{r}{r-t}\right) + \frac{h}{\pi r}\sqrt{\frac{\pi f \mu_0}{\sigma_c}} \\
C_{port2} &= \varepsilon_0 \varepsilon_r \left(2\frac{bt}{d}+\frac{hr}{s-r}\right) \\
L_{port2} &= \frac{\mu_0}{\pi} h \ln\left(\frac{s}{r}\right) \\
G_{port2} &= 2\pi f C_{port2}\tan(\delta)
\end{aligned}
\tag{6}
$$

III. Power Integrity of the Grid Structure on a PCB

1. Proposed Model Validation

To verify the proposed grid structure modeling based on 2D TLM, 3D EM simulation is performed using High

Frequency Structure Analysis (HFSS) from Ansys Inc, as shown in Fig. 9. A test PCB structure was created, and S-parameters were measured using the vector network analyzer (VNA) E5071B from Agilent with a microprobe and probe station, as shown in Fig. 10. Simulation and measurement were conducted for a frequency range of 10 MHz to 3 GHz.

To analyze the power integrity, we convert the S-parameters to Z-parameters using the following relationship (7) with a Z_0 of 50 ohm [19]:

$$Z_{11} = Z_0 \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}, \quad (7)$$

where Z_{11} represents the actual power distribution network impedance that is observed by the circuit when it is connected to port 1 [20].

Fig. 11(a) shows the PDN impedance (Z11) comparison between the 2D TLM-based equivalent circuit model and the VNA measurement results at port 1 for the plane structure. The comparison results using 3D EM simulation and the 2D TLM simulation methods, as well as measurement using VNA with micro tips, are well matched. Fig. 11(b) shows the PDN impedance (Z11) comparison between the 2D TLM-based equivalent circuit model and 3D EM simulation results at port 1 for the grid structure. By adding fringing capacitance and the port model to the plane, the 2D-TLM based results

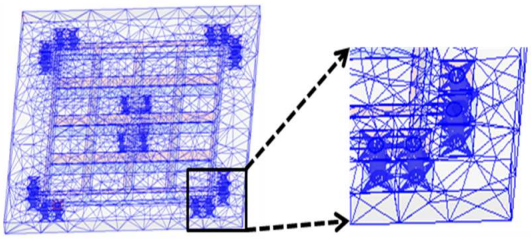
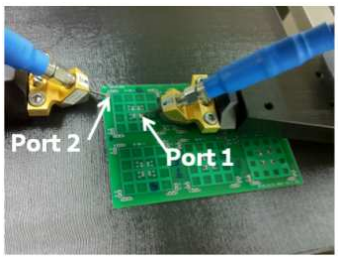
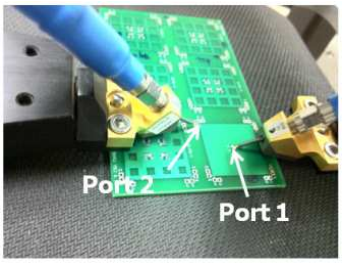


Fig. 9. Mesh of 3D simulation for the grid structure.

(a)

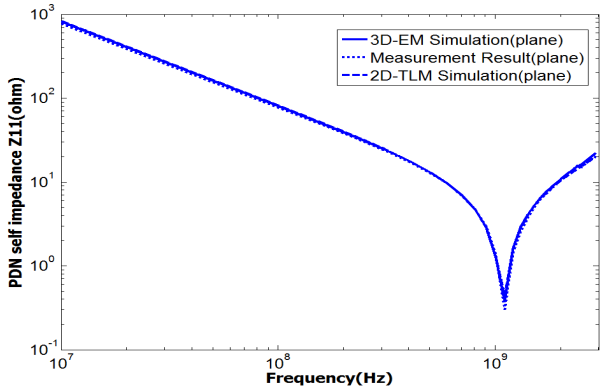


(b)

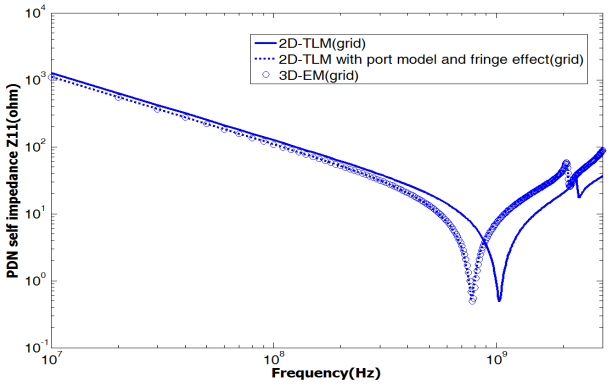


(c)

Fig. 10. Experimental setup using a two-port VNA with micro tips (a) E7071B Agilent vector network analyzer, (b) measurement of the grid structures on a PCB, (c) measurement of the plane structures on a PCB.



(a)



(b)

Fig. 11. Self impedance, Z11, comparison between simulation and measurement (a) Plane structure, (b) grid structure.

become closer to the 3D EM simulation results.

Three types of grid structures were designed based on the portion of metal (POM) as shown in Fig. 12(a). The grid structure is defined as the ratio of area filling to copper-metal of the PCB structures. The structure of the PCB POM36 consists of 36% copper metals and 64% FR4 (or air space) materials, as shown in Fig. 12(b). The Z_{11} values of the three different sizes of grid structure are simulated by 3D EM simulation, and the results are shown in Fig. 12(c). Fig. 13 shows the equivalent circuit analysis of impedance versus frequency including grid and port models to explain the changes in resonance and anti-resonance frequencies for difference POMs. Since the port models are the same for different POM structures, differences in resonance frequency, f_1, are dominated by the change in C_{grid}. For larger POM structures, C_{grid} is larger, so the resonance frequency becomes smaller as in Fig. 12(c). The anti-resonance frequency, f_2, is proportional to $1/2\pi\sqrt{L_{grid}C_{port}}$ because C_{grid} is larger than C_{port}. Since C_{port} is the same for difference POM structures, f_2 is determined by the L_{grid}. For a larger POM structure, the loop size that determines the inductance becomes smaller, so L_{grid} becomes smaller. As a result, in Fig. 12(c), the anti-resonance frequency is higher for larger POM structures.

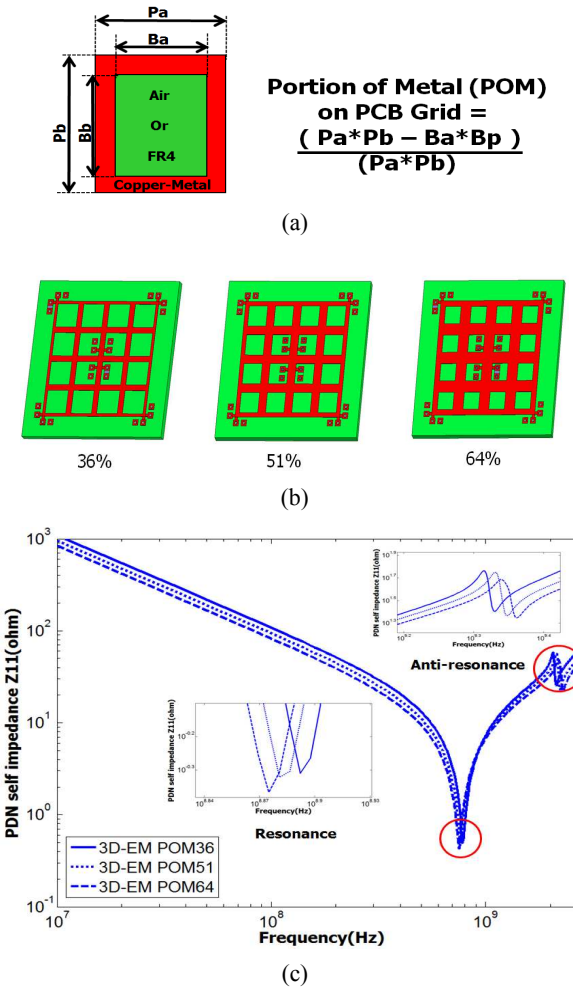


Fig. 12. The comparison results for the PDN self-impedance Z11 of the grid structures with different sizes (a) The definition of POM for the grid structure on the PCB, (b) grid structure with a different POM, (c) Z11 simulation results for the three different grid sizes.

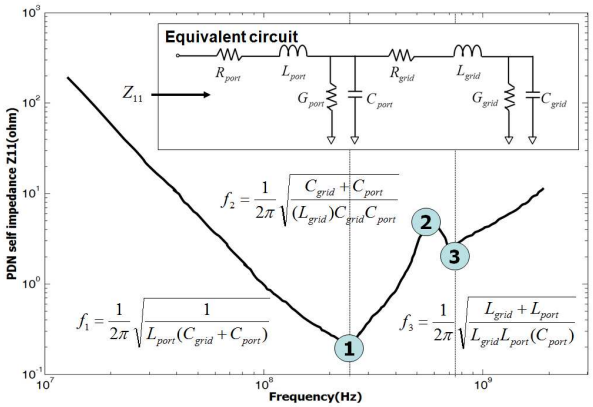


Fig. 13. Analysis of impedances in grid structure including the port model.

2. Grid Structure Impedance Optimization

In order to design the PCB of a mobile system using the grid structure for power distribution, we need to consider these impedance characteristics. Often, the power network impedance is optimized by inserting decoupling capacitors [20]. Fig. 14 shows the impedance comparison of plane and grid structures using 2D-TLM model. The return current can be larger in grid structure than that of the plane structure resulting in larger inductance. The difference of the total capacitance is less dominant, because there is less area capacitance in grid structure there is additional capacitance from fringing capacitance. As a result, the resonance frequency is smaller for grid structure than that of the plane structure. So for the grid structure, the frequency range where the impedance is inductive is larger than that of the plane

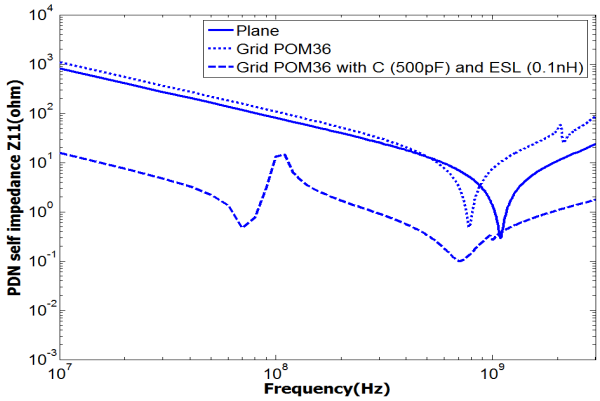


Fig. 14. The impedance optimization result of the grid structures by adding decoupling capacitor using 2D-TLM simulation.

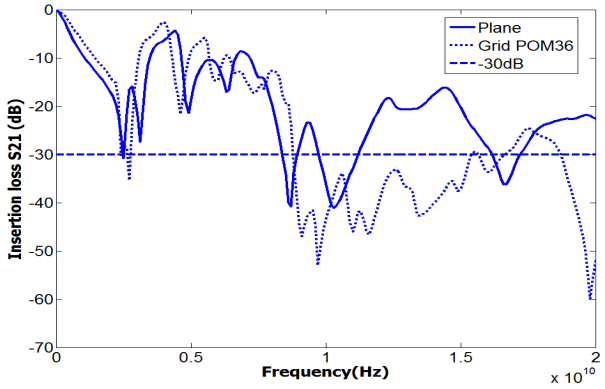


Fig. 15. Insertion loss comparison (S21) between the plane and grid structure using 2D-TLM simulation.

structure. Fig. 14 shows the impedance optimization of the grid structures using the 2D TLM model with a decoupling capacitor, which is added at port 1. By adding a 500 pF decoupling capacitor with 0.1 nH equivalent series inductance (ESL) to the grid structure, the frequency-dependent Z-parameter can be controlled to be less than or similar to that of the plane for the overall frequency range. Using the 2D TLM-based equivalent circuit model for the grid structure developed in this research, the power impedance change due to addition of the decoupling capacitor can be easily tested using a circuit simulator. The impedance characteristics are optimal if the ESL and ESR is minimized, which is achieved at the expense of additional cost.

Fig. 15 shows the insertion loss (S_{21}) between port 1 and port 2 of the plane and grid structures. The insertion loss shows how the simultaneous switching noise propagates and affects other ICs that are connected to the PCB [20]. Up to 8 GHz, the difference is minor; however, at a higher frequency range, the grid structure shows better noise rejection than the plane structure.

IV. Shielding Effectivenss of the Grid Structure

If the grid structures replace the plane structures in PCBs, they should provide effective shielding of the electromagnetic interference in mobile systems. In this section, we investigate how effective the grid structures are in providing EMI shield, and develop an analytical model to predict the shielding effectiveness.

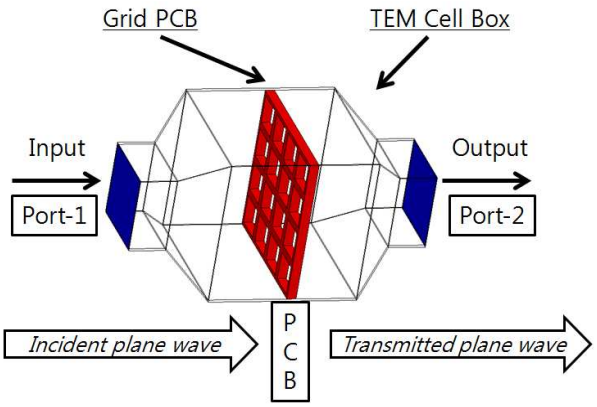
The shielding effectiveness (SE) of a barrier is defined as the ratio of the incident wave to the transmitted wave, and is used to measure the effectiveness of shielding against EMI. The shielding effectiveness of the barrier for electric field is defined, in decibels, as:

$$\mathrm{SE} = -20\log\left|\frac{E_i}{E_t}\right|, \qquad (8)$$

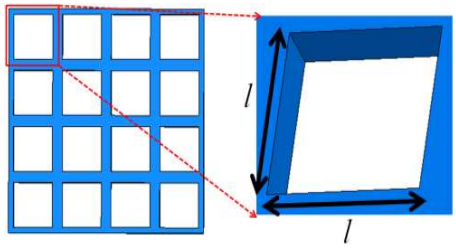
where E_i and E_t are the incident and transmitted electric fields, respectively [21]. The plane-wave shielding effectiveness is usually measured using a coaxial test fixture, however, the results are sensitive to the amount of air-gap between the sample and the coaxial line, and the contact resistances. As a result, transverse EM (TEM) cell based measurement or simulation method is used [22, 23]. To measure plane-wave shielding effectiveness of the proposed grid using 3D EM simulator, the transverse EM (TEM) cell as shown in Fig. 16(a) is designed. The TEM cell consists of a section of rectangular coaxial transmission line tapered down at each end to match 50 ohm transmission line. The incident plane wave is injected at port-1 and the transmitted wave through the grid is measured at port-2.

For a single slot with a dimension equal to or less than a half wavelength, the SE in decibels is equal to (9)

$$\mathrm{SE} = 20\log(\frac{\lambda}{2l}) = 20\log(\frac{c}{2l}) - 20\log(f), \qquad (9)$$



(a)



(b)

Fig. 16. The simulation setup to measure the shielding effectiveness of the grid structure (a) The TEM cell enclosure model [22], (b) the slot size definition of the grid structure on a PCB.

where λ is the wavelength, l is the dimension of the slot, and c is the speed of light in a vacuum [21]. The grid structure proposed in this work consists of multiple slots as shown in Fig. 16(b).

We compare the SE with several cases of different aperture sizes, as shown in Fig. 16(b). The grid PCB consists of 16 unit block cells. The length of each unit block cell is same. Different l values of 0.508, 0.445, 0.381 and 0.201 cm correspond to POMs of 36, 51, 64 and 90, respectively. 3D EM simulation was performed for the TEM cell setup in Fig. 16(a) over the frequency range of 10 MHz to 1 GHz. The EM simulation results in Fig. 16 show that the SE is inversely proportional to the grid size, in other words, effectiveness of EM shielding is higher for grid structures with higher percentage of metal area.

Based on the 3D EM simulation results and the basic model of SE of Eq. (9), an analytical Eq. (10) is proposed to predict the SE of the grid structure for different slot and grid sizes.

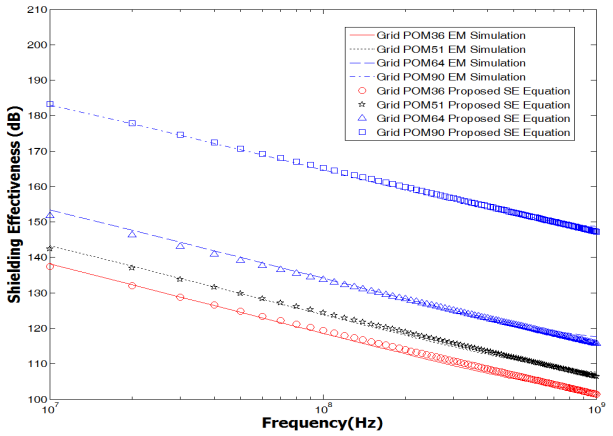


Fig. 17. The shielding effectiveness of the proposed grid structure for different POMs. Comparison of the results from 3D EM simulation and the proposed analytical equation.

$$\mathrm{SE}_{\mathrm{dB}} = 20\left(K + \log\left(\frac{c}{2l}\right) - 0.9\log(f)\right) - 20\log(2N^2),$$
$$K = 1.9\exp(-246.6l^{5.7}). \qquad (10)$$

where K represents the offset values from multiple apertures using EM simulation at the low frequency, l is the grid size in cm, N is the number of grid cells on a PCB, and c is the speed of light in a vacuum. The comparison of the results from 3D EM simulation and the proposed analytical equation is shown in Fig. 17.

V. CONCLUSIONS

In this paper, we propose a 2D TLM-based equivalent circuit model for the power integrity analysis of grid structures on a PCB. The grid structure is divided into three types of unit cells considering the fringe capacitance. To further improve the accuracy of the model, the effect of the probing ports is also included in the model. The proposed model for the grid structures has been verified by measurement and 3D EM simulation. In order to predict the EMI shielding effectiveness of the grid structure, we propose an analytical model based on 3D EM simulation with the TEM cell enclosure model. Using the proposed model, we can optimize power integrity of the PCB-Package-IC system, including the decoupling capacitor insertion for various structures in mobile systems.

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