

Low Drop-Out (LDO) Voltage Regulator with Improved Power Supply Rejection

Ho-Joon Jang, Yong-Seong Roh, Young-Jin Moon, Jeongpyo Park, and Changsik Yoo

Abstract—The power supply rejection (PSR) of low drop-out (LDO) voltage regulator is improved by employing an error amplifier (EA) which is configured so the power supply noise be cancelled at the output. The LDO regulator is implemented in a 0.13- μm standard CMOS technology. The external supply voltage level is 1.2-V and the output is 1.0-V while the load current can range from 0-mA to 50-mA. The power supply rejection is 46-dB, 49-dB, and 38-dB at DC, 2-MHz, and 10-MHz, respectively. The quiescent current consumption is 65- μA .

Index Terms—Low drop-out regulator, error amplifier, power-supply rejection

I. INTRODUCTION

The supply voltage of a system-on-chip (SoC) is generally generated from an external supply voltage as shown in Fig. 1. First, the external supply voltage level is converted to another level with a switching DC-DC converter to get high power efficiency [1]. Because the output voltage of a switching DC-DC converter can have large ripple, a low drop-out (LDO) regulator is followed to reject the ripple noise of the switching converter.

Because one of the main purposes of using a LDO regulator is to reject the ripple of a switching converter, the power supply rejection (PSR) is very critical. Higher DC gain of the error amplifier (EA) of a LDO regulator

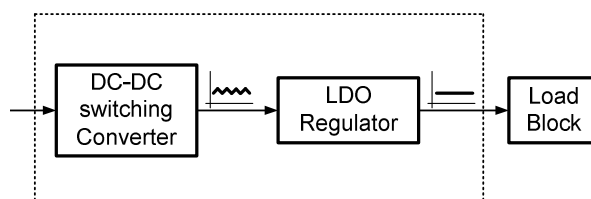


Fig. 1. Generation of power supply voltage.

can improve the PSR at DC. The PSR at higher frequency, however, is very critical as well because the power supply noise has high frequency components, especially at the switching frequency of the DC-DC converter preceding the LDO regulator. Moreover, the switching frequency of a DC-DC converter is desired to be high to reduce the size of reactive components, which increases the ripple frequency [2]. In order to have good PSR at high frequency, the DC gain and bandwidth of the EA of a LDO regulator have to be large, which is very challenging.

This paper describes a LDO regulator with improved PSR at high frequency. The EA of the LDO regulator is composed of multiple stages which are designed so the noise of the external power supply line can be cancelled and does not appear at the output.

Section II and Section III review the conventional LDO regulator and previously proposed techniques to improve the PSR, respectively. Section IV describes the proposed LDO regulator in detail and its measurement results are given in Section V. Finally Section VI concludes this paper.

II. CONVENTIONAL LDO REGULATOR

As shown in Fig. 2, a LDO regulator is composed of a

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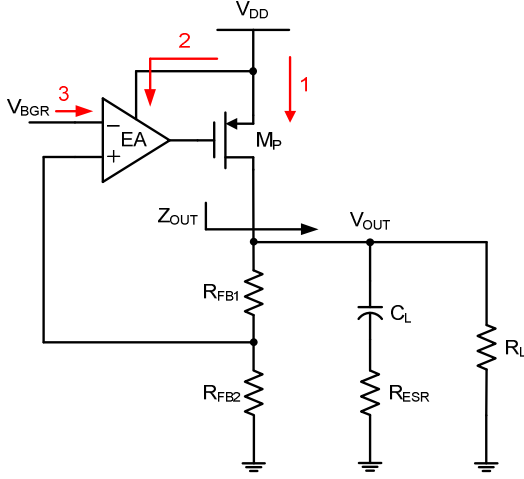


Fig. 2. Coupling paths of power supply noise to the output of LDO regulator.

power transistor M_P and EA which compares the feedback voltage with the reference voltage V_{BGR} . The noise on the external power supply V_{DD} can be coupled to the output of the LDO regulator through the power transistor (path 1), EA (path 2), and the reference voltage (path 3) as shown in the figure.

The small-signal gain of the path 1 can be represented as [3];

$$\left. \frac{V_{out}}{V_{DD}} \right|_{path1} = \frac{g_{mp} Z_{out}}{1 + g_{mp} Z_{out} \beta A_{EA}} \approx \frac{1}{\beta A_{EA}}. \quad (1)$$

where g_{mp} , Z_{out} , β , and A_{EA} are the transconductance of the power transistor M_P , load impedance at the output node, feedback factor $R_{FB2}/(R_{FB1} + R_{FB2})$, and the gain of the EA, respectively. From this equation, it can be seen the power supply noise coupling through the path 1 is determined by the feedback factor and the gain of the EA. The PSR may be deteriorated at high frequency due to the limited bandwidth of the EA.

The gain of the path 2 can be found in the same manner as that of the path 1 and the result is;

$$\left. \frac{V_{out}}{V_{DD}} \right|_{path2} = \frac{g_{mp} Z_{out} A_{EA} V_{DD}}{1 + g_{mp} Z_{out} \beta A_{EA}} \approx \frac{A_{EA} V_{DD}}{\beta A_{EA}}. \quad (2)$$

where A_{EA_VDD} is the gain from the power supply of the EA to its output which is the gate of the power transistor. The ripple of the power supply through the path 2 is first coupled to the gate of the power transistor M_P before

affecting the output. Because the gate capacitance of the power transistor is generally very large, its gate node voltage is free of ripple at high frequency and therefore the supply noise coupling through the path 2 becomes less problematic at high frequencies.

The gain of the path 3 is given as;

$$\left. \frac{V_{out}}{V_{DD}} \right|_{path3} = \frac{g_{mp} Z_{out} A_{EA}}{1 + g_{mp} Z_{out} \beta A_{EA}} \cdot \frac{V_{BGR}}{V_{DD}} \approx \frac{1}{\beta} \cdot \frac{V_{BGR}}{V_{DD}}. \quad (3)$$

From the above Eq. (3), it is clear the power supply noise coupling through the path 3 is dominated by the PSR of the bandgap reference circuit itself.

III. PREVIOUS TECHNIQUES FOR IMPROVED POWER SUPPLY REJECTION

As described in the previous section, the power supply noise can be coupled to the output of a LDO regulator through multiple paths and therefore it is generally very complicated to get a good PSR.

The simplest way of improving the PSR is to place a low-pass RC filter on the external power supply line as shown in Fig. 3(a) [4]. The RC filter reduces the ripple noise of the external power supply before being delivered to the input of the LDO regulator. The resistor of the RC filter, however, causes the voltage drop on the power supply line, which can make the design of LDO very challenging. A common-gate nMOS transistor may be inserted between the external power supply input and the pMOS power transistor as shown in Fig. 3(b) [5]. The nMOS transistor consumes voltage headroom and may require large silicon area if the voltage headroom is to be minimized.

In [6], the ripple on the external supply line is coupled to the gate of the power transistor using a feed-forward amplifier which equalizes the phase delay of the compensating signal path with that of the main path of the power supply noise coupling. However, the feed-forward amplifier cannot perfectly equalize the phase delay at all frequencies and operation conditions, which limits the improvement of PSR.

In [7], the diode connected gain stage is inserted between the power transistor and the error amplifier, which injects the supply noise to gate of the power transistor. The supply noise is not transferred to the

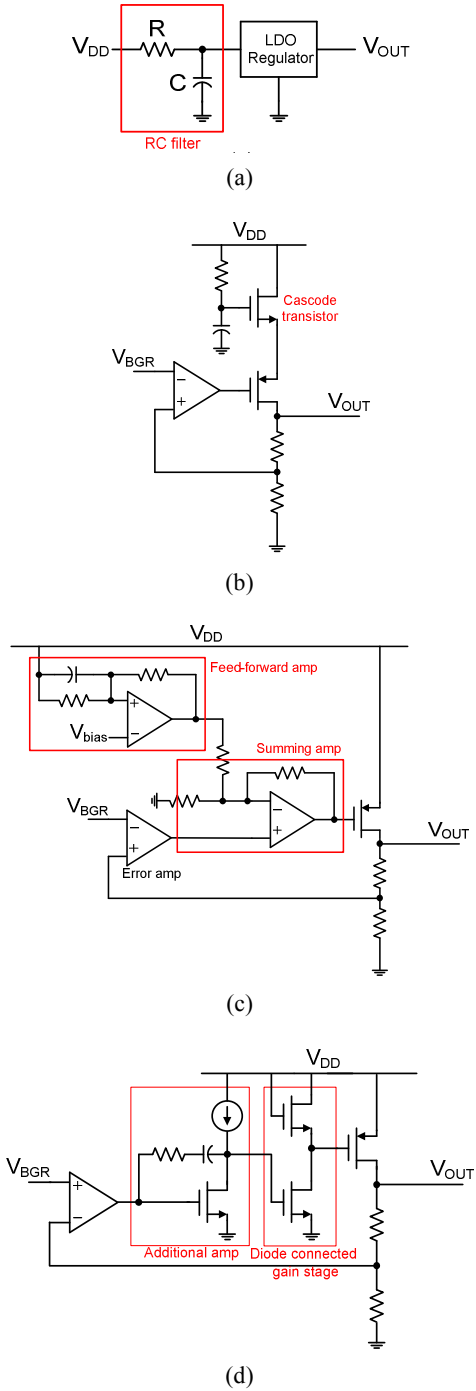


Fig. 3. Power supply rejection improvement techniques with (a) RC-filter on external supply line, (b) cascode transistor, (c) feedforward ripple cancellation, (d) diode connected gain stage.

output due to the unaffected gate-source voltage of the power transistor. Because the diode connected gain stage reduces the loop gain, the additional gain stage is required, which requires a complex frequency compensation technique.

IV. POWER SUPPLY REJECTION (PSR) IMPROVED LDO REGULATOR

The noise of the external power supply line can be rejected if the exactly the same amount of noise can be coupled to the gate of power transistor. This is the basic background knowledge of the proposed LDO regulator shown in Fig. 4. To perform the function, the diode connected gain stage consisting of \$M_7\$, and \$M_8\$ uses a power transistor driver, which reduces the loop gain and regulation characteristics. The additional gain stage and the bleeding current sources \$I_{bleed1}\$ and \$I_{bleed2}\$ are added to increase voltage gain [8]. The EA of the LDO regulator consisting of three stages is designed so the noise of the external power supply line is cancelled.

The noise of the external supply is coupled to the output of the first stage which drives the gate of the pMOS transistor \$M_5\$ [9]. Through this path, the supply noise is delivered without much attenuation over a wide frequency range because the parasitic capacitor of the first stage output is not large. The output of the second stage is free of the supply noise because the noises on the gate and source nodes of the transistor \$M_5\$ cancel each other. Therefore, the output of the third stage is coupled to the external power supply noise only by the transistor \$M_8\$. Because the transistor \$M_8\$ is configured as a diode, the output impedance of the third stage is very small and the external power supply noise appears at the output of the third stage without much attenuation over a wide frequency range as well. The gate-source voltage of the power transistor is free of the external power supply noise and the PSR of the LDO regulator is improved.

The PSR of the proposed LDO regulator is derived as in the Eq. (4) shown at the bottom of this page.

$$\frac{v_{OUT}}{v_{DD}}(s) = g_{mp} Z_{TOT}(s) \times \frac{1 - 1/\{1 + s(C_{P3}/g_{m8})\} + A_2(s)A_3(s)s(r_{o2}/r_{o4})C_{P1}/\{s(r_{o2}/r_{o4})C_{P1} + 1\}}{1 + g_{mp} Z_{TOT}(s)A_1(s)A_2(s)A_3(s)\beta(s)} \quad (4)$$

where $A_1(s) = \frac{g_{m1}(r_{o2}/r_{o4})}{1 + s(r_{o2}/r_{o4})C_{P1}}$, $A_2(s) = \frac{g_{m5}}{g_{m6} + sC_{P2}}$, $A_3(s) = \frac{g_{m7}}{g_{m8} + sC_{P3}}$, $Z_{TOT}(s) = \beta(s) // \frac{1}{sC_L} // R_L$, and $\beta(s) = \frac{R_{FB2}}{R_{FB1} // \frac{1}{sC_Z} + R_{FB2}}$.

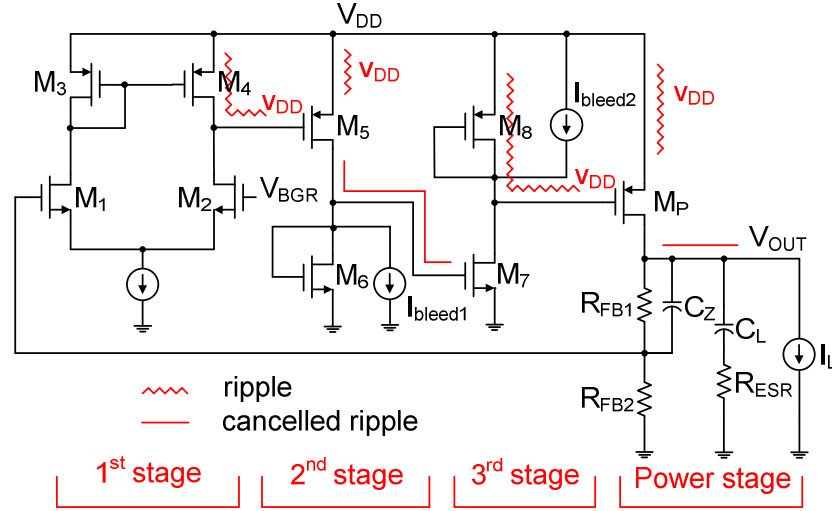


Fig. 4. Proposed LDO regulator.

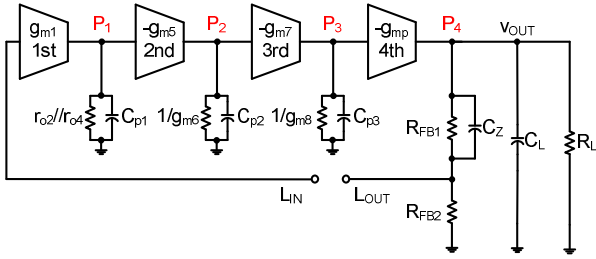
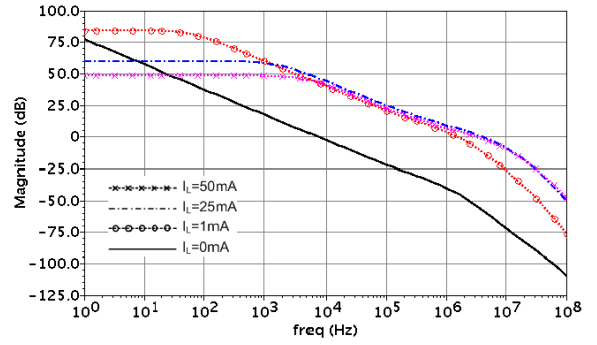


Fig. 5. Small-signal equivalent circuit of the proposed LDO regulator for stability analysis.

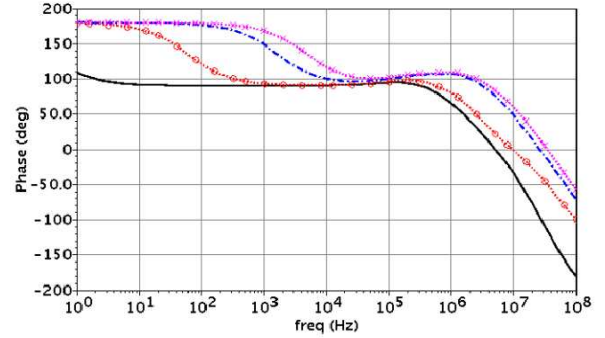
Because the LDO regulator has four stages including the power transistor, its stability has to be carefully analyzed. The loop gain of the LDO regulator can be derived with the small signal equivalent circuit shown in Fig. 5 and the result is;

$$L(s) = \frac{g_{m1}(r_{o2}/r_{o4})(g_{m5}/g_{m6})(g_{m7}/g_{m8})g_{mp}R_L\beta(s)}{(1+s(r_{o2}/r_{o4})C_{p1})\left(1+\frac{sC_{p2}}{g_{m6}}\right)\left(1+\frac{sC_{p3}}{g_{m8}}\right)(1+sR_L C_L)} \quad (5)$$

The loop gain has four poles and one zero due to $\beta(s)$ in the loop gain as shown in the above Eq. (5). The equivalent series resistor (ESR) R_{ESR} of the capacitor C_L is neglected because a ceramic capacitor is used which is known to have small ESR. The pole at the LDO output P_4 is the dominant pole of the loop. The poles at the outputs P_2 and P_3 of the second and third stages can be neglected because they are at high frequency. The zero generated by the capacitor C_Z compensates for the phase shift due to the pole at the output of the first stage. The loop gain



(a)



(b)

Fig. 6. Simulated loop gain of the LDO regulator (a) magnitude, (b) phase shift versus the frequency.

can be reduced to two poles and one zero system. Therefore the proposed scheme does not require a large compensation capacitor. The loop gain of the LDO regulator is simulated for various values of load current and the result is shown in Fig. 6.

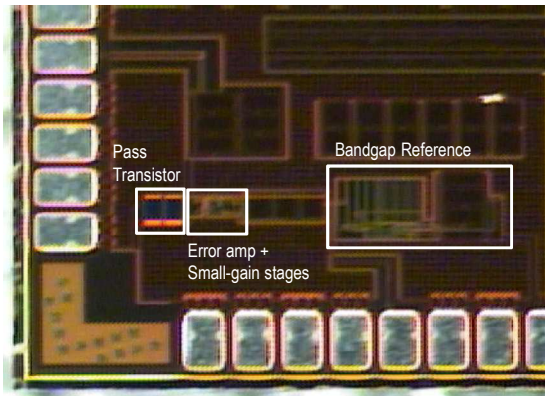
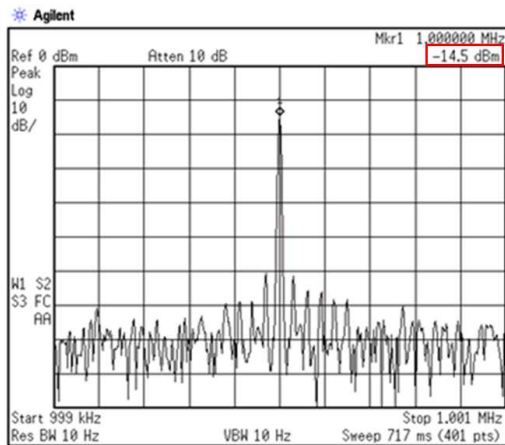
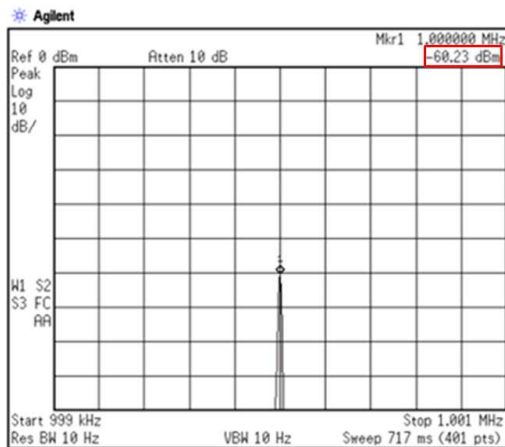


Fig. 7. Microphotograph of the LDO regulator.



(a)



(b)

Fig. 8. Measured AC power under the condition of $V_{DD}=1.2$ V coupled with 1MHz and $I_L=30$ mA at (a) input supply voltage,, (b) output voltage.

V. MEASUREMENT RESULTS

The proposed LDO regulator has been implemented in a 0.13- μ m standard CMOS technology and the chip

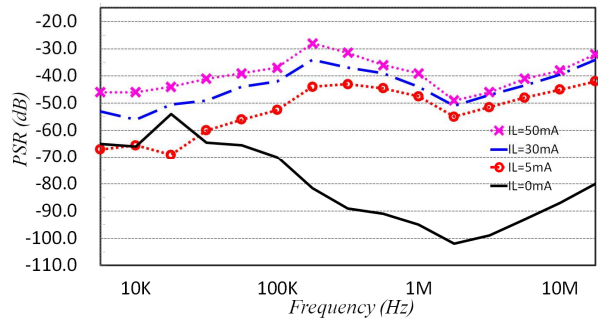


Fig. 9. Measured PSR for different load conditions.

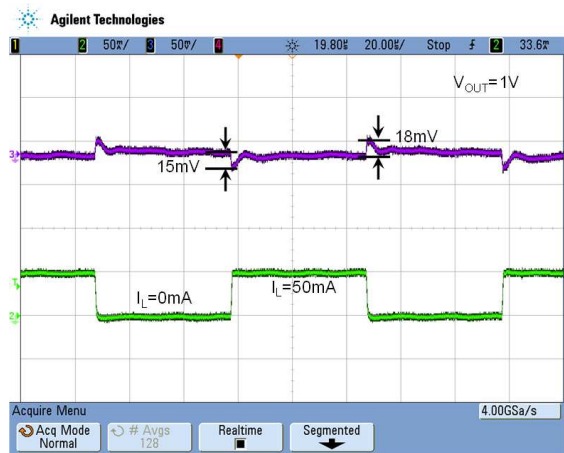


Fig. 10. Measured load transient response.

microphotograph is shown in Fig. 7. The total area of the LDO is 0.4- mm^2 . The output voltage is 1.0-V with the nominal external supply voltage level 1.2-V and the load current is from 0-mA to 50-mA. An off-chip ceramic output capacitor 4.7- μ F is used. The LDO regulator including a bandgap reference circuit consumes only 65- μ A quiescent current.

To measure the PSR of proposed LDO, an AC coupled supply voltage is fed into the LDO through Bias-T. The PSR is calculated by subtraction of input and output AC power as in [6]. Fig. 8 shows the measurement of the input and output power at 1.2 V supply coupled with 1 MHz sine wave and load current of 30 mA. The measured PSR for various load current conditions is shown in Fig. 9. The minimum PSR is 46-dB at DC, 49-dB at 2-MHz, and 38-dB at 10-MHz. The PSR at low frequency is degraded for larger load current because the loop gain is decreased. The load current is changed from 0-mA to 50-mA and vice-versa to see the ripple of the output voltage due to the load transient. As shown in Fig. 10, the output voltage level changes by 15-mV and 18-

Table 1. Performance summary of the LDO regulator

	[6]	[7]	This work
Technology [μm]	0.13	0.35	0.13
V_{DD} [V]	1.15	3.1	1.2
V_{OUT} [V]	1	2.8	1.0
Max. load current [mA]	25	100	50
Quiescent current [μA]	50	N.A.	65
Line regulation [mV/V]	N.A.	N.A.	4.25
Load regulation [mV/mA]	0.048	0.05	0.13
PSR [dB]	DC	60	70
	2-MHz	80	N.A.
	10-MHz	55	N.A.

mV for the change of load current from 0-mA to 50-mA and from 50-mA to 0-mA, respectively. The performance of the LDO regulator is summarized and compared with other works in Table 1.

VI. CONCLUSIONS

The power supply rejection of a linear LDO regulator is improved by configuring the error amplifier so the power supply noise can be cancelled at the output. The LDO regulator implemented in a 0.13- μm CMOS process achieves 46-dB, 49-dB, and 38-dB power supply rejection at DC, 2-MHz, and 10-MHz, respectively.

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