Novel Hierarchical Test Architecture for SOC Test Methodology Using IEEE Test Standards

Dongkwan Han, Yong Lee, and Sungho Kang

Abstract—**SOC test methodology in ultra deep sub-micron (UDSM) technology with reasonable test time and cost has begun to satisfy high quality and reliability of the product. A novel hierarchical test architecture using IEEE standard 1149.1, 1149.7 and 1500 compliant facilities is proposed for the purpose of supporting flexible test environment to ensure SOC test methodology. Each embedded core in a system-on-a-chip (SOC) is controlled by test access ports (TAP) and TAP controller of IEEE standard 1149.1 as well as tested using IEEE standard 1500. An SOC device including TAPed cores is hierarchically organized by IEEE standard 1149.7 in wafer and chip level. As a result, it is possible to select/deselect all cores embedded in an SOC flexibly and reduce test cost dramatically using star scan topology.**

Index Terms—**IEEE standard 1149.1, IEEE standard 1149.7, IEEE standard 1500, SOC, test architecture**

I. INTRODUCTION

SOC is an increasing trend in semiconductor design and manufacturing process. New materials and complex process are introduced for integrated circuits so as to employ a single chip combining high speed logic, low power logic, analog and I/O logic application. However, the emergency of new defect types and reliability problems from the new design and manufacturing process requires a variety of test methods to ensure high quality at reasonable test cost [1].

Test complexity issues pertaining to varying parametric distribution and multiple domain test conditions are solved by testing methodology using adaptive test. Economic scaling of test using multi-site test, concurrent test and test time/data volume reduction methods counteract the expenses with increasing test pattern, conditions and design complexity.

This paper focuses on developing an on-chip design for testability (DFT) test architecture applying flexible test environment which can handle a number of embedded cores in an SOC. The hierarchical test architecture realizes a flexible test environment in structural test mode with IEEE standard 1149.1, 1149.7 and 1500.

The outline of this paper is as follows. Section II reviews the IEEE test standards used to this paper. Section III describes the new hierarchical test architecture in detail. The experimental results are presented in Section IV, followed by the conclusion in Section V.

II. IEEE TEST STANDARDS

The more complex the SOC designs are getting, the harder we test those big designs. The more complicated methods are needed to handle embedded cores for test and debug, especially considering the design and test overhead generating the cost issues. To solve the problems and for easy implementation, researchers have reported SOC test architectures [2]. The majority of the researches used a controller to reduce pins for testing; moreover, the most of the controllers are made with

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IEEE standard 1149.1 (TAP.1) [3]. With the controller, test process control and pin attribution control were derived. IEEE standard 1500 enables test reuse as well as integration for embedded cores and associated circuitry [4]. However, IEEE standard 1149.1 and 1500 are insufficient to address the recent changes in integrated circuit trends.

IEEE standard 1149.7 (TAP.7) provides not only reduced pins as a test access port but also enhanced functionality complementary IEEE standard 1149.1 regard to controlling multi-core on chip level and multi-chip on board for test and debug [5].

III. HIERARCHICAL TEST ARCHITECTURE

An SOC includes a plurality of cores in a single chip. Because of the constant time-to-market pressure, a large number of chip designers and integrators reuse existing designs to make complex SOC in a limited time budget. The cores embedded in the SOC are separately designed and tested through IEEE std. 1149.1 and 1500 before being combined in an SOC chip. Once an SOC chip is integrated with several TAPed cores, then the test and debugging scheme of an SOC chip should be compatible with IEEE standards from chip level test using boundary scan register to core debugging scheme with the test data register of embedded cores. The management method compliant with IEEE test standards for multiple TAP controllers in a chip is needed to test and debug at the chip level.

In this paper, we propose a hierarchical test architecture which is based on the star scan topology of IEEE standard 1149.7. The hierarchical test architecture can support the test and debug point of view in the chip level test and debug as shown in Fig. 1. Chip level TAP controller (CLTAPC) compliant with T0 TAP.7 in IEEE standard 1149.7 selects at least one core of the embedded TAP controllers (EMTAPC) to be tested. The test results of picked cores are evaluated through the daisy-chained TDI-TDO connection. T0 TAP.7 includes core selection logic which can be a test data register or an instruction register. The embedded cores using IEEE standard 1149.1 and 1500 for test or debug are linked with daisy-chained TDI-TDO connections by using core selection values of core selection logic and bypass logic. To the test and debug point of view the one or multiple embedded cores can be selected.

The automatic test equipment (ATE) can act like the hub and the node is regarded as a DUT. The ATE broadcasts the test input data to several DUTs using channel sharing method of the ATE. The bandwidth required to interface the ATE and one DUT is dramatically reduced by the hierarchical test architecture using only TAP and input TAM. Just one pin, test data output (TDO) is used to measure the sink value which is generated from test data compressor in each core. In addition, this star scan topology makes the ATE easy to find a fail DUT. The hierarchical test architecture is easy to manage connected DUTs because of its simplicity in testability. The failure can be easily located logically in a star scan topology and therefore is easy to troubleshoot also. All input and output pins are shared with the same channels of the ATE. Then a direct addressable method is needed to prevent drive conflicts among the DUTs.

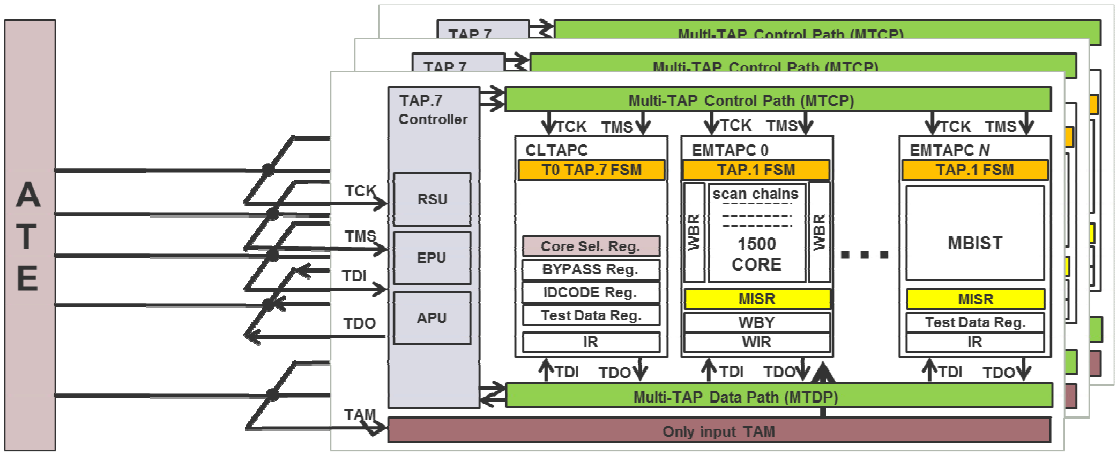

Fig. 1. The proposed hierarchical test architecture.

Generally, the SOC includes chip identification (CHIP_ID) code register which uniquely identifies each DUT at the wafer level. The process and defect information is informed by identification code. There are several methods to store the code at the chip level. Fusible elements and programmable elements such as EEPROMs are widely used. CHIP_ID can be used TCA for T3 TAP.7. T3 TAP.7 uses this codes and SSD to address one DUT in star network. This means that a DUT will be selected only if the value of TCA is equal to address payload of SSD.

IV. EXPERIMENTAL RESULTS

The proposed architecture for manufacture test works with the following test sequence. At first the embedded all cores are tested in regular sequence with TAP.1 after setting star scan topology with T3 TAP.7 controller. All DUTs are tested simultaneously by the star scan test topology at this time. A series of these core test schemes is repeated until all cores are tested. After testing of all cores is complete, the concurrently tested DUTs are checked with T3 TAP.7. In the same manner as cores test a series of the evaluations of DUTs are repeated until all DUTs are checked.

The MISR dramatically reduces output test data of scan design. The pass/fail results of embedded cores of DUTs can be achieved in chip and wafer levels for high volume manufacturing. However, it is difficult to recover the information lost during signature compaction. The diagnostics scheme with MISR is based on the bypass mode which unloads the scan cell information directly.

1. Test Cost Reduction

In order to compare the effectiveness of the proposed test architecture with the conventional method [2], several ITC'02 SOC test benchmarks are used. With a target ATE with 512 channels, each of which can be shared by 4 probes, Table 1 lists the test cost reduction ratios of the conventional method and the proposed test architecture. The proposed architecture is easily scalable and shows a significant test cost reduction with small additional test time.

Table 1. Performance Comparison

ITC'02	TAM width (32)						
	Conventional [2]			Proposed			
	Test time (cycle)	# of test sites	Test time per DUT (cycle)	Test time (cycle)	# of test sites	Test time per DUT (cycle)	Test cost reduction ratio
P22810	226364	25	9054	401449	97	4138	54%
P34392	544879	25	21795	646244	97	6662	69%
P93791	886183	25	35447	1078340	97	11116	68%
T512505	5256830	25	210273	5431915	97	55999	73%

2. Adaptive Test

Adaptive test changes test conditions, test flow, test content and test limits at the die level based on manufacturing test data and statistical data analysis. The flexible test environment and real-time test analysis is essential to achieve lower test costs, higher yields and better quality & reliability. The hierarchical test architecture is suitable for supporting adaptive test by selecting one or more than one EMTAPCs and debugging environment for analysis.

3. Design Consideration

Since the proposed architecture is composed of a simple structure including TAP.1 and TAP.7 controller units, a comparator and bypass logic, the size of the architecture is very small. In addition, the architecture adapts the existing test and debug scheme with no modifications. In our test case, which has 10 embedded cores and a 32-bit CHIP_ID, the gate count of the proposed architecture was approximately 1500. The number of embedded cores has not too much effect on the gate count.

4. 3D-SIC

As if the hierarchical test architecture is applied to support multi-site test and SOC core test and debug, it can be applied to the 3D-stacked integration chip (3D SIC) with through silicon via (TSV) technology, one of the chip integration technology. The 3D SIC includes several independent ICs which have its own TAP controller. The hierarchical test architecture can select one embedded IC and connect the TAP pins of 3D SIC to the TAP pins of the selected IC.

V. CONCLUSIONS

SOC test methodology is definitely required to screen new defect types and reliability problems from new design and manufacturing process. The hierarchical test architecture is seamless new managing method to handle the plenty of embedded cores for testing and debugging with the feasibility of already existing test/debug methods or software. In addition, we have introduced new test architecture for multi-site testing using star scan topology implemented by IEEE test standards. The hierarchical test architecture is compliant with IEEE test standards so that it is not needed to use added test ports and modify embedded cores.

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