A Digital Readout IC with Digital Offset Canceller for Capacitive Sensors

Dong-Hyuk Lim, Sang-Yoon Lee, Woo-Seok Choi, Jun-Eun Park, and Deog-Kyoon Jeong

***Abstract*—A digital readout IC for capacitive sensors is presented. Digital capacitance readout circuits suffer from static capacitance of sensors, especially single-ended sensors, and require large passive elements to cancel such DC offset signal. For this reason, to maximize a dynamic range with a small die area, the proposed circuit features digital filters having a coarse and fine compensation steps. Moreover, by employing switched-capacitor circuit for the front-end, correlated double sampling (CDS) technique can be adopted to minimize low-frequency device noise. The proposed circuit targeted 8-kHz signal bandwidth and oversampling ratio (OSR) of 64, thus a 3rd-order ΔΣ modulator operating at 1 MHz was used for pulse-density-modulated (PDM) output. The proposed IC was designed in a 0.18-μm CMOS mixed-mode process, and occupied 0.86 × 1.33 mm^2. The measurement results shows suppressed DC power under about -30 dBFS with minimized device flicker noise.**

***Index Terms*—Capacitive sensor, digital offset canceller, sigma-delta modulator, correlated double sampling**

I. INTRODUCTION

Capacitive sensors are widely used in many applications such as bio-medical sensors [1], micro-phones [2, 3], or touch screen panels [4], because they are hardly impacted by temperature variations and they can be produced with a high accuracy. Most capacitive sensors generate low-frequency signals ranging from a few Hz to a few kHz [1-3]. This fact, however, makes it difficult to design a readout IC in two aspects.

First, capacitive sensors have nominal capacitance values and provide relatively small capacitance variations. The static offset by this nominal capacitance, especially in single-ended sensors, limits the dynamic range of the circuit. To maximize the dynamic range of the ADC and to keep the charge amplifier's output from being saturated without any loss in signal band, a high pass filter with a very low cut-off frequency is required. If a high pass filter is implemented with common RC filter as shown in Fig. 1, the chip size should be extremely increased. A pseudo-resistor using the sub-threshold current of the MOS transistor has been studied to overcome this problem [1]. The MOS transistor in the threshold region, however, becomes very sensitive to temperature or process variations that cause signal distortion.

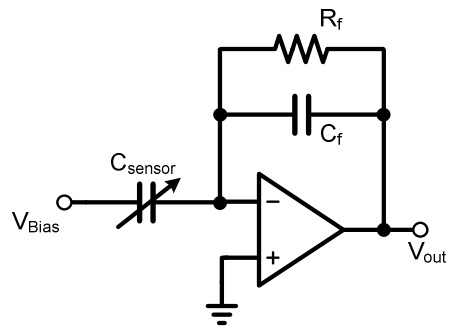

Fig. 1. Conventional capacitance-to-voltage converter using RC feedback components.

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The other aspect is that a low-frequency signal band can be disturbed by device flicker noise [5]. In order to reduce the flicker noise, analog front-end circuits usually adopt chopper-stabilized amplifiers [6-8]. A chopper-stabilized amplifier, however, is easily impacted by non-ideal effects of the switches such as charge injection to the input node or non-linearity. These non-idealities generate harmonics of the chopping frequency, which can be folded back into the signal band. Enlarging the size of the input differential pair of an op-amp can be another option to suppress the flicker noise but has a limit due to the whole chip area.

This paper proposes a digital capacitive readout IC with a digital offset canceller composed of a digital filter and a digital-to-analog converter (DAC). The digital offset canceller occupies small area and functions as a high pass filter with a cut-off frequency as small as 10 Hz. Moreover, it is obvious that the digital offset canceller is insensitive to PVT variations. In addition, switched-capacitor circuit is employed for a capacitance-to-voltage converter to suppress the low-frequency noise. Owing to the discrete-time operation of the switched-capacitor circuit, the front-end converter can utilize the correlated double sampling (CDS) technique for the flicker noise reduction.

This paper is organized as follows. Section II depicts the overall system and the architecture of the proposed IC. Section III describes how each block was implemented and what should be considered. Section IV and V show the measurement results and conclusion.

II. ARCHITECTURE

Fig. 2 shows the block diagram of the proposed interface IC. The capacitance value of a capacitive sensor can be affected by physical pressure, acoustic pressure, or electric field change according to the proximity. Such capacitance variation in a sensor triggers the change in a charge amount present at an input node, and the switched-capacitor buffer converts it into a voltage signal. A following third-order ΔΣ modulator translates this analog signal to a pulse-density-modulated (PDM) digital output stream, which has minimized quantization noise in the signal band.

As described in Introduction, the static charge flowing through the input node, which is the signal we are not interested in, may limit the performance of the readout IC, so an offset cancellation feedback loop is required to cancel it and maximize the dynamic range. The proposed digital offset canceller makes the best use of the digital output to remove the DC signal in the input, and it produces two types of output: one is for the coarse calibration, and the other is for fine tuning. The coarse control signal is applied to the analog front-end directly, and the fine control data pass the DAC. The coarse control signal makes the C/V converter work in a proper operating region as soon as possible, and the fine control signal maximizes the dynamic range of the IC.

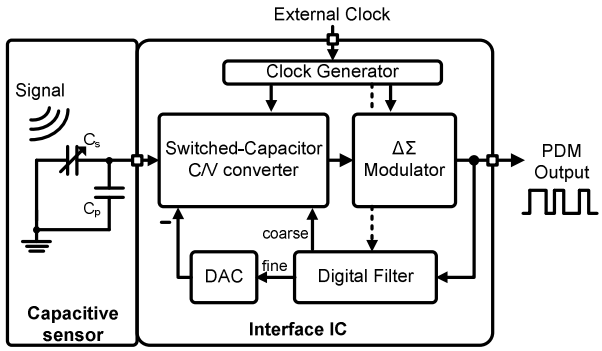


Fig. 2. Overall architecture of the proposed digital capacitance readout circuit.

The proposed IC was designed for digital microphones, and therefore the signal bandwidth of the input was set to the audible band, 8 kHz. All blocks except the DAC operate at the over-sampling clock frequency, 128 times higher than signal bandwidth, which comes from the oversampling ratio (OSR) of 64 in the ΔΣ modulator. The clock generator produces a non-overlapping clock and provides it to a switched-capacitor buffer and a ΔΣ modulator.

III. CIRCUIT DESCREPTION

1. Switched-Capacitor C/V Converter

The front-end converter senses charge variation of a sensor and converts it to an analog voltage signal. This operation has been mostly performed using continuous-time analog circuits. The continuous-time circuits usually require high-valued resistors to cancel a DC offset signal. The proposed converter, in contrast, operates in the discrete-time domain using a switched-capacitor as shown in Fig. 3. Although the signal coming out of a

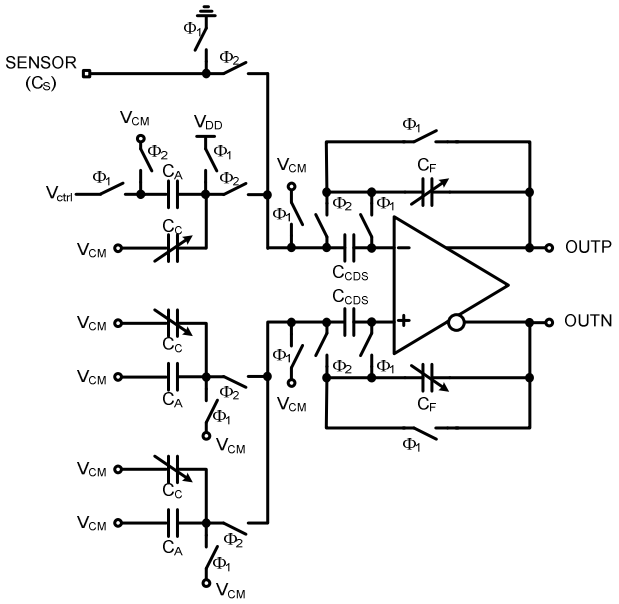


Fig. 3. The proposed C/V converter using switched-capacitor circuit.

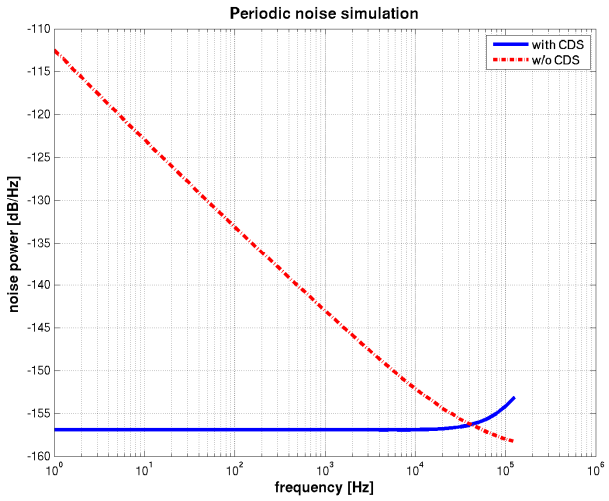


Fig. 4. The simulated input-referred noise of the front-end amplifier.

sensor is single-ended, the circuit is designed to have a fully-differential structure to increase power supply rejection (PSR).

In the main path, the top branch in Fig. 3, at Φ_1 phase, the charge stored in the capacitive sensor is reset. At the end of Φ_2 phase, the sensor's charge changes to $V_{CM}(C_{S,static}+\Delta C_S[n])$, where $C_{S,static}$ represents the static capacitance of the sensor, and $\Delta C_S[n]$ is the capacitance variation at n-th clock cycle. By the law of charge conservation, this amount of charge is transferred to C_F, which can be controlled externally to adjust the buffer gain.

The second path, by generating the opposite charge, removes the static charge of the sensor that may degrade the dynamic range of the op-amp. If the offset canceller controls the bias voltage of a small single capacitor, there will be a limit on the cancelling range. This compensation range can be extended by choosing a large single capacitor, but fine resolution will be sacrificed in this case. Controlling the capacitance value seems a solution that achieves fine resolution and a wide range, however, it raises the kT/C noise level when increasing the resolution. Hence, the proposed circuit compensates for the offset in two steps—a coarse tuning step for wide-range operation and a fine tuning step for higher resolution. In the coarse tuning phase, C_C is adjusted roughly to set a proper operating point. After coarse locking, the fine compensation is achieved through controlling V_{ctrl} applied to a fixed capacitor C_A. In the fine lock condition, the control values satisfy that:

$$(V_{DD} - V_{CM})C_C + (V_{DD} - V_{ctrl})C_A = V_{CM}C_{S,static} \quad (1)$$

As a result, after fine locking process, the op-amp output will include only capacitance variation information, $\Delta C_S[n]$. The two paths in the bottom are intended for the impedance matching between the input nodes of the op-amp for fully differential operation.

The rest part of the circuit around C_{CDS} is for the correlated double sampling. During Φ_1 phase, C_{CDS} stores the input offset of the op-amp, and at Φ_2 phase adds it up to transferred signal. The CDS technique can suppress the flicker noise without increasing the bandwidth of the op-amp. Fig. 4 shows the simulation result of op-amp input-referred noise using periodic noise simulation in SpectreRF. The low-frequency noise power is suppressed below -150 dB/Hz with help of the CDS.

2. ΔΣ Modulator

Several types of ADCs, such as successive approximation register (SAR), and cyclic ADC have been investigated for digital readout ICs. However, each type of ADC has some difficult requirements to implement. For example, in order to suppress quantization noise power, a SAR requires a high resolution DAC, and a cyclic ADC needs a very accurate and low

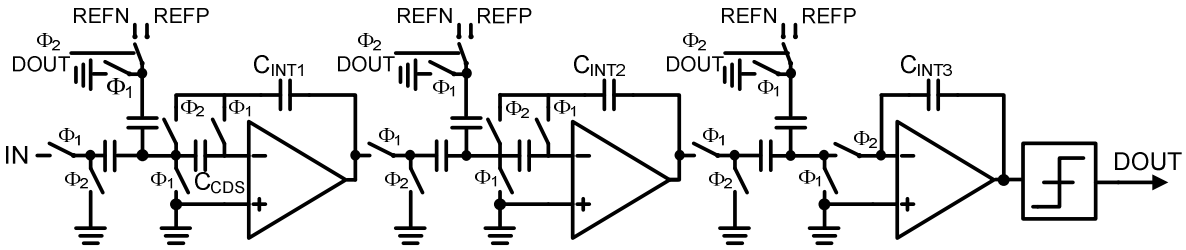


Fig. 5. Implemented 3rd-order low-pass ΔΣ modulator.

noise amplifier. A ΔΣ ADC mitigates such constraints by shaping the quantization noise. Fig. 5 represents the implemented ΔΣ modulator architecture. Although it is drawn as single-ended for simplicity, the circuit was implemented to have a fully-differential structure. A single-loop 3rd-order low-pass ΔΣ modulator digitizes the C/V converter's analog output to a 1-MHz, 1-bit data stream. Based on the target in-band noise power of -80 dB, the order of 3 and OSR of 64 are chosen [9].

Considering the kT/C noise, we choose the sampling capacitor of the first stage to be 1.25 pF. The CDS is employed in the first and the second stage to minimize the input offset of the op-amp and the flicker noise. However, the third stage does not utilize the CDS scheme for design simplicity. Since the second and the third stage have less effects on overall performance than the first stage, the second and the third stage have smaller capacitors and lower power-consuming op-amps than the first stage to optimize the chip area. For the op-amp in a switched-capacitor integrator, the folded-cascode topology is chosen because of its large gain and stability. The unity-gain bandwidth of the first stage op-amp is 15 MHz, which is sufficient for 1-MHz sampling operation.

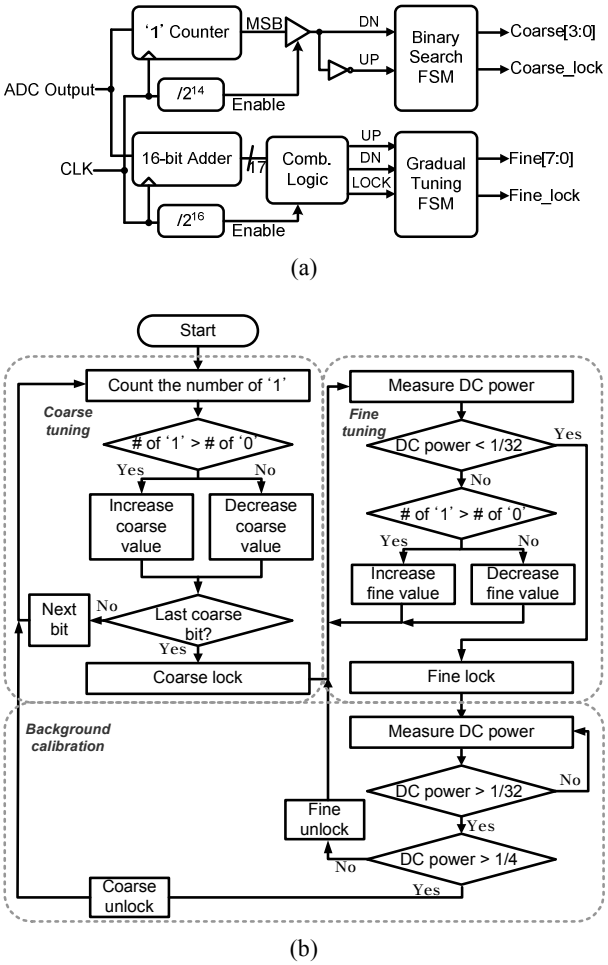


Fig. 6. The proposed digital filter (a) block diagram, (b) flowchart.

3. Digital Filter

The proposed digital filter operation is divided into two phases: a coarse tuning phase and a fine tuning phase as shown in Fig. 6. During the coarse tuning phase, a '1' counter accumulates the output of the ΔΣ modulator for 2^{14} cycles. Then, the MSB of the counter controls a finite state machine to find the nominal capacitance of a sensor. In the coarse tuning phase, binary search algorithm is adopted for fast locking. After four coarse cycles, the coarse control value will be fixed, and a coarse lock flag goes high. Although the readout circuit can sense the capacitance from the sensor after coarse locking, the fine tuning phase starts to maximize the performance of the conversion. The output of the ΔΣ modulator is added during the 2^{16} clock cycles, and the following combinational logic decides whether the output has a spectral power over 1/32 of the full scale at the frequency range lower than $f_s/2^{16}$. The 16-bit adder was chosen from the fact that the frequency band below 16 Hz (1 MHz / 2^{16}) is out of the signal band in microphone application. The value of 1/32 determines the suppressed

level of a DC offset. The decision of the DC power is made from the five MSBs of the 16-bit adder output. If the MSBs represent '00000' or '11111', the DC power can be considered sufficiently small. The fine locking occurs when *UP*, *DN* direction is changed, or when no power in the low frequency band is detected in 2^{16} cycles. After fine locking, coarse and fine control values are frozen not to affect the sensing operation afterwards. However, the filter maintains its role in the background against an environmental change. If the static value of the sensor has been changed, either fine tuning or coarse-and-fine tuning is reperformed according to the changed DC power. Even if unlocking condition is detected in background calibration, the filter measures DC power once again not to respond to measurement noise. Of course, the cut-off frequency and suppressed level are tunable according to applications.

Fig. 7 shows the behavioral simulation results explaining how the digital filter works. A sinusoidal signal is applied to verify its functionality under a signal incoming condition. And the third-order $\Delta\Sigma$ ADC is modeled in a behavioral language to verify the function-ality of the digital filter. Fig. 7(a) shows initial locking process, and Fig. 7(b) shows a coarse reset and re-locking process in case of an environmental change (step signal of DC offset at time t_1). As shown in Fig. 7, the ADC output is stuck to low or high according to the DC offset before the digital tuning is completed. After the tuning, the operating point of the ADC is moved to the center, and therefore the dynamic range can be maximized.

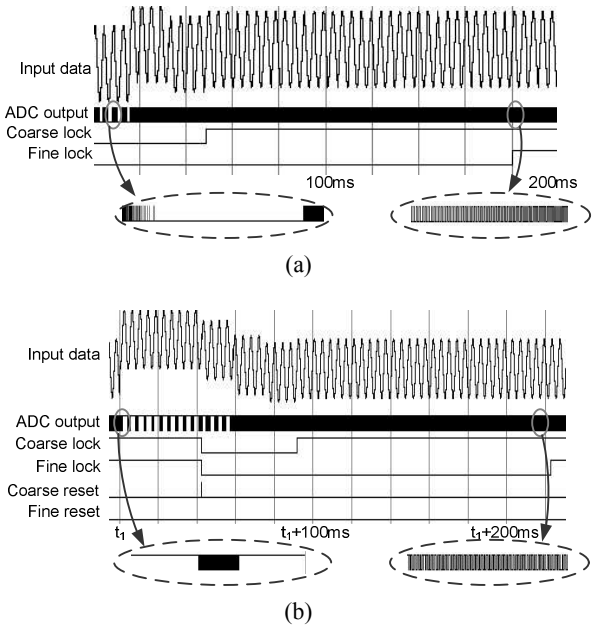
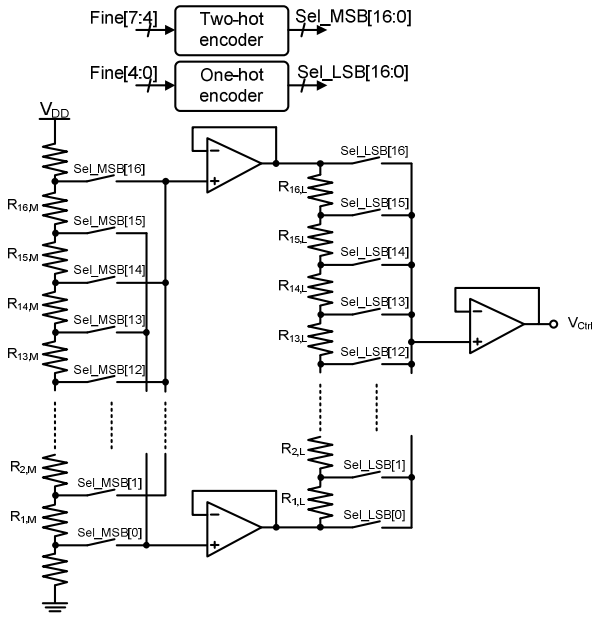


Fig. 7. Behavioral simulation of the proposed digital filter (a) Initial locking process, (b) Response of an environmental change.

4. Digital-to-Analog Converter

The DAC feeds V_{ctrl} back to the front-end converter using 8-bit fine control values. Since the performance of the DAC is not critical viewed in the system architecture, the monotonic characteristic and power consumption were the main considerations in DAC design. In order to implement an 8-bit DAC, 2-stage resistor-string type topology is selected because of its simple design and less power consumption.

Fig. 8(a) shows the implemented DAC. In the first stage, two adjacent analog values are selected among the



(a)

Fine[7:4]	Sel_MSB	Fine[4:0]	Sel_LSB
0000	00000000000000011	00000	00000000000000001
0001	00000000000000110	00001	00000000000000010
...		...	
1111	11000000000000000	01111	01000000000000000
		10000	10000000000000000
		...	
		11111	00000000000000010

(b)

Fig. 8. (a) Schematic of the DAC, (b) Truth table of the two encoders.

16 values from 0.45 V to 1.35 V in a 1.8-V supply. To select top and bottom level of $R_{n,M}$, the two-hot encoder provides two adjacent selection signals using four MSBs, Fine[7:4]. In the second, only one output is selected among the 17 discrete values and buffered to the output. For the monotonicity of the DAC, the selection signal direction in the second stage should be changed at every switching in the first stage, and the one-hot encoder refers five LSBs, Fine[4:0]. The truth table shown in Fig. 8(b) explains the operation of the two encoder. Two resistor strings and two intermediate buffers consume only 4 μA. However, the buffer of V_{ctrl} consumes relatively large power, 25 uA, because it charges the sampling capacitor in the ADC every cycle. The DAC output V_{ctrl} has a minimum step of 3.5 mV with a 1.8-V supply voltage, which is equivalent to the capacitance of 4 fF in the coarse tuning when C_A is 1 pF.

IV. MEASUREMENT RESULTS

The proposed capacitance readout IC was fabricated in a 0.18-μm CMOS process. To verify its capacitance readout operation, a commercial electret condenser microphone (ECM) was used. Fig. 10 shows the output spectrum of the ΔΣ modulator with 1-kHz electrical signal, and Fig. 11 shows the output spectrum when the sensor receives a 4-kHz single tone sound through a typical speaker. A 60-Hz tone was found due to the measurement environment. The in-band noise power was -77 dB, which is comparable level with the target design. The test environment is shown in Fig. 9. The readout IC was originally designed for a MEMS microphone, but unfortunately the sensor was failed with some process issues. For this reason, the ECM was soldered externally, and the increased parasitic capacitor at the input node causes the degradation of sensitivity and increased power consumption.

For testing the digital offset canceller, several static capacitors in place of ECM were connected to the interface IC. Fig. 12 shows the result of the final suppressed DC level after the cancelling process. From 0.5 pF to 6 pF capacitance value, the IC suppressed DC power under about -30 dBFS, which is consistent with the digital filter resolution of 1/32.

The summarized characteristics of the interface IC are shown in Table 1. The analog blocks consume 1.7 mW,

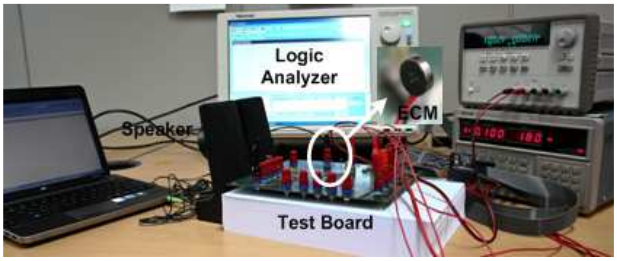


Fig. 9. Test environment.

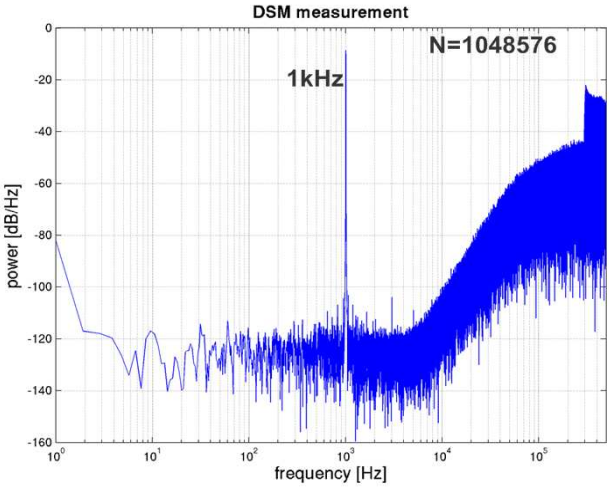


Fig. 10. Output spectrum of the ΔΣ modulator with 1-kHz signal.

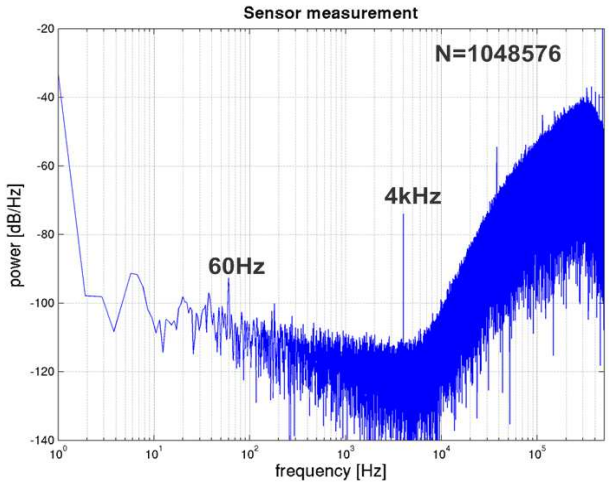


Fig. 11. Output spectrum with 4-kHz single tone sound.

and the digital filter 144 μW from a 1.8-V supply voltage. The chip photograph is shown in Fig. 13, and the chip occupied an area of 1.33×0.86 mm^2.

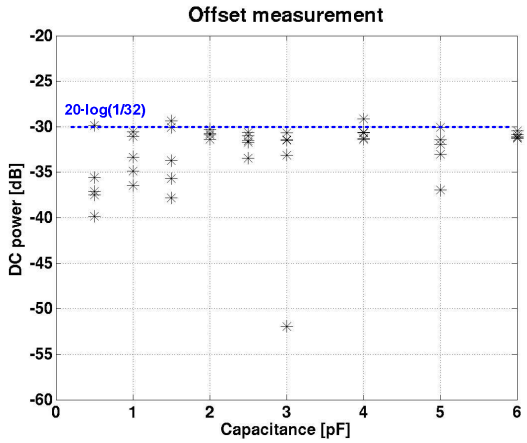


Fig. 12. Output DC levels for several capacitor samples.

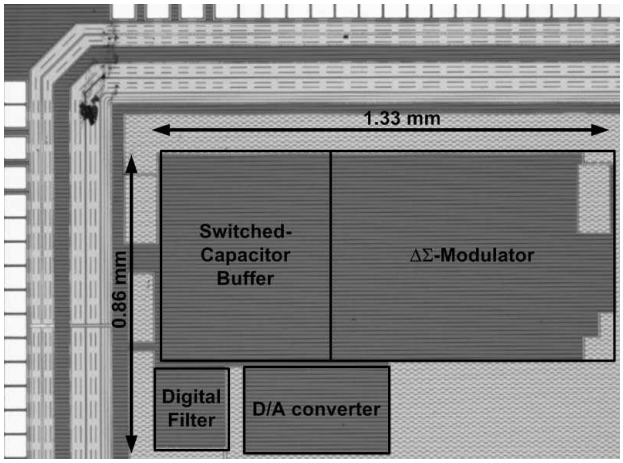


Fig. 13. Chip photograph.

Table 1. Characteristics of the interface IC

Performance Summary	
Process	*0.18-μm 1P6M CMOS*
Sampling Frequency (f_s)	*1 MHz*
Signal Bandwidth	*8 kHz*
Over-sampling Ratio	*64*
In-Band Noise Power	*-77 dB*
Detectable Range	*Nominal: 0.5 pF ~ 6 pF* *Amplitude: ±1.6 pF*
Power Dissipation	*Analog : 1.4mW (@ 1.8 V)* *Digital : 144μW (@ 1.8 V)*
Chip Size	*1.33 × 0.86 mm²*
DC Offset Canceller Resolution	*< -30 dBFS*

V. CONCLUSIONS

We propose a capacitance readout IC for capacitive sensor using a switched-capacitor C/V converter and a digital DC canceller. The digital DC canceller enables the IC to avoid large passive elements for a very low cutoff frequency. The described coarse and fine locking process achieves short start-up time, low kT/C noise, and maximized dynamic range simultaneously. The proposed switched-capacitor C/V converter minimizes device flicker noise by utilizing the CDS technique. The fabricated IC suppressed DC power to less than -30 dB for several static capacitors, and the switched-capacitor front-end successfully read out a dynamic signal from a capacitive sensor.

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