A 6-bit 3.3GS/s Current-Steering DAC with Stacked Unit Cell Structure

Si-Nai Kim, Wan Kim, Chang-Kyo Lee, and Seung-Tak Ryu

Abstract—**This paper presents a new DAC design strategy to achieve a wideband dynamic linearity by increasing the bandwidth of the output impedance. In order to reduce the dominant parasitic capacitance of the conventional matrix structure, all the cells associated with a unit current source and its control are stacked in a single column very closely (stacked unit cell structure). To further reduce the parasitic capacitance, the size of the unit current source is considerably reduced at the sacrifice of matching yield. The degraded matching of the current sources is compensated for by a self-calibration. A prototype 6-bit 3.3-GS/s current-steering full binary DAC was fabricated in a 1P9M 90 nm CMOS process. The DAC shows an SFDR of 36.4 dB at 3.3 GS/s Nyquist input signal. The active area of the DAC occupies only 0.0546 mm^2 (0.21 mm x 0.26 mm).**

Index Terms—**DAC, wideband dynamic linearity, stacked unit cell**

I. INTRODUCTION

Emerging high speed data communication systems such as 60-GHz WPAN and ultra-wideband (UWB) radios require high speed data converters with GHz-order sampling rates. One of the critical design issues with high speed DACs is how to preserve the dynamic linearity (spurious free dynamic range, SFDR) at high frequency signals while avoiding reduction of the output impedance [1, 2]. The common-centroid based two-dimensional (2-D) current source array [2, 3] is a suitable DAC architecture for good static linearity (DNL/INL). However, when it comes to the dynamic linearity, i.e. SFDR, the common-centroid based two-dimensional (2-D) current source array may not be the best choice because of the large parasitic capacitance at the output of the current source. This paper focuses on the dynamic linearity of a high speed DAC and presents a new design strategy to achieve wideband linearity from a high-speed 6-bit current-steering DAC. In order to minimize the parasitic capacitance at nodes in the output current path, this study proposes a stacked unit cell structure that minimizes the length of the interconnection wires. In addition, to further reduce the capacitance, the current source size is considerably reduced at the cost of increased mismatch. The degraded matching yield is compensated for by a self-calibration.

In the next section, design considerations for the wideband DAC are discussed. The proposed wideband DAC architecture is presented in Section III. In Section IV, the self-calibration scheme for the suggested design is explained. Measurement results are discussed in Section V, and Section VI concludes the paper.

II. DESIGN CONSIDERATIONS FOR WIDEBAND DAC

Fig. 1(a) shows a representative structure of a 2-D current-matrix-based current-steering DAC with a schematic of a 1-bit cell. The structure is good for cell matching owing to the compact current source array, often with common centroid or randomized cell placement [3-5]. However, one drawback with this

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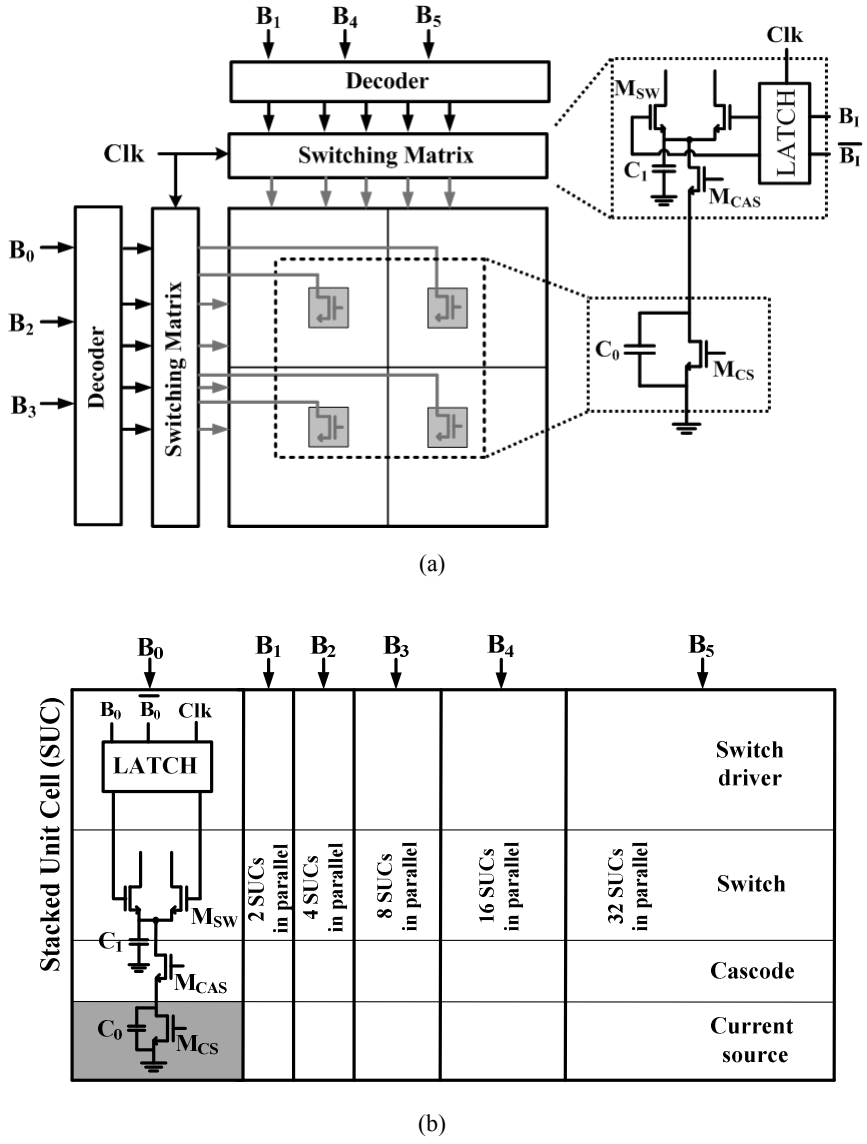

Fig. 1. (a) Structure of 2D current source array, (b) proposed DAC structure based on SUC.

structure is that the spread of current sources (M_{CS}) for better static matching requires relatively long interconnection wires, which results in large parasitic capacitance (C_0) at the output of the current sources.

C_0 reduces the output impedance as the signal frequency increases and, thus, SFDR degrades. In order to alleviate the effect of C_0 at high frequency, many designs have employed cascode current sources (M_{CAS} + M_{CS}) [2, 3] to increase both the static and dynamic output impedance. The cascode transistor (M_{CAS}) on top of the current source (M_{CS}) provides high output resistance at low frequency. One drawback with the cascode structure might be the added junction capacitance at C_0 by M_{CAS}. Even though the cascode current source comes at the expense of increased C_0, the increased output resistance at DC and small C_1 provides wider bandwidth of output impedance than does the simple current source. Fig. 2 illustrates the output impedance characteristics of the simple current source, the cascode, and the proposed design. Here, it is assumed that the switch transistors (M_{SW} in Fig. 1) work in the saturation region when they are on. In order to reduce the parasitic capacitance C_1, the sizes of M_{SW} and M_{CAS} can be minimized by considering the operational voltage conditions. Another drawback of the cascode current source that we can think of is that the insertion of M_{CAS} reduces the available V_{DS} of M_{CS}.

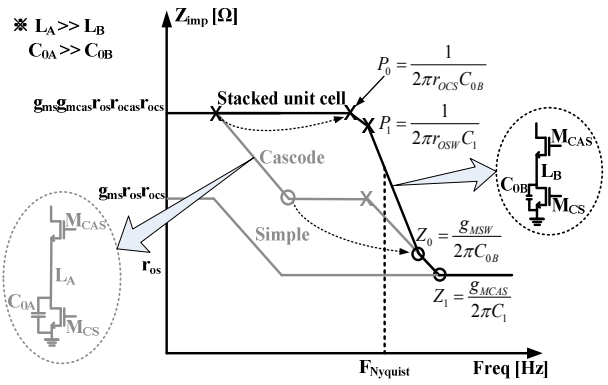

Fig. 2. Frequency response of output impedance.

Therefore, the overdrive voltage (V_{OV} = V_{Dsat} = V_{GS} − V_{TH}) of M_{CS} should be reduced with increased transistor size, which increases C_0. However, since the routing parasitic at the drain of M_{CS} is more dominant, M_{CS} does not increase C_0 substantially in the 2-D structure. A side effect of the reduced V_{OV} in M_{CS} is that the current matching characteristic degrades according to (1) [6]. This problem will be revisited in Section III with

$$WL = \left[A_\beta^{\,2} + \frac{4A_{VT}^{\,2}}{(V_{GS} - V_{TH})^2} \right] \frac{I^2}{2\sigma^2(I)} \qquad (1)$$

the proposed design.

Even though C_0 has not been a serious problem, as the sampling frequency further increases to more than several GHz, it can be difficult to secure sufficient output impedance up to the Nyquist frequency. As the graph 'Cascode' in Fig. 2 illustrates, the long routing line (L_A) at the drain node of M_{CS} makes large capacitance (C_{0A}). Thus, if the routing (L_B) wire can be shortened the value of capacitance (C_{0B}) can be reduced substantially (P_0 can be located close to P_1) and consequently the impedance bandwidth will be extended.

III. Proposed Wideband DAC Architecture

To extend the bandwidth of the output impedance, the present work focuses on reducing C_0. Reduction of C_0 is achieved in this work by two design approaches: 1) minimization of the interconnection path from the current source to the current switch, and 2) reduction of the current source size at the expense of degraded matching yield. In order to minimize C_0 from the interconnection

Table 1. Current source size reduction

	3σ INL	Vov [V]	WL [um^2]	(W/L)$_{CS}$ [um^2]	C_0 [fF]	Comparison (WL)
(a)	6-bit	0.11	3.68	8.3/0.4	10.1	1
(b)	4-bit	0.15	0.51	2.3/0.2	3.1	0.14

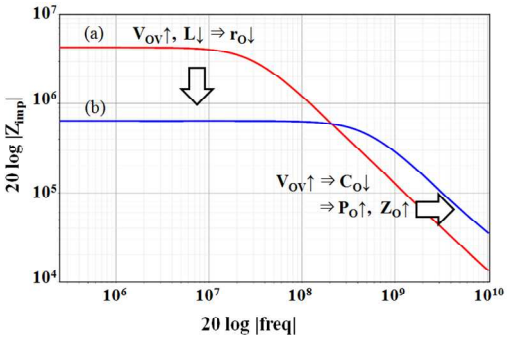

Fig. 3. Bandwidth variation according to V_{OV} and INL yield.

lines, all the elements for a unit current cell, including its control, are stacked in a single column; the structure is referred to as a Stacked Unit Cell (SUC) in this paper, as the B_0 cell in Fig. 1(b) illustrates. In order to avoid design complexity, the DAC was designed in a full binary-weighted manner. Since M_{CS}, M_{CAS}, M_{SW}, and a latch for switch driving are stacked closely, the parasitic capacitances due to the interconnection lines between them, i.e. C_0 and C_1, are minimized. To construct a binary weighted current-steering DAC, all the SUCs are placed in a single line and grouped for binary-weight generation.

This structure provides a very compact layout. In contrast to the traditional 2-D current source array, in which the contribution of the junction capacitance of M_{CS} is not significant due to the excessive interconnection parasitic capacitance, the proposed SUC structured single-line layout scheme can be dominantly affected by the junction capacitance of the transistors. This implies that the pole frequency P_0 can be pushed to a higher frequency by using a smaller transistor size. Table 1 shows how we were able to reduce C_0 in this design. Since this work targets 6-bit resolution, the required output impedance values Z_{imp} for 0.5 LSB INL and for 38 dB SFDR are 98.5 KΩ and 50 KΩ, respectively [7, 8]. Row (a) in Table 1 is the current source design result for a 6-bit DAC with 3σ yield for 0.5LSB INL. In order to further extend the bandwidth of the output impedance, the overdrive voltage of M_{CS} was increased by 40mV with reduced W/L in order to reduce the current source size (row (b) in Table 1). In addition, we guarantee only a

4-bit linearity (0.5 LSB INL with 3-sigma yield) even though the design target is 6-bit resolution. As row (b) illustrates, the 4-bit matching design with enhanced V_{ov} and the reduced transistor size reduces the parasitic capacitance by about 1/3 while at which bandwidth of the output impedance (frequency where Z_{imp}=50 KΩ) is extended 2.5-fold (up to 6 GHz) compared with that of the 6-bit yield design shown in (a).

While the proposed design extends the bandwidth of the output impedance, the DC resistance is degraded due to the reduced output resistance (r_o) of the current source, as delineated in (2). However, the output resistance of the unit current source is set at 650 KΩ, guaranteeing the required static linearity.

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}V_{OV}^2,\ \lambda \propto \frac{1}{L} \Rightarrow r_O \propto \frac{L^2}{W * V_{OV}^2} \qquad (2)$$

In order to minimize glitches during the transition period, the latch introduced in [2] was used. The latch synchronizes the control signals in front of the switch transistors. In addition, by raising the crossing point of the differential input signals, the NMOS switches are not turned off simultaneously and the voltage fluctuation at the source coupled node is mitigated. In order to obtain high frequency input data and clock signal, a typical differential receiver was used [1].

IV. Self-Calibration for Current Mismatch

The degraded matching between the current sources due to the reduced yield design for wideband dynamic linearity in the single line SUC array is compensated for by a self-calibration. Since only a 4-bit linearity is guaranteed by the designed transistor size, current sources for the fifth and sixth bits (B_4 and B_5) are calibrated. Fig. 4(a) and (b) illustrate the operational principle of the current source calibration with simple block diagrams, which is a quite popular method [9]. In order to calibrate the B_4 segment (Fig. 4(a)), the currents from the lower bits (B_3 ~ B_0) and the dummy current whose amount is the same as that of B_0 are added together and then the added current is compared with the current from the B_4 segment. Until the polarity of the comparator changes, the input code of CAL-DAC is

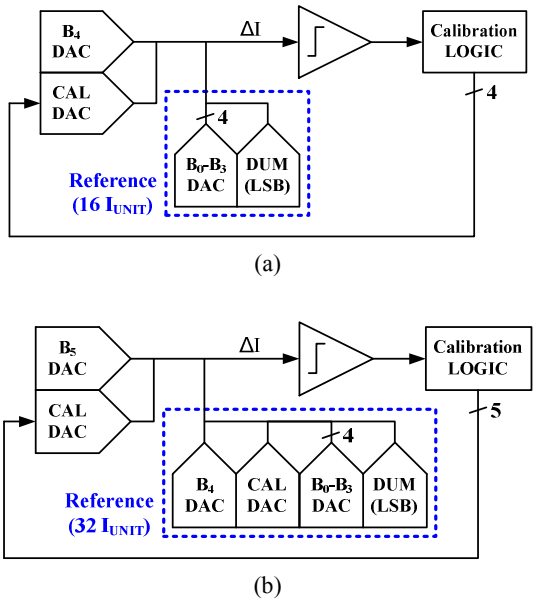

Fig. 4. Block diagram of the self-calibration (a) B_4 DAC (b) B_5 DAC.

controlled. A detailed calibration scheme for B_4 is illustrated in Fig. 5 with a transistor-level circuit diagram.

The main current source array for B_4 (MSB-1 bit) was designed with 15 unit current sources, instead of 16, for a nominal current of 15 I_{UNIT}. The calibration DAC for the B_4 segment (Cal-DAC4) has a 4-bit resolution with LSB current of 1/8 I_{UNIT} and a full current of 2 I_{UNIT}. In its calibration period (VC=1), the total current from the termination current source (DUM with I_{UNIT}) and $B_3 \sim B_0$ segments, whose nominal value is 16 I_{UNIT}, is compared with the sum of the current from the B_4 segment and from Cal-DAC4. Cal-DAC4 increases its current until the polarity of the current comparator changes.

The calibration operation for B_5 is similar to that for B_4 except that it operates when VC=0 (VCB=1); the calibration DAC for B_5 (Cal-DAC5) has a 5-bit resolution. The B_5 segment has a nominal current of 30 I_{UNIT} instead of 32 I_{UNIT} and Cal-DAC5 has a full current of 4 I_{UNIT}. Since the current comparison is done in the foreground with a different current path, not to the output load, the comparator can incorporate large transistors for small offset. Our Monte-Carlo simulation estimated the 1-sigma offset value of the current comparator at 2.3 μA, which is sufficiently small for 6-bit DAC calibration because the 1LSB current of the main DAC is 64 μA. The PMOS load of the comparator was laid out in a common-centroid fashion for offset reduction.

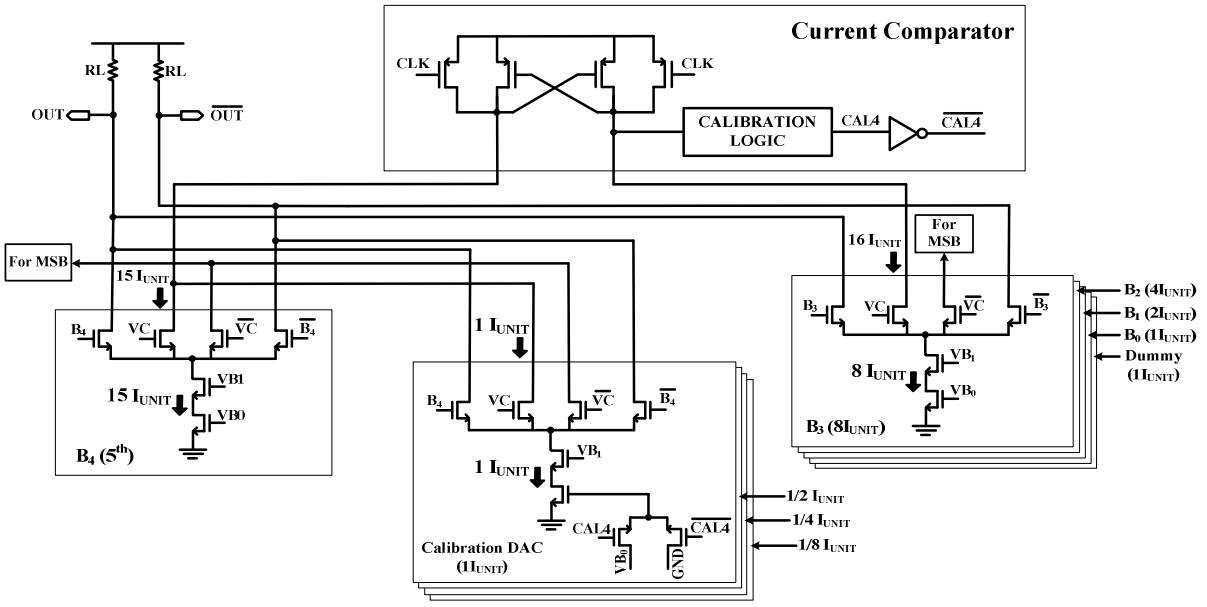

Fig. 5. Calibration scheme for MSB-1(B_4) bit segment calibration.

V. MEASUREMENT RESULTS

A prototype of the proposed 6-bit DAC was implemented in 90 nm CMOS technology. The chip photo is shown in Fig. 6. Note that the area occupied by the cascode current sources and the switches is as small as 10 μm x 260 μm owing to the single-line layout. Most of the area of SUC is occupied by the 100 μm- high latches for the switch driver. The total active area, including the loosely drawn calibration control logic, is 210 μm x 260 μm.

The measured static linearity is shown in Fig. 7. Before calibration, the peak DNL and INL are -1 LSB and -0.71 LSB, respectively. After calibration, the peak DNL and INL are reduced to -0.22 LSB and 0.25 LSB.

Dynamic performance was measured at several sampling frequencies. Fig. 8 shows the measured 46.2 dB SFDR for 51 MHz input signal frequency, at 3.3 GS/s.

The SFDR for the Nyquist input at 3.3 GS/s is 36.4 dB as shown in Fig. 9. Due to the degraded matching property of the signal path on the test board, THD performance is not so good.

The summary of the measured SFDR as a function of signal frequency at 1 GS/s, 2 GS/s, and 3.3 GS/s is presented in Fig. 10. SFDR at 3.3 GS/s (0.1 ~ 0.4 Fsig/Fclk) is degraded. In the measurement, S11 of the output network on the evaluation board showed degrading performance as the frequency increases.

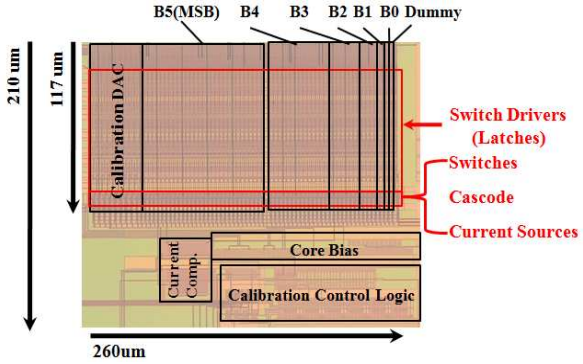

Fig. 6. Chip photo of the prototype 6-bit DAC.

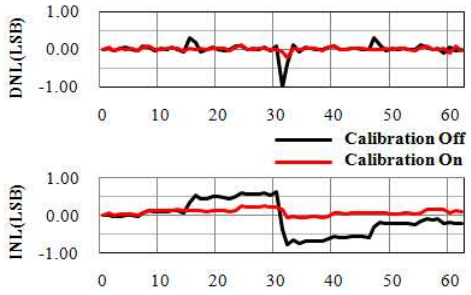

Fig. 7. Measured DNL and INL profiles.

Table 2 summarizes the measured performances of the proposed DAC. Performance comparison is shown in Table 3. Both [1] and the proposed design basically do not have the problem for the operation in 3 GS/s

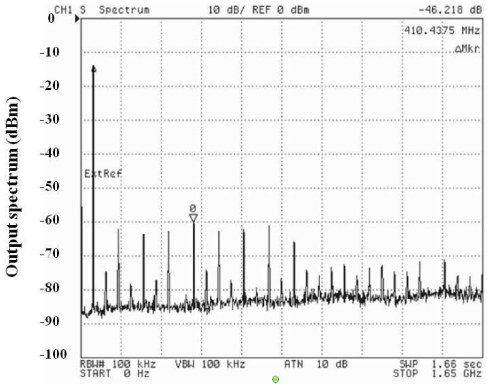

Fig. 8. Measured output spectrum for a 51 MHz input at 3.3 GS/s.

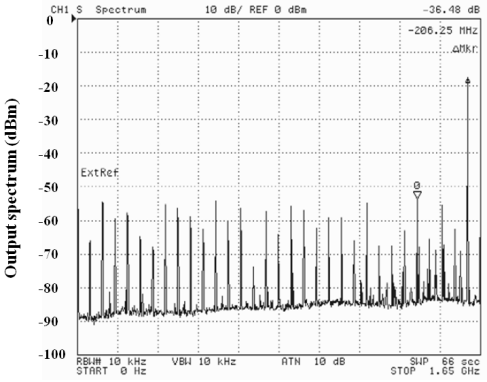

Fig. 9. Measured output spectrum for a 1.596 GHz input at 3.3 GS/s.

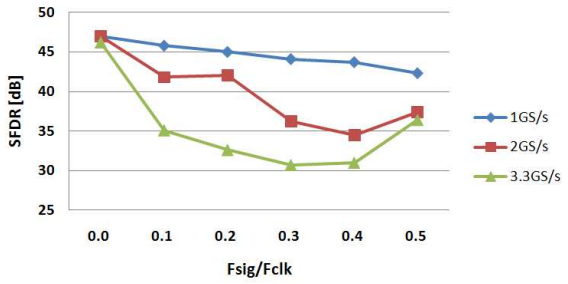

Fig. 10. Measured SFDR for 1 G, 2 G, and 3.3 GS/s.

sampling rate. However, in the simulation, the proposed DAC showed wideband output impedance up to 6 GS/s while conventional cascade design showed limited output impedance up to 3 GS/s. Thus, the proposed SUC is potentially suitable for future high-speed wideband application. Unfortunately, our design did not show such a good performance in the measurement due to impedance matching.

The proposed design occupies the smallest possible area, only 0.0546 mm^2. Due to the complicated latch design according to [2], power consumption is larger than other designs. Power consumption information of a proposed design is given in Table 4.

Table 2. Performance summary

Resolution		6-bit
Analog / Digital Supply		1.2 / 1 V
Conversion Rate		3.3 GS/s
Power Dissipation		47 mW
SFDR	16M, 484 MHz @ 1 GS/s	47 dB, 42.3 dB
	31M, 968 MHz @ 2 GS/s	47 dB, 37.4 dB
	51M, 1.59 GHz @ 3.3 GS/s	46.2 dB, 36.4 dB
DNL / INL		-0.22 / 0.25 LSB
Core Area		0.21 mm x 0.26 mm

Table 3. Performance comparison

	[1]	[10]	This work
Technology	130 nm	130 nm	90 nm
Supply Voltage	1.2 V	1.2 V	1.2 / 1 V
Resolution	6 bit	6 bit	6 bit
Conversion Rate	3 GS/s	2.7 GS/s	3.3 GS/s
Output Bandwidth	1.426 GHz	520 MHz	1.596 GHz
Segmentation	4(Una) + 2(Bin)	4(Una) + 2(Bin)	6(Bin)
Power Dissipation	29 mW	28 mW	47 mW
INL / DNL	0.02 LSB	0.1 LSB	0.25 / 0.22 LSB
SFDR	36.2 dB	37 dB	36.4 dB
Core Area	0.2 mm^2	0.76 mm^2	0.055 mm^2
Calibration	NO	NO	YES

Table 4. Dynamic power dissipation

Analog	Unit current cell and bias	4 mW
Digital	Latches (63 Core, 7 Calibration)	21 mW
	Buffer, Calibration Logic	22 mW
Total Power		47 mW

VI. CONCLUSIONS

This paper presented a design methodology for realizing a full binary DAC that provides good dynamic linearity at high frequency. The stacked unit cell structure minimizes the active area of the DAC and the parasitic capacitance of the current sources, which maintain high output impedance at high frequency. Although the prototype did not show constant performance for the entire range of output signal frequency, it exhibited dynamic performance at the Nyquist frequency superior to that of the state of the art 6-bit DAC. The design strategy can be useful for wideband DAC design for future communication applications.

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