A 15-GHz CMOS Multiphase Rotary Traveling-Wave Voltage-Controlled Oscillator

Changchun Zhang*,**, Zhigong Wang*, Yan Zhao*, and Sung Min Park**

Abstract—This paper presents a 15-GHz multiphase rotary traveling-wave voltage-controlled oscillator (RTW VCO) where a shielded coplanar stripline (CPS) is exploited to provide better shielding protection and lower phase noise at a moderate cost of characteristic impedance and power consumption. Test chips were implemented in a standard 90-nm CMOS process, demonstrating the measured results of 2-GHz frequency tuning range, -11.3-dBm output power, -109.6-dBc/Hz phase noise at 1-MHz offset, and 2-ps RMS clock jitter at 15 GHz. The chip core occupies the area of 0.2 mm^2 and dissipates 12 mW from a single 1.2-V supply.

Index Terms—CMOS, shielded coplanar stripline, phase noise, rotary traveling-wave, VCO

I. INTRODUCTION

Voltage-controlled oscillators (VCOs) are categorized into three distinct types by their physical mechanism: RC-based VCOs, LC-based VCOs, and transmission line (TL)-based (or wave-based) VCOs. Among these types, the RC-based VCOs that include relaxation VCOs and ring VCOs exhibit the most inferior phase noise characteristics because of their inevitable resistor-related thermal noises. The LC-based VCOs are less competent than the TL-based VCOs because the feasible frequency range of the lumped passive inductors is much lower than that of the transmission-lines because of their parasitic

capacitances. In other words, the inherent parasitic capacitances of the TL-based VCOs can be almost absorbed into the transmission-lines, and thus the oscillation frequency can occur at a much higher frequency than other types.

Typically, three types of TL-based VCOs exist such as standing-wave VCOs, traveling-wave VCOs, and rotary traveling-wave (RTW) VCOs [1]. The standing-wave VCOs are unable to generate multiphase clocks and the travelling-wave VCOs show inferior phase noise characteristics due to their termination resistors. Thus, the RTW VCOs provide the best performance owing to their ability to generate multiphase clock outputs and demonstrate excellent phase noise characteristics [2-5]. In addition, a multiple array of RTW VCOs can be utilized as a clocking distribution circuit [2].

This paper presents a 15-GHz RTW VCO which is realized in a standard 90-nm CMOS technology. Particularly, it employs half-quadrature topology and improved coupled coplanar waveguides so that the measured results demonstrate wider tuning range and lower power consumption with comparable phase noise than recently reported multiphase CMOS VCOs.

Section II and Section III provide the design
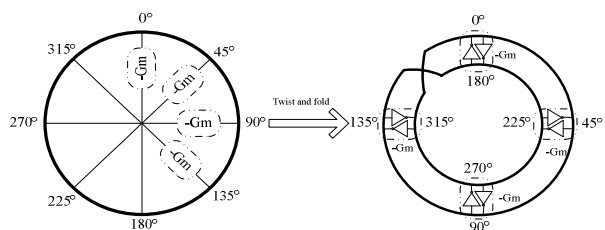
Fig. 1. RTW VCO topologies (a) untwisted single ring, (b) möbius twisted ring.

methodology and the circuit description. Section IV demonstrates the chip implementation and its measured results. Conclusion follows in Section V.

II. DESIGN METHODOLOGY

Fig. 1 shows a conventional ring RTW VCO and its transformed version which is a Möbius ring RTW VCO. This transformation provides a number of advantages, including easier placement of –Gm cells, simpler tapping-off of the required differential clocks, better matching of differential clocks, less EMI radiation, better tolerance of large EMI, smaller physical area, etc.

Fig. 2 illustrates an equivalent transforming process of a periodically loaded coupled transmission line (PLCTL), where the parameters L, R, C, and G indicate per-unit-length inductance, resistance, capacitance, and conductance, respectively. Also, 'unload', 'load', or 'PLCTL' represents unloaded CTL, load network, and PLCTL, respectively. Fig. 2(b) shows its lumped-element equivalent circuit of the PLCTL, and Fig. 2(c) depicts the odd-mode equivalent circuit by omitting the even-mode parts. Thereby, the relations of the circuit parameters between the equivalent circuit and the original one are clearly observed.

Table 1 lists the corresponding parameters and the equations related to both unloaded CTL and PLCTL, where 'o' and 'e' indicate the odd-mode and the even-mode, respectively. Also, the parameters k_L, Z, γ, α, β, υ, and l represent the inductance coupling coefficient, the characteristic impedance, the propagation constant, the attenuation constant, the phase constant, the phase velocity, and the segment length, respectively.

Unlike a TL with infinite-bandwidth, the PLCTL has passband-stopband characteristics due to its existing periodical discontinuity, indicating that a cutoff frequency exists for the desired low-pass transmission [6]. This frequency is called 'Bragg frequency', which is a notable effect on the characteristics of the PLCTL.

$$f_{\text{bragg}} = 1 \big/ \pi l \sqrt{L_{\text{PLCTL}} \cdot C_{\text{PLCTL}}} \; . \qquad (1)$$

Fig. 3(a) shows an equivalent circuit of an RTW VCO where the load components (i.e. the combination of a cross-pair, varactors, and an output buffer) are represented as a passive load network with a negative conductance in parallel. Namely, the RTW VCO can be simplified to a combination of a passive PLCTL ring and multiple active energy-compensation cells. Then, this modeling is similar to that of an LC VCO in Fig. 3(b) because the passive PLCTL functions as a tank-load of the RTW VCO, as shown in Fig. 3(c).

The start-up conditions of the closed-loop RTW VCO can be obtained as below,

$$g_m \geq \frac{2}{Z_{\text{PLCTL,O}}} \exp\left(\alpha_{\text{PLCTL,O}} \cdot l\right)$$

$$\beta_{\text{PLCTL,O}} \cdot l = \frac{n \cdot \pi}{N} \qquad (2)$$

where n is an arbitrary odd integer for the odd-mode operation of the RTW VCO [4].

Meanwhile, the fundamental oscillation frequency (f_{RTW}) of the RTW VCO is given by,

$$f_{\text{RTW}} = \frac{v_{\text{PLCTL,O}}}{2N \cdot l} = \frac{1}{2Nl\sqrt{L_{\text{PLCTL,O}} C_{\text{PLCTL,O}}}} \; . \qquad (3)$$

Then, the tuning range of the RTW VCO is given by,

$$\frac{1}{2Nl\sqrt{L_{\text{PLCTL,O}} C_{\text{PLCTL,O,max}}}} \leq f_0 \leq \frac{1}{2Nl\sqrt{L_{\text{PLCTL,O}} C_{\text{PLCTL,O,min}}}} \; . \qquad (4)$$

Also, the power dissipation of the RTW VCO is given by,

$$P_{diss} = \frac{V_{\text{DD}}^2}{Z_{\text{PLCTL,O}}^2} \cdot R_{loop} \qquad (5)$$

where R_{loop} is the loop resistance [2, 7].

The phase noise of the RTW VCO can be derived as below, as for an LC VCO in Ref. [8]:

$$L\{\Delta\omega\} = \frac{2D}{\left(\Delta\omega\right)^2 + \left(D\right)^2} \approx \underbrace{\frac{2D}{\left(\Delta\omega\right)^2}}_{\text{Noise-to-carrier ratio}} \qquad (6)$$

$$D \sim \underbrace{\left(\frac{\omega_0}{Q}\right)}_{\substack{\text{Loss}\\(\text{unloaded})}} \cdot \underbrace{\left(\frac{1}{V_0^2} \cdot \frac{k_B T}{C} \cdot \frac{Q}{Q_{loaded}}\right)}_{\substack{\text{Linewidth}\\\text{compression factor}}} = \underbrace{\frac{1}{V_0^2} \cdot \left(\frac{k_B T}{C}\right)}_{\text{Sensitivity}} \cdot \underbrace{\left(\frac{\omega_0}{Q_{loaded}}\right)}_{\substack{\text{Loss}\\(\text{loaded})}} \qquad (7)$$
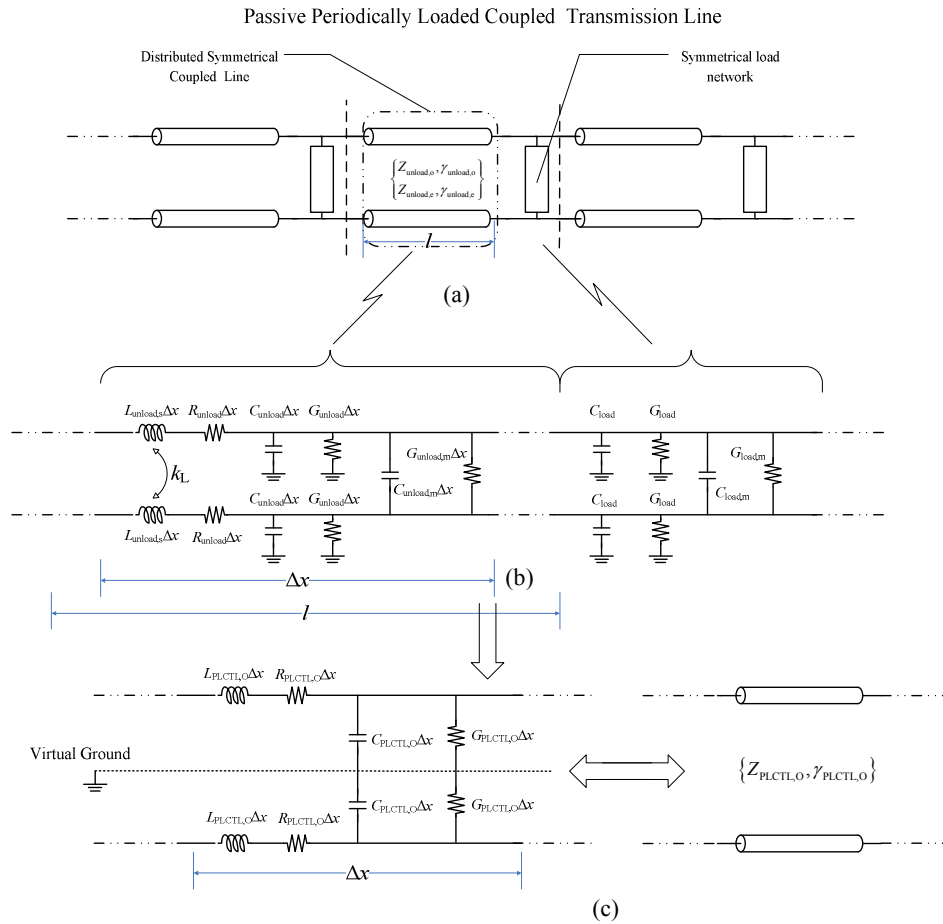
Fig. 2. (a) Segments of a passive PLCTL, (b) its lumped-element equivalent circuit, (c) its odd-mode equivalent circuit.
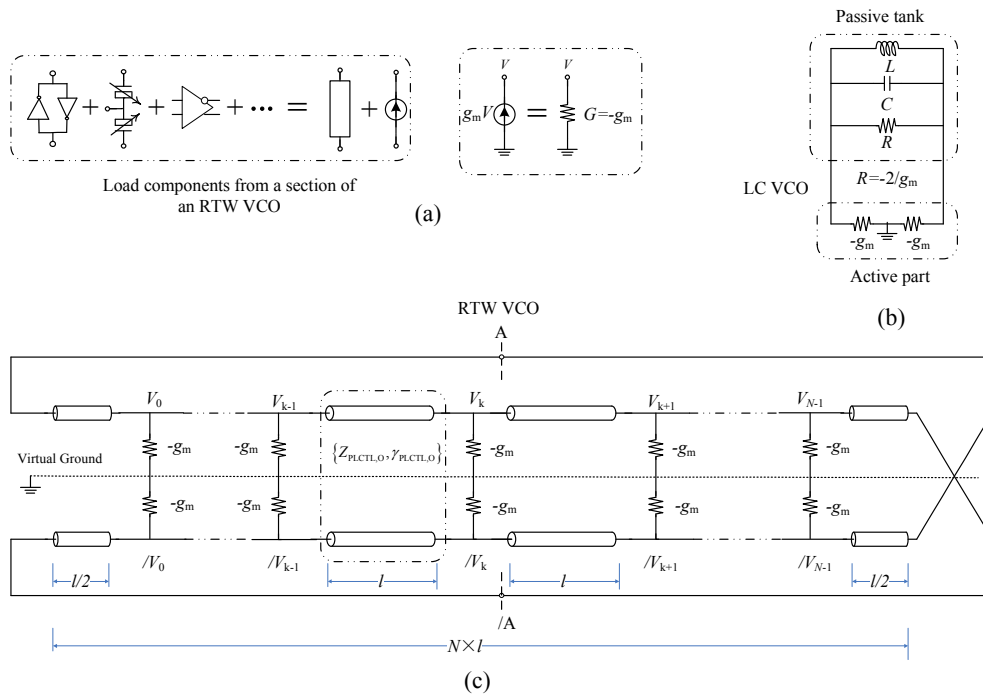

Fig. 3. Equivalent circuits of (a) load components from a section of an RTW VCO, (b) a differential LC VCO, (c) an RTW VCO.

Table 1. Parameters and equations related to unloaded CTL and PLCTL

	unloaded CTL	PLCTL	
L_o	$L_{unload,s}(1-k_L)$	$L_{unload,s}(1-k_L)$	
R_o	R_{unload}	R_{unload}	
C_o	$C_{unload}+2C_{unload,m}$	$C_{unload}+2C_{unload,m}+$ $C_{load}/l+2C_{load,m}/l$	
G_o	$G_{unload}+2G_{unload,m}$	$G_{unload}+2G_{unload,m}+$ $G_{load}/l+2G_{load,m}/l$	$\gamma=\alpha+j\beta;$
L_e	$L_{unload,s}(1+k_L)$	$L_{unload,s}(1+k_L)$	$(R\ll\omega L,$ and $G\ll\omega C)$
R_e	R_{unload}	R_{unload}	(for PLCTL, $\omega\ll 2\pi f_{bragg}$)
C_e	C_{unload}	$C_{unload}+C_{load}/l$	$Z\approx\sqrt{L/C}$
G_e	G_{unload}	$G_{unload}+G_{load}/l$	
Z	$\sqrt{(j\omega L+R)/(j\omega C+G)}$		$\gamma\approx\dfrac{1}{2}\left(\dfrac{R}{Z}+GZ\right)+j\omega\sqrt{LC}$
γ	$\sqrt{(j\omega L+R)\cdot(j\omega C+G)}$		$v\approx 1/\sqrt{LC}$
v	ω/β		$Q\approx\dfrac{\omega\sqrt{LC}}{(R/Z+GZ)}=\dfrac{1}{R/\omega L+G/\omega C}$
Q	$\beta/2\alpha$		

where D, k_B, T, Q, Q_{loaded}, V_0, ω_0, and C represent the diffusion constant, the Boltzmann constant, the absolute temperature, the unloaded quality-factor of the tank, the loaded quality-factor of the tank, the oscillation amplitude, the oscillation frequency, and the tank capacitance, respectively.

The optimization of the phase noise requires two-step procedures. The first is to select a high-Q loaded resonator tank, and the second is to achieve the highest possible line-width compression ratio which involves the loaded Q and the noise-to-carrier ratio.

Namely, an RTW VCO can achieve an excellent phase noise performance only with high loaded-Q factor in the selected transmission lines. Yet, another design tradeoff exists between power consumption and phase noise.

Due to the Bragg frequency, the Q-factor (Q_{PLCTL}) of the passive PLCTL is given by [3],

$$Q_{PLCTL}=\underbrace{\frac{1}{R_{PLCTL}/\omega L_{PLCTL}+G_{PLCTL}/\omega C_{PLCTL}}}_{\text{from resistive loss}}\cdot\underbrace{\left(1-\frac{f^2}{f_{bragg}^2}\right)}_{\text{from reflection loss}} \quad (8)$$

where Q_{PLCTL} depends not only on resistive loss, but also on reflection loss.

The resistive loss attenuates signals and gives rise to thermal noise, while the reflection loss reduces the effective signal transmission via reflection. For $f\ll f_{bragg}$, the Q_{PLCTL} becomes dependent upon resistive loss only. Then, it reduces to $1/(R_{PLCTL}/\omega L_{PLCTL}+G_{PLCTL}/\omega C_{PLCTL})$. As f approaches f_{bragg}, the reflection loss gradually becomes dominant over the resistive loss.

Hence, the loaded Q (Q_{loaded}) of an RTW VCO depends not only on the resistive loss, but also upon the reflection loss. Particularly, the latter is closely related to the interval between two neighboring discontinuities. Thereby, the shorter the interval is, the higher the Bragg frequency becomes, the better the quality factor is, and the steeper the clock waveforms become.

Meanwhile, the number (n) of the sustained harmonics of the PLCTL (correspondingly, of the RTW VCO) must meet the condition below:

$$(2n+1)f_{RTW}<f_{bragg}\Rightarrow n<\frac{1}{2}\cdot\left(\frac{f_{bragg}}{f_{RTW}}-1\right) \quad (9)$$

where the relation between n and N is given by,

$$n=\left\lfloor\frac{N}{\pi}-\frac{1}{2}\right\rfloor. \quad (10)$$

With the total gain of $N\cdot g_m$ unchanged, a larger N results in a higher Bragg frequency, which in turn leads to a higher Q-factor of the loaded CTL and steeper waveform edges. Eventually, these higher Q-factor and steeper edges improve the phase noise. However, too large N degrades the phase noise because of the serious high-frequency loss from the PLCTL and of the reduced Q-factor from the drastic increase of small-size gate resistance. Thus, a compromise must occur between the Q-factor and the number of gain stages which loads the transmission lines.

Also, (7) indicates that increasing capacitance (which is equivalent to the increase of the tank energy) results in lower phase noise at the expense of higher power dissipation, provided that the amplitude (A) is kept constant (e.g. at the border of voltage-limited region). It is because a larger capacitance corresponds to a lower characteristic impedance of the PLCTL tank, and thus leads to lower phase noise. Yet, the characteristic impedance should not be too much lowered since the condition below must be satisfied [2]:

$$Z_{\text{PLCTL}} > \frac{R_{loop}}{2}. \tag{11}$$

III. CIRCUIT DESCRIPTION

Fig. 4 depicts the three-dimensional layout of the proposed RTW VCO, which consists of the proposed shielded coplanar stripline, eight –Gm cells (which comprises inverter cross-pairs and varactors), and four output buffers. In particular, the oscillation tank comprises the shielded CPS, varactors, and the parasitic capacitances from inverters and output buffers.

1. Proposed Shielded Coplanar Stripline

Typically, there are four types of symmetric coupled lines: (a) coplanar stripline (CPS) [3, 4], (b) coupled microstrip line [9], (c) coupled coplanar waveguide (CCPW), and (d) folded coupled coplanar waveguide (FC_CPW) in which an U-shaped return ground is employed [10]. Even in a symmetric coupled line, electromagnetic interference (EMI) effect would become very serious both at high oscillation frequencies and with full swing square waveforms (which are commonly occurred at RTW VCOs). Therefore, a design tradeoff exists between shielding and characteristic impedance (Z_o). However, the former is related to both EMI and substrate loss, and the latter is closely related to power consumption in (5). Thus, better shielding indicates larger capacitance and smaller inductance, which will induce lower Z_o and hence higher power consumption. Yet, this lower Z_o benefits the phase noise of the RTW VCO, as described in Section II. Among the fore-mentioned four CTLs, the CPS yields the highest Z_o and the poorest shielding, whereas the FC_CPW provides the
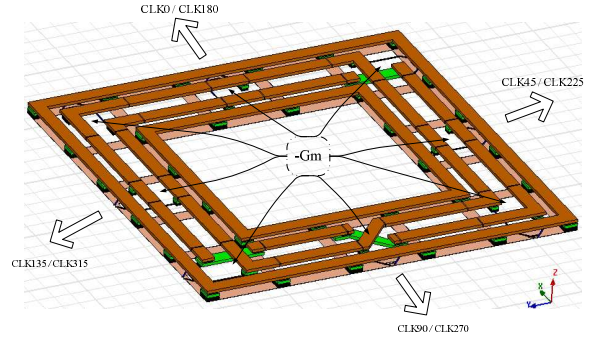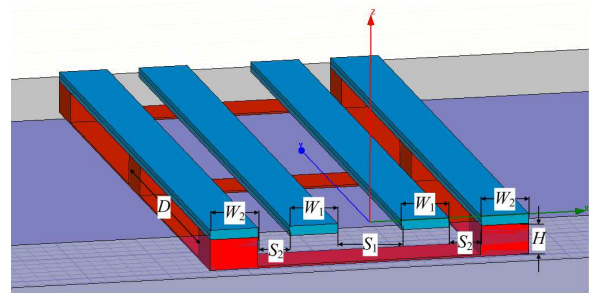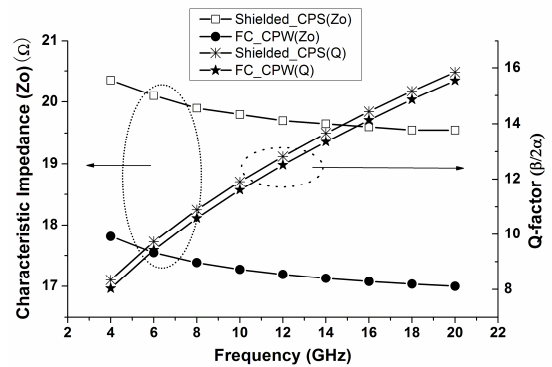

Fig. 4. Three-dimensional layout of the RTW VCO topology.

Fig. 5. (a) Three-dimensional layouts of the shielded CPS, (b) their comparison to FC_CPW in terms of odd-mode characteristic impedance and Q-factor.

lowest Z_o and the most excellent shielding.

Fig. 5(a) illustrates the proposed shielded CPS which is an optimized version between a CPS (or CCPW) and a FC_CPW. The performance of the shielded CPS can be easily controlled by either altering the ground grid density or varying the distance between the shielding ground and signal stripes. Fig. 5(b) depicts the simulation results of both the shielded CPS and the FC_CPW for the odd-mode Z_o and the Q-factor, in which the shielded CPS possesses a higher Z_O with a slightly better Q-factor as the representative FC_CPW. Also, the Q-factor of the

shielded CPS increases as the operation frequency, which is easily predicted from the definition of $Q \approx 1/(R/\omega L + G/\omega C)$ in Table 1.

Yet, as either the distance (S_1) between two signal strips or the distance (S_2) between signal strip and ground becomes larger, the odd-mode inductance increases, the capacitance reduces, and the proximity effect weakens. Therefore, both the odd-mode Z_o and the Q-factor increase at the cost of three factors: (a) EMI becomes more severe for a larger S_1 or S_2, (b) the matching between differential signals worsens, and (c) the chip area becomes larger. If the width (W) of the signal strip is wide enough, the odd-mode Q-factor increases and the odd-mode Z_o decreases.

2. Varactors

Frequency tuning is conducted by varying either the ring-length, or the effective dielectric constant, or the effective capacitance [21], among which the effective capacitance tuning with varactors is most popular due to its easiness and compactness. Particularly, accumulation-mode NMOS varactors provide excellent performance [22].

It is seen from (4) that the tuning range (Δf_o) of an RTW VCO is proportional to the ratio of $C_{tank,O,max}/C_{tank,O,min}$. Here, $C_{tank,O}$ is the sum of the equivalent odd-mode unit-length capacitance from the distributed tank, i.e. $C_{tank,O} = C_{CPS,O} + (C_{-Gm,O} + C_{buf,O} + C_{var,O})/l$. $C_{CPS,O}$ is the equivalent unit-length capacitance from the shielded CPS, and $C_{-Gm,O}/l$, $C_{buf,O}/l$, & $C_{var,O}/l$ represent the unit-length capacitance from -Gm cells, output buffers, and varactors, respectively. Therefore, $C_{var,O}$ should be much larger than other three capacitances for a wide tuning range.

Now, the Q-factor (Q_{tank}) of the distributed tank in the RTW VCO is given by,

$$Q_{tank} = Q \cdot \left(1 - \frac{f^2}{f_{bragg}^2} \right) \qquad (12)$$

$$\frac{1}{Q} = \frac{1}{Q_L} + \frac{1}{Q_C} \qquad (13)$$

$$\frac{1}{Q_C} = \sum_i \frac{1}{Q_i \cdot \left(\dfrac{C}{C_i} \right)} \qquad (14)$$

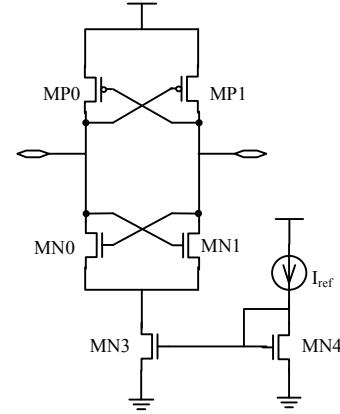where Q_L is the Q-factor of the unit-length equivalent

Fig. 6. Schematic diagram of a gain cell.

inductance of the distributed tank, C & Q_C are the total unit-length equivalent capacitance and the Q-factor of the tank, respectively. Also, C_i & Q_i represent $C_{CPS,O}$, $C_{-Gm,O}/l$, $C_{buf,O}/l$, or $C_{var,O}/l$, and their respective Q-factor.

Since the capacitance of the shielded CPS is equivalent to an MIM capacitance, its Q-factor is much higher than that of other capacitances. Also, $C_{-Gm,O}/l$ and $C_{buf,O}/l$ show higher Q-factor than $C_{var,O}/l$. Thus, Q_C in (14) is mainly determined by Q_{var} due to its lower Q-factor and bigger capacitance. Besides, Q_L is much higher than Q_{var} and then the tank Q-factor (Q_{tank}) is dominated by Q_{var}.

In this work, the minimum Q-factor of the varactors is only 6 at 15 GHz while the Q-factor of the proposed shielded CPS reaches 14.

3. Gain Cell and Output Buffers

Fig. 6 presents the schematic diagram of a gain stage, where the complementary configuration yields a higher transconductance, more symmetric oscillation waveforms, and more compact layout [14]. Here, the wave rotation uncertainty may occur and thus the direction control transistors with minimum size are added [5]. Fig. 7 illustrates the proposed -G_m cell which consists of a pair of cross-coupled CMOS inverters and a couple of varactors. The CMOS cross-coupled pair takes the same configuration as the gain stage in Fig. 6, except for the removed tail current source. Removing the tail current source provides a number of advantages [15-20]: (a) it eliminates the voltage overhead, thus maximizing the signal swing and improving the phase noise, (b) the gate-widths can be reduced because the transistors can be
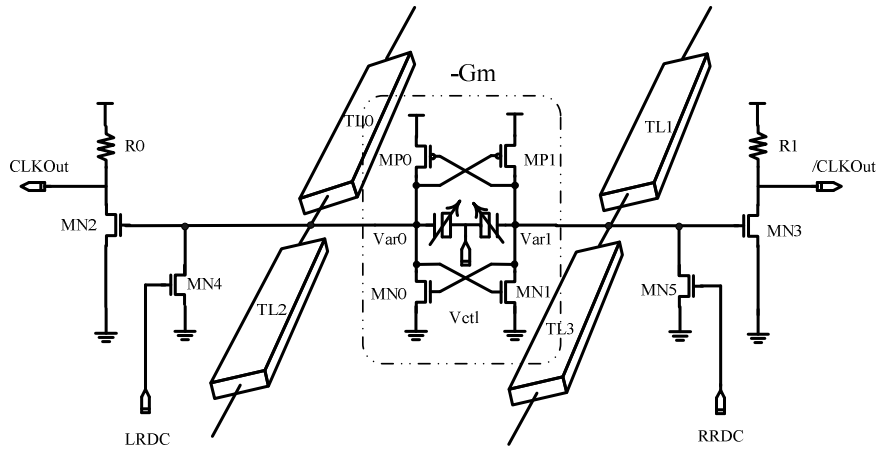
Fig. 7. -G_m cell with varactors, clock buffers, and direction control transistors.

biased at higher transconductance, and thus its nonlinear parasitic capacitances decrease accordingly. Typically, these parasitic capacitances are closely related with the tuning range and the noise conversion from both CM (common-mode) noise and AM-noise to phase noise. Besides, these parasitic capacitances degenerate the Q-factor of tank-load. (c) tail current-source is a notorious thermal noise and flicker noise source, and thus its removal improves the phase noise performance. Yet, frequency pushing problem occurs with no tail current-source.

Meanwhile, resistor-loaded common-source output buffers are employed in this work for the sake of integration-level even at the cost of larger phase noise from the loaded resistors. The resistance value is judiciously chosen to be 100-Ω in order to optimize the design tradeoff between gain and reflection.

IV. MEASUREMENT RESULTS

The proposed RTW VCO has been fabricated in a standard 90-nm CMOS technology. Fig. 8 depicts the chip microphotograph, where the core occupies the area of 450 μm × 450 μm. DC measurements reveal that the power consumption is 12 mW in total from a single 1.2-V supply.

For RF measurements, on-wafer probing has been conducted by utilizing an RF probe-station with a wide-bandwidth oscilloscope (Agilent 86100A Infinium DCA) and an E4440a digital spectrum analyzer.

Fig. 9 demonstrates the measured oscillation frequency and output power versus tuning voltage of the RTW VCO,
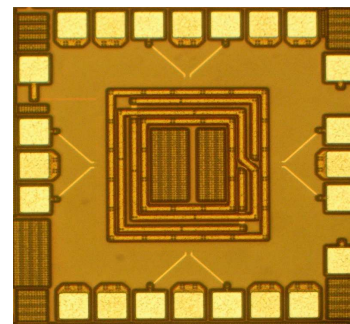

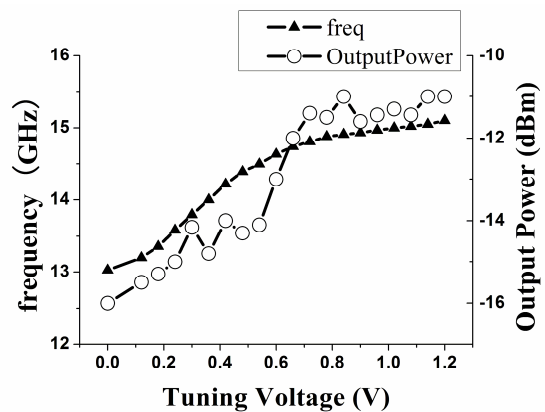**Fig. 8.** Chip microphotograph of the proposed RTW VCO.

Fig. 9. Measured oscillation frequency and output power versus tuning voltage of the proposed RTW VCO.

achieving the tuning range of 2 GHz and the corresponding VCO gain of 1.7 GHz/V on average.

Fig. 10 shows the measured waveforms of the two adjacent 15-GHz clocks with 45° phase offset, where each clock waveform has an RMS jitter of 2 ps and the amplitude of 167 mV$_{pp}$. These results confirm the measurements of the frequency domain.
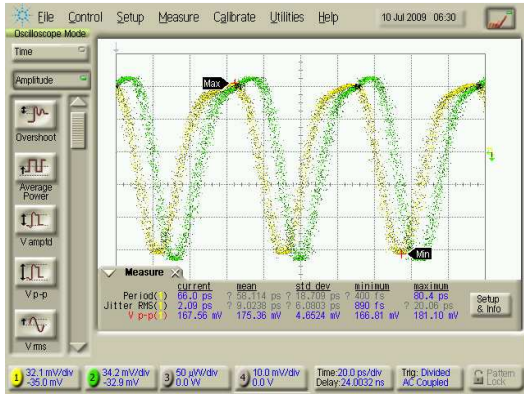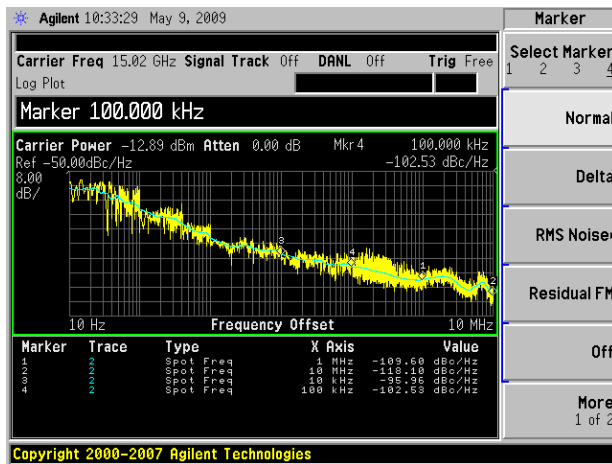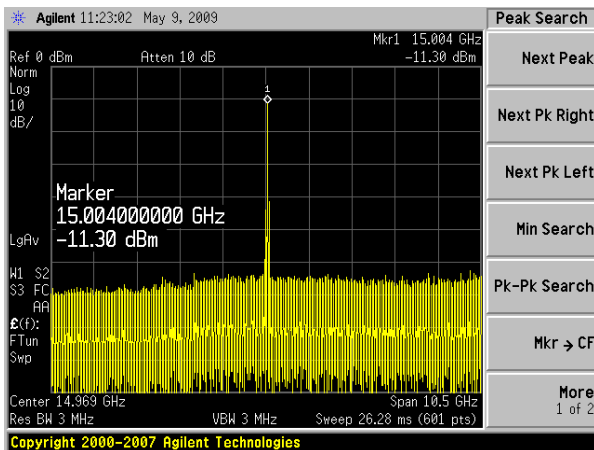
Fig. 10. Measured waveforms of the two adjacent clocks with 45° phase offset.

(a)

(b)

Fig. 11. (a) Measured phase noise of the RTW VCO, (b) the power spectrum of the generated 15-GHz clock.

Fig. 11 shows the measured phase noise and the power spectrum of the RTW VCO at the center frequency of 15 GHz, where the generated 15-GHz clock achieves the power spectrum of -11.3 dBm, and the phase noise of -95.96 dBc/Hz at 10-kHz offset, -102.5 dBc/Hz at 100-kHz offset, and -109.6 dBc/Hz at 1-MHz offset, respectively.

Table 2 summarizes the performance of the proposed RTW VCO along with the comparison with the prior arts, in which the performance is first evaluated by utilizing a typical figure-of-merit (*FoM*) defined by,

$$FOM = L\left(\Delta f_{offset}\right) - 20\log\left(\frac{f_0}{\Delta f_{offset}}\right) + 10\log\left(P\right) \quad (15)$$

where $L(\Delta f_{offset})$, f_0, and P represent the measured phase noise at the offset frequency Δf_{offset}, the oscillation frequency, and the power consumption (mW), respectively.

In addition, another figure-of-merit (*FoM_T*) is proposed as below, because frequency tuning range is a crucial performance criterion in the performance evaluation.

$$FOM_T = L\left(\Delta f_{offset}\right) - 20\log\left(\left(\frac{f_0}{\Delta f_{offset}}\right) \cdot \left(\frac{FTR}{10}\right)\right) + 10\log\left(P\right)$$

$$(16)$$

where *FTR* is the percentage of frequency tuning range.

It is clearly seen in both FoM and FoM_T that the proposed RTW VCO demonstrates superior performance among the recently published multiphase CMOS VCOs.

V. CONCLUSIONS

A 15-GHz multiphase RTW VCO is realized in a standard 90-nm CMOS process with the core area of 450 µm × 450 µm. Measured results demonstrate the frequency tuning range of 2 GHz, the output power of -11.3 dBm, and the phase noise of -109.6 dBc/Hz at 1-MHz offset. Also, the clock waveforms show the RMS jitter of 2 ps with the amplitude of 167 mV_pp. DC measurements reveal the power dissipation of 12 mW from a single 1.2-V supply. Conclusively, the proposed RTW VCO provides a low-power low-cost solution for the applications of high-speed digital interface and RF systems, such as clock and data recovery circuits and integrated phase arrays.

Table 2. Performance summary of the RTW VCO and comparison with the prior arts of multiphase CMOS VCOs

Parameters	[23]	[12]	[11]	[5]	[9]	[4]	[24]	**This work**
CMOS tech.	0.18 μm	0.18 μm	0.13 μm	90 nm	0.13 μm	0.18 μm	90 nm	**90 nm**
Frequency	5G Hz	10 GHz	11 GHz	11 GHz	12 GHz	15 GHz	18 GHz	**15 GHz**
Configuration	Revised coupled VCO	Revised RTW VCO	Revised LC-tuned ring VCO	RTW VCO	RTW VCO	RTW VCO	VCO array	**RTW VCO**
No. of phases	Half- Quad	Half- Quad	Half- Quad	24- Phase	Quad.	Half- Quad	Half- Quad.	**Half-Quad.**
Tuning range	400 MHz (7.5%)	1GHz (10%)	2.7GHz (23%)	1GHz (9%)	1.2GHz (10%)*	250 MHz (1.7%)	N/A	**2GHz (14%)**
Phase noise (dBc/Hz@1MHz)	-115.4	-105	-107	-96.65	-105	-112.2	-97.52	**-109.6**
Power diss. (mW)	7.4	N/A	26	70	30	52	9.6	**12 (10mA)**
FoM (dBc)	-181	N/A	-174	-159	-172	-179	-173	**-182**
FoM$_T$ (dBc)	-179	N/A	-182	-158	-172*	-164	N/A	**-185**

*switch array technique adopted

ACKNOWLEDGMENTS

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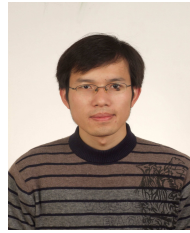
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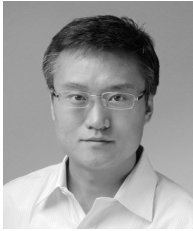
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