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Leg-Balancing Control of the DC-link Voltage for Modular Multilevel Converters

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Abstract

This paper applies carrier phase shifted pulse-width modulation (CPS-PWM) to transformerless modular multilevel converters (MMC) to improve the output spectrum. Because the MMC topology is characterized by the double-star connection of six legs consisting of cascaded modular chopper cells with floating capacitors, the balance control of the DC-link capacitor voltage is essential for safe operation. This paper presents a leg-balancing control strategy to achieve DC-link voltage balance under all operating conditions. This strategy based on circulating current decoupling control focused on DC-link balancing between the upper and lower legs in each phase pair by considering the six legs as three independent phase-pairs. Experiments are implemented on a 100-V 3-kVA downscaled prototype. The experimental results show that the proposed leg-balancing control is both effective and practical.

Key words: DC-link voltage control, MMC

I. INTRODUCTION

Since the concept of a modular multilevel converter (MMC) was firstly suggested for medium-voltage high-power application [1] [2], MMC has gained a great deal of attention from researchers and engineers due to its characteristics of natural modularity and several degrees of freedom for control [3]. These characteristics bring the advantages of high reliability, a high-quality output spectrum, a low switching frequency and low power loss for medium-or high–voltage MMC systems. Therefore, the MMC topology has been widely accepted in the application of high voltage dc transmission (HVDC), medium-voltage motor drive systems and static synchronous compensator (STATCOM) systems [4]-[8].

However, the MMC topology suffers from the issue of an imbalance dc-link voltage of the floating capacitors [6]. In order to solve this problem, several approaches have been introduced and published in the literature [9]-[17]. One approach is the so-called sorting voltage of capacitors method, which decides the charging or discharging of each chopper cell based on the current direction and the dc-link voltage value [9], [10]. Sorting capacitor voltage can effectively balance the individual dc voltage of a chopper cell, but the DC voltage balance between the upper and lower legs in each phase pair is not clear. Another method uses the negative-sequence current for leg balance control. This is accomplished at the cost of losing the capability for compensating an unbalanced load [11]. Another control strategy is adopting the circulating current for capacitor voltage control [12]-[14]. In [12], phase balancing control is achieved by adjusting the dc component in the circulating current, while the leg balancing control in one phase pair is realized by superimposing an AC command voltage on the original voltage command of the corresponding phase pair. This superimposed AC command voltage results in an AC component in circulating current. As the AC components from the different phase pairs may not be canceled out all the time, the remaining part must flow through a fourth branch to meet the KCL law. This is not available for the three-phase three-pair MMC structure which has no DC supply connected to a common DC bus. Similarly, the control strategy in [13], [14] have the same problem. A new approach for the "estimation of stored energy" for the leg-balancing control is presented in [15], [16]. Stored energy is estimated by a combination of the converter electromotive force reference, the measured alternating output current, and the known direct voltage. The total DC voltage of each leg is calculated based on the energy estimation. This method saves DC-link voltage

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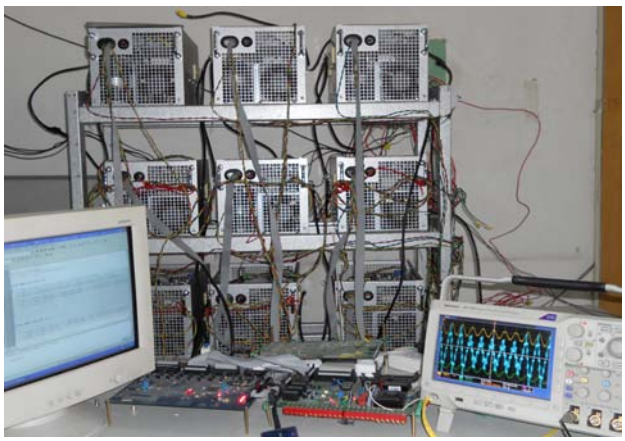
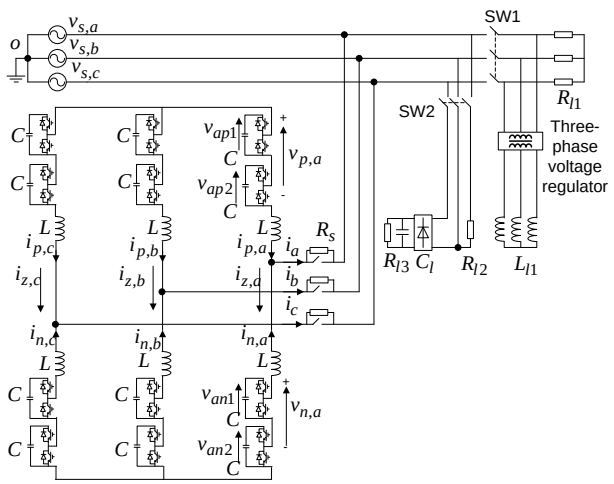


(a) Experimental hardware view.



(b) Configuration of experimental system.

Fig. 1. 100-V 3-kVA downscaled STATCOM system.

sensors and close-loop controllers, resulting in a high reliability and a reduction in the complication of the control. However, this method relies on accurate circuit parameters. As time goes by, the capacitance of the DC capacitor may changes. As a result, the performance of this control method may be affected. In addition, individual voltage control is not sufficiently discussed.

In this paper, a new method for decoupling circulating current is proposed to equalize the DC-link voltage of each leg. This method together with the overall voltage control, the phase balancing control and the individual voltage control, provides a general scheme of the capacitor voltage control for the application of HVDCs, motor drive systems and STATCOM systems. The control scheme can successfully stabilize all of the capacitor voltage under all load conditions even in unbalanced power supply systems. The related experiments are implemented on a downscaled MMC system rated at 100-V 3-kVA.

TABLE I

CIRCUIT PARAMETERS IN FIG 1

Nominal line-to-line rms voltage		100V
Power rating	P	3kVA
AC inductor	L	3.5mH
Starting resistor	R_s	51 Ω
DC capacitor voltage		90V
DC capacitor in chopper cell	C	4700 μ F
PWM carrier frequency		2.5kHz
AC load	R_{l1}	40 Ω
AC load	R_{l2}	10 Ω
DC load	R_{l3}	20 Ω
DC capacitor in diode rectifier	C_l	2200mF
AC inductive load	L_{l1}	3mH

II. CIRCUIT CONFIGURATION OF THE EXPERIMENTAL SYSTEM

Fig. 1 shows the circuit configuration of the experimental prototype. Table I summarizes the electrical specifications and the circuit parameters. This prototype is designed as a downscaled model of a medium-voltage MMC system to verify the control effect of the floating DC-links and the performance of the whole system. A cascaded number of N=2 is assigned to each leg because of the limitations of authors' lab. Here, a leg means a cluster of series-connected chopper cells with equal voltage and power ratings. An electrolytic capacitor with a capacitance of 4700 μ F is equipped for each chopper cell. No auxiliary circuits are connected to either the split DC-link of the chopper cells or the common DC bus except for the 12 DC voltage sensors. An AC inductor is also required for each leg to support the difference between the sinusoidal source voltage and the PWM converter voltage, as well as to filter the current ripple flowing through each leg. Although many modulation strategies have been published in the literature [9] [17] [18], this paper uses the carrier phase shifted pulse-width modulation (CPS-PWM) because the cascaded number is as low as N=2 for the prototype.

The combining of the switching, sw1 and sw2, realizes a balanced adjustable reactive load (RL) and an unbalanced nonlinear load (UNL).

This prototype is controlled by a fully digital control system based on a digital signal processor (TMS320F28335) and a filed programmable gate array (FPGA). Most of the mathematic calculations are implemented on DSP chip while all of the gating signals are modulated and generated by the FPGA chip. In the experiment, the carrier frequency is assigned as 2.5 kHz, so that an equivalent switching frequency of 10 kHz is achieved to match the sampling frequency.

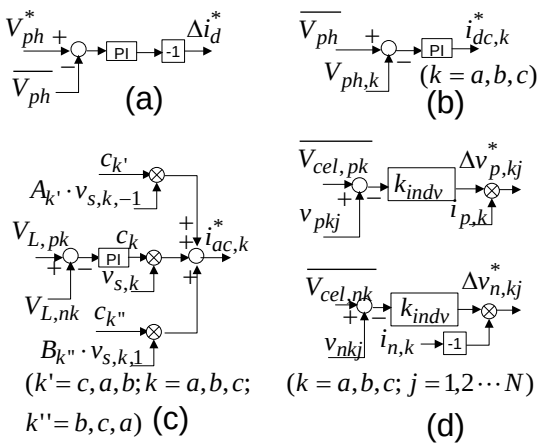
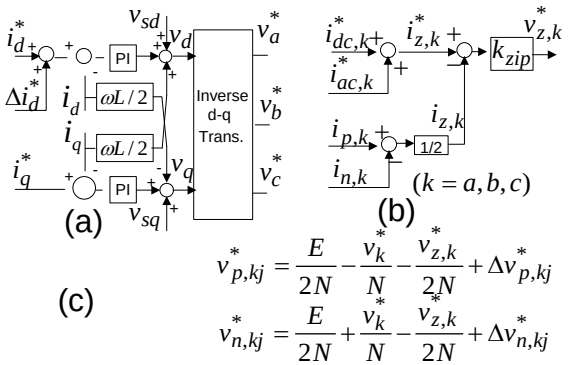


Fig. 2. Block diagram of DC capacitor voltage control. (a) Overall control. (b) phase balancing control. (c) leg balancing control. (d) individual voltage control.



$$v^*_{p,kj} = \frac{E}{2N} - \frac{v^*_k}{N} - \frac{v^*_{z,k}}{2N} + \Delta v^*_{p,kj}$$

$$v^*_{n,kj} = \frac{E}{2N} + \frac{v^*_k}{N} - \frac{v^*_{z,k}}{2N} + \Delta v^*_{n,kj}$$

Fig. 3. Block diagram of inner current-loop control. (a) Output current control. (b) circulating current control. (c) individual modulated voltage.

III. CONTROL STRATEGY

Since the circuit fundamental and operating principle are described in paper [6], this paper just pays attention to the control strategy. The whole control algorithm can be divided into two groups of control, the DC capacitor voltage control and the inner current-loop control. Fig. 2 shows a control block diagram of the 12-floating DC capacitor control which is composed of four layers, namely, the overall voltage control, the phase balancing control, the leg balancing control and the individual voltage control. Fig. 3 demonstrates a block diagram of the inner current-loop control, the output current control and the circulating current control.

A. Overall Voltage Control

Fig. 2 (a) shows a block diagram of the overall voltage control. The aim is to maintain the three-phase average DC voltage at a given value. A proportional and integral (PI) regulator with two constant parameters, k_{vp} and k_{vi}, is introduced for overall voltage control. The output of the PI regulator is the active current in the d axis for overall capacitor voltage maintaining. The three-phase average DC voltage and the active current command are given by:

$$\overline{V_{ph}} = \frac{1}{3}\sum_{k=a,b,c}\sum_{j=1}^{N}(v_{kpj} + v_{knj}) \quad (1)$$

$$\Delta i^*_d = -k_{vp}(V^*_{ph} - \overline{V_{ph}}) - k_{vi}\int(V^*_{ph} - \overline{V_{ph}})dt] \quad (2)$$

where, v_{kpj} and v_{knj} represent the DC-link voltage of k-phase j-th module in upper and lower legs, respectively.

B. Phase Balancing Control

Fig. 2 (b) shows a block diagram of the phase balancing control. This layer of the control forces the DC voltage of each phase to be equalized. The two constant parameters, $k_{p,dc}$ and $k_{i,dc}$, form a PI regulator for each phase. The output of the PI regulator is considered as the command of the DC circulating current. In Fig. 2(b), $\overline{V_{ph}}$ can be found in equation (1) and $V_{ph,k}$ is the total capacitor voltage in the k-phase converter. The command of the DC circulating current and the k-phase total capacitor voltage are expressed by:

$$i^*_{dc,k} = k_{p,dc}(\overline{V_{ph}} - V_{ph,k}) + k_{i,dc}\int(\overline{V_{ph}} - V_{ph,k})dt \quad (3)$$

$$V_{ph,k} = \sum_{j=1}^{N}(v_{pkj} + v_{nkj}) \quad (4)$$

C. Leg Balancing Control

Fig. 2(c) shows a block diagram of the leg balancing control. This layer of the control uses the fundamental AC circulating current for equalizing the DC capacitor voltages between the upper and lower legs in each phase pair. When the active AC circulating current in one phase pair flows to the other two phase pairs, it splits in two reactive currents to avoid influencing the DC voltages of the other two phases. Therefore, the circulating current in each phase pair contains three parts: one active current for the leg balancing and two reactive currents resulting from the active currents in the other two phase pairs.

In order to estimating the amount of active current for the leg balancing control, one PI regulator with constant parameters of $k_{p,ac}$ and $k_{i,ac}$ is introduced for each phase pair. The outputs of three PI regulators are marked as c_k, $c_{k'}$ and $c_{k''}$. In Fig. 2(c), the terms of $A_{k'} \cdot v_{s,k,-1}$ and $B_{k''} \cdot v_{s,k,1}$ are the reactive current references. The details are discussed in the next section. Finally, the command AC circulating current can be obtained by:

$$c_k = k_{p,ac} \cdot (v_{L,pk} - v_{L,nk}) + k_{i,ac} \cdot \int(v_{L,pk} - v_{L,nk})dt \quad (5)$$

$$i^*_{ac,k} = c_{k'} \cdot v_{s,k,-1} + c_k \cdot v_{sk} + c_{k''} \cdot v_{s,k,1} \quad (6)$$

D. Individual Voltage Control

Fig. 2 (d) shows a block diagram of the individual voltage control. Redistribution of the active power among the chopper cells in each leg can be achieved by trimming the output voltage of each module along the direction of the leg current. One proportional regulator k_{indv} is introduced for each module. The trimming command for the cells in the upper and lower legs can be expressed as:

$$\Delta v^*_{p,kj} = k_{indv} \cdot (\overline{V_{cel,pk}} - V_{cp,kj}) \cdot i_{p,k} \quad (7)$$

$$\Delta v^*_{n,kj} = k_{indv} \cdot (\overline{V_{cel,nk}} - V_{cn,kj}) \cdot (-i_{n,k}) \quad (8)$$

E. Inner Current-loop Control

Fig. 3(a) shows a block diagram of the output current control, which is based on a d-q transformation. Two PI regulators with constant parameters of k_{ip} and k_{ii} are adopted for the d-and q-axis controls. The command current of i^*_d and i^*_q are derived according to the instantaneous power theory [19]. The term of Δi^*_d is given by the overall voltage control. Finally, the three-phase line-to-neutral voltage commands of v^*_a, v^*_b and v^*_c are obtained by applying a reverse d-q transformation.

Fig. 3(b) shows a block diagram of the circulating current control. A proportional regulator k_{zip} is introduced for its implementation. The command circulating current $i^*_{z,k}$ includes a dc component $i^*_{dc,k}$ and an AC component $i^*_{ac,k}$. The real circulating current is obtained by detecting the upper leg current $i_{p,k}$ and the lower leg current $i_{n,k}$. The command voltage is calculated by:

$$v^*_{z,k} = k_{zip} \cdot (i^*_{z,k} - i_{z,k}) \quad (9)$$

$$i_{z,k} = \frac{1}{2}(i_{p,k} - i_{n,k}) \quad (10)$$

Considering the cascaded number N and the common DC bus voltage feed forward E, the command voltages for the modules in the upper and lower legs are synthesized by:

$$v^*_{p,kj} = \frac{E}{2N} - \frac{v^*_k}{N} - \frac{v^*_{z,k}}{2N} + \Delta v^*_{p,kj} \quad (11)$$

$$v^*_{n,kj} = \frac{E}{2N} + \frac{v^*_k}{N} - \frac{v^*_{z,k}}{2N} + \Delta v^*_{n,kj} \quad (12)$$

The regulator design procedure is similar to that in [21] and all of the regulator parameters are summarized in Table II.

TABLE II
CONTROL GAINS AND PARAMETERS

Symbol	experiment	Symbol	experiment
k_{vp}	0.3A/V	k_{vi}	0.5A/V
k_{ip}	8V/A	k_{ii}	100V/A
$k_{p,dc}$	0.2A/V	$k_{i,dc}$	2A/V
$k_{p,ac}$	0.3A/V	$k_{i,ac}$	0.6A/V
k_{zip}	5V/A	k_{indv}	0.2V/V

IV. THEORETICAL ANALYSIS OF THE LEG BALANCING CONTROL

A. Overview

Since the theory analyses of the overall voltage control, the phase balancing control and the individual voltage control, have been presented in [12]-[14], this paper just focuses on the leg balancing control using the "decoupling circulating current." Since the concept of decoupling current was first proposed in [20] for active power filters with the star configuration, this paper does further research on this method and applies it to the leg balancing control of the MMC topology.

B. Theoretical Analysis of the Decoupling Circulating Current

Substituting equation (7) and (8) into (11) and (12), the output voltages of the upper and lower legs in one phase-pair are obtained by:

$$v^*_{p,k} = \sum_{j=1}^{N} v^*_{p,kj} = \frac{E}{2} - v^*_k - \frac{v^*_{z,k}}{2} \quad (13)$$

$$v^*_{n,k} = \sum_{j=1}^{N} v^*_{n,kj} = \frac{E}{2} + v^*_k - \frac{v^*_{z,k}}{2} \quad (14)$$

The redistributed active power for the upper and lower legs can be derived by multiplying equation (6) with (13) and (14), respectively:

$$\overline{p_{p,k}} = \frac{1}{T_s}\int_t^{t+T_s} (v^*_{p,k} \cdot i^*_{ac,k})dt \approx -\frac{c_k \cdot V^2_{sk}}{2} \quad (15)$$

$$\overline{p_{n,k}} = \frac{1}{T_s}\int_t^{t+T_s} (v^*_{n,k} \cdot i^*_{ac,k})dt \approx \frac{c_k \cdot V^2_{sk}}{2} \quad (16)$$

where, V_{sk} is the amplitude of the k-phase source voltage and $k = a,b,c$ represent the A, B, C phases, respectively. The approximation in equations (15) and (16) are reasonable because $v^*_{z,k}$ is negligible when compared with E and v^*_k, and the source voltage $v_{s,k}$ is very close to the converter voltage v^*_k.

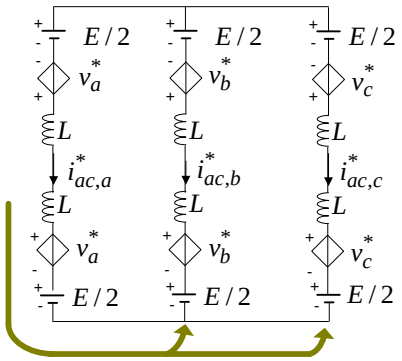


Fig. 4. Equivalent circuit for decoupling circulating current. Taking A-phase for example.

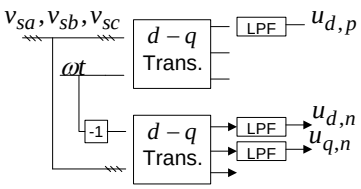


Fig. 5. Source voltages calculation.

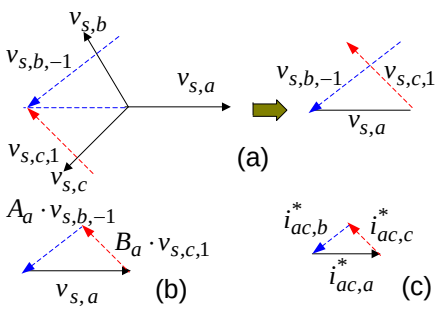


Fig. 6. Circulating current command synthesis. Taking A-phase for example.

Equations (15) and (16) indicate that active component in circulating current just causes a redistribution of the active power between the upper and lower legs without any influence on the total active power in the k-phase converter. When the active current in one phase pair flows to the other two phase pairs, it splits in two reactive currents with respect to their source voltage to avoid influencing their DC voltage. An equivalent circuit is shown in Fig. 4. Considering the interaction of the three phase pairs, the circulating current in one phase pair contains two parts: the active current for the leg balancing and the two reactive current resulting from the active currents in the other two phase pairs.

C. Circulating current command synthesis

When applying the d-q transformation and a low-pass filter (LPF) to the three-phase source voltages in Fig. 5, the positive-sequence and the negative-sequence components can be obtained by:

$$U_p = u_{d,p} \tag{17}$$

$$U_n = \sqrt{u_{d,n}^2 + u_{q,n}^2} \tag{18}$$

$$\theta = \tan^{-1}\left(\frac{u_{q,n}}{u_{d,n}}\right) \tag{19}$$

where, U_p and U_n are the amplitudes of the positive-sequence and negative-sequence voltages. θ is the original phase angle for the negative-sequence voltage. The phase angle for the d-q transformation is aligned to the positive-sequence d axis. According to equations (17) through (19), the reactive reference for each phase can be obtained by:

$$\begin{aligned} v_{s,m,n} = {} & U_p \sin(\omega t - m \cdot 2\pi/3 + n \cdot \pi/2) + \\ & U_n \sin(\omega t + \theta + m \cdot 2\pi/3 + n \cdot \pi/2) \end{aligned} \tag{20}$$

where, $m = 0,1,2$ represent the a, b, c phases, respectively and $n = 1,-1$ indicates leading or lagging by $\pi/2$.

Because the MMC structure is symmetric, the following part just takes the A-phase as an example to explain the splitting of the A-phase active current into two reactive currents for the B and C phases. The reactive vectors of $v_{s,b,-1}$ and $v_{s,c,1}$, shown in Fig. 6(a), are obtained by equation (20). In order to force the three vectors of $v_{s,a}$, $v_{s,b,-1}$ and $v_{s,c,1}$ to comply with a triangular relationship, the two coefficients of A_a and B_a are introduced by:

$$-v_{s,a} = A_a \cdot v_{s,b,-1} + B_a \cdot v_{s,c,1} \tag{21}$$

When substituting equation (20) into (21), the following two equations are obtained:

$$\begin{cases} A_a\left(U_n \cos(\theta + \dfrac{\pi}{6}) - \dfrac{\sqrt{3}U_p}{2}\right) + \dfrac{\sqrt{3}B_a}{2}(U_n - U_p) \\ = -U_p - U_n \cos\theta \\ A_a\left(U_n \sin(\theta + \dfrac{\pi}{6}) + \dfrac{1}{2}U_p\right) - \dfrac{1}{2}B_a(U_n + U_p) \\ = -U_n \sin\theta \end{cases} \tag{22}$$

By solving equation (22), the two coefficients are obtained by:

$$\begin{cases} A_a = \dfrac{U_p^2 + U_n^2}{\sqrt{3}(U_p^2 - U_n^2)} \\ B_a = \dfrac{U_p^2 + U_n^2 + 4U_pU_n \sin(\theta + \pi/6)}{\sqrt{3}(U_p^2 - U_n^2)} \end{cases} \tag{23}$$

The vectors produced in Fig. 6(b) are the basic vectors for the A-phase leg balancing control. In order to achieve a good performance, the PI regulator, shown in Fig. 2(c), is suggested to adjust the amount of the A-phase active current. Therefore, the AC circulating current commands produced by the A-phase control are given by:

$$i^*_{ac,a} = c_a \cdot v_{s,a} \quad (24)$$

$$i^*_{ac,b} = c_a \cdot A_a \cdot v_{s,b,-1} \quad (25)$$

$$i^*_{ac,c} = c_a \cdot Ba \cdot v_{s,c,1} \quad (26)$$

Equations (24) to (26) indicate that the A-phase leg balancing control will not affect the DC voltage conditions in B-phase and C-phase converters because of the reactive currents. The leg balancing controls in the three phases are completely decoupled. When considering the leg balancing controls of the total three phase pairs, the circulating current command for each phase pair includes three terms:

$$i^*_{ac,a} = c_a \cdot v_{s,a} + c_b \cdot B_b \cdot v_{s,a,1} + c_c \cdot A_c \cdot v_{s,a,-1} \quad (27)$$

$$i^*_{ac,b} = c_a \cdot A_a \cdot v_{s,b,-1} + c_b \cdot v_{s,b} + c_c \cdot B_c \cdot v_{s,b,1} \quad (28)$$

$$i^*_{ac,c} = c_a \cdot B_a \cdot v_{s,c,1} + c_b \cdot A_b \cdot v_{s,c,-1} + c_c \cdot v_{s,c} \quad (29)$$

Note that the source voltage fault condition of $U_p = U_n$ does not usually happen. This decoupling circulating current control method can be put into practical use for leg balancing control.

V. Experimental Results

Fig. 7 shows the experimental waveforms of the upper-leg output voltage and the converter current in the A-phase. Because of cascaded number of N=2, the three-level voltage waveform is produced as expected based on CPS-PWM. The converter current of the upper and lower legs can not merge together due to the DC component in the circulating current caused by the phase balancing control. However, the output current is a smooth sinusoidal waveform without any distortion or DC bias, because the circulating current just flows through the MMC structure.

Fig. 8 shows the waveforms of the source voltage $v_{s,a}$, the output current i_a, the output voltage $v_{p,a}$ and the capacitor voltage v_{pa1}. The overall voltage control was intentionally disabled during the start up procedure of the experimental system and this condition was intentionally maintained for 10 seconds after the prototype start up. During this process the capacitor voltage is apparently lower than the given value of 90V. At the end of this process, the overall voltage control was triggered and the capacitor voltage charged up slowly to the given value of 90V.

Fig. 9 shows the experiment results of phase balancing control. The four waveforms are the source voltage $v_{s,a}$ and the capacitor voltages of v_{pa1}, v_{pb1} and v_{pc1}. The phase balancing control was intentionally disabled for 10 seconds and then re-enabled. During this process, the other control remains active. As soon as the phase balancing control was enabled, the three curves quickly merge into one.

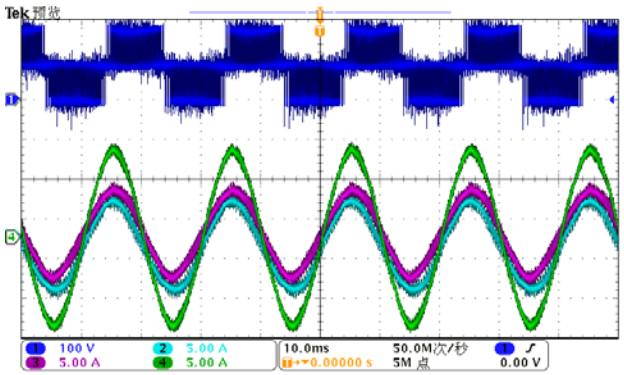


Fig. 7. Modulation effect and a-phase current.

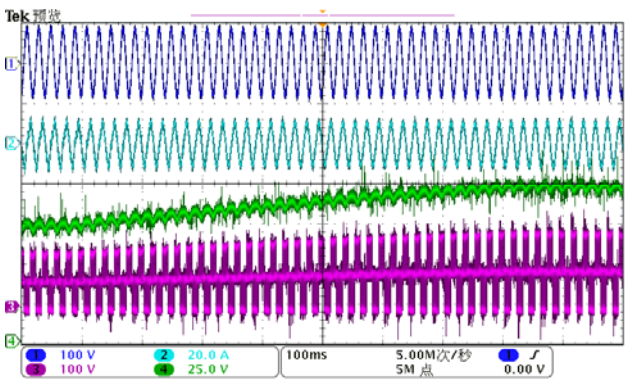


Fig. 8. Experiment waveforms verifying overall voltage control.

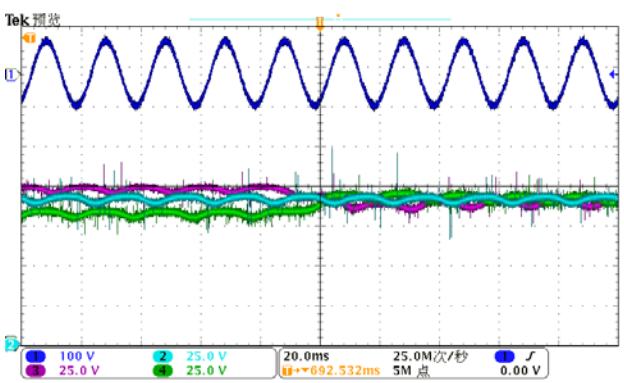
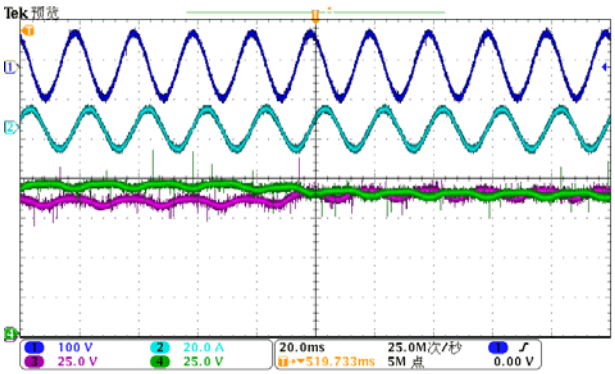
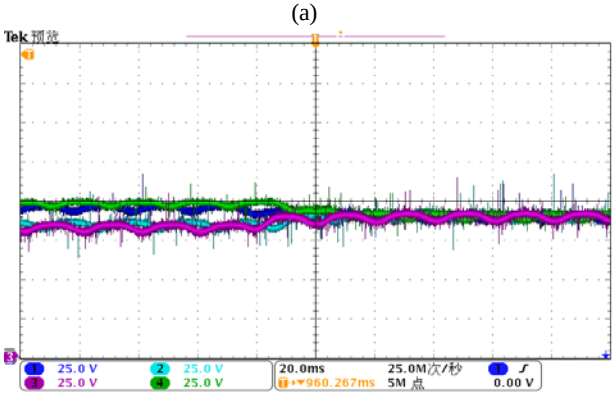


Fig. 9. Experimental waveforms confirm the effect of phase balancing control.

Fig. 10 shows the experimental waveforms of the source voltage $v_{s,a}$, the compensating current i_a and the six chopper-cell capacitor voltages v_{pa1}, v_{na1} v_{pb1}, v_{nb1}, v_{pc1} and v_{nc1}. The leg balancing control was intentionally disabled for 40 seconds while the other controls were kept active. During this period of time, the imbalance in the DC voltage between the upper and lower legs occurred. When the leg balancing control was enabled, the six curves converge to the given value of 90V.



(a)



(b)

Fig. 10. Experimental waveforms verifying the effect of leg balancing control.

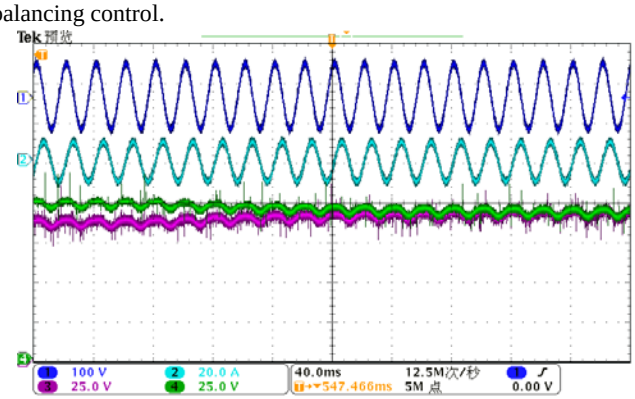


Fig. 11. Experimental waveforms verifying individual control.

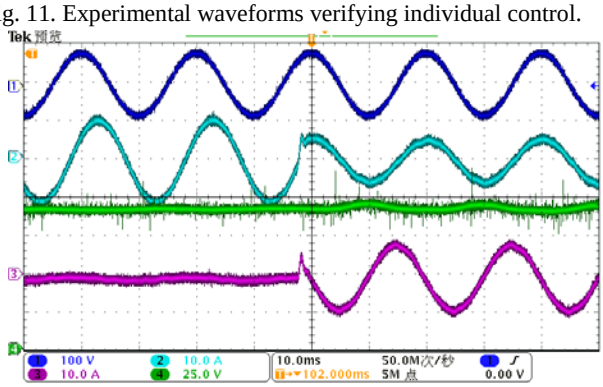
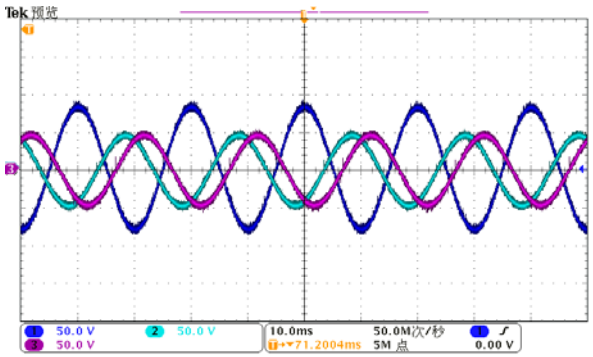
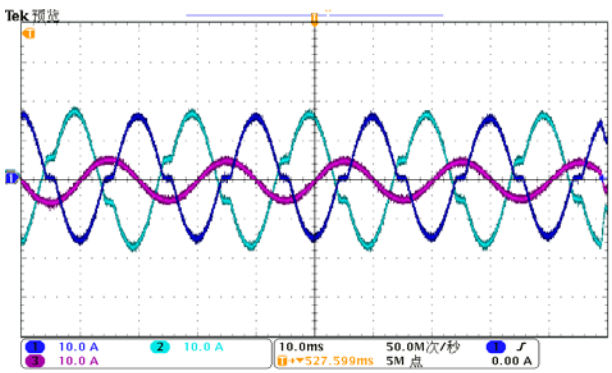


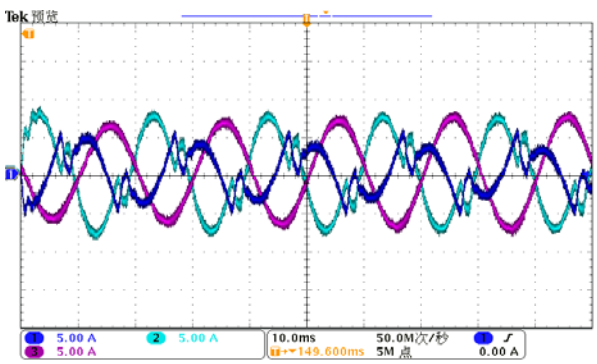
Fig. 12. Experimental waveforms verifying the performance of compensating balanced reactive load in normal power supply system.



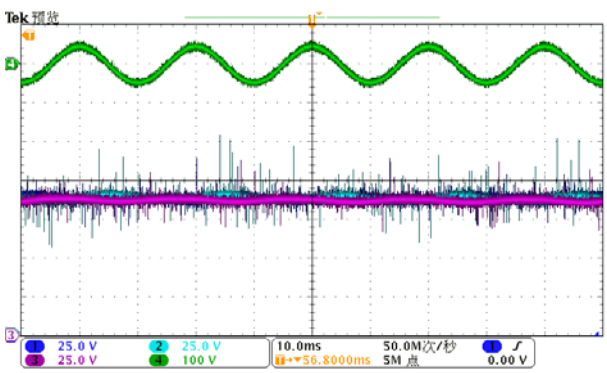
(a) Asymmetric three-phase source voltages.



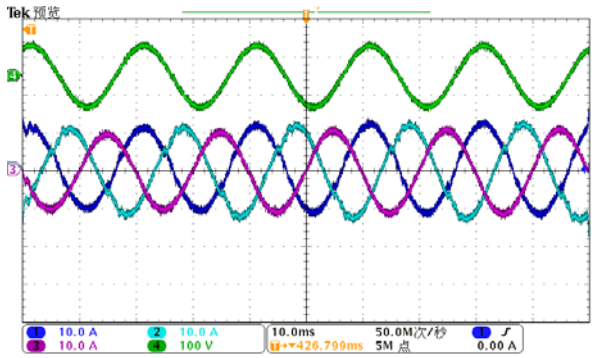
(b) Unbalanced nonlinear load.



(c) three-phase compensating current.



(d) Source voltage and capacitor voltage.



(e) A-phase source voltage and three-phase source-end current after compensation.

Fig. 13. Experimental waveforms confirm the performance of compensating unbalanced nonlinear load in asymmetric power supply system.

Fig. 11 confirms the effectiveness of the individual voltage control. Similarly, the individual voltage control was also intentionally disabled for 40 seconds during the experimental period, and then it was re-enabled. After the individual voltage control was enabled, the two DC voltage waveforms of the splitting capacitors in the a-phase upper leg quickly merge together.

Fig. 12 confirms the whole-system capability of the compensating balanced reactive load in the normal utility condition. The four curves from top to botton are: the source voltage $v_{s,a}$, the source-end current $i_{s,a}$, the capacitor voltage v_{pa1} and the output current $i_{c,a}$. When the system works in stand-by mode, there is a phase difference between the source-end current and the source voltage. As soon as the system works in the run mode, the reactive load is sufficiently compensated by the MMC system and the source-end current keeps in phase with the source voltage.

Fig. 13 records the performance of the compensating unbalanced nonlinear load under the asymmetric power supplies condition. The experiment results confirm that the unbalanced distorted load can be sufficiently compensated by the MMC system along with the proposed control strategy while keeping all of the capacitor voltage regulated and maintained at the reference value of 90V. After compensation, the three-phase source-end currents are almost balanced and kept in phase with the positive-sequence of the source voltage.

VI. Conclusions

This paper proposed a new method of decoupling circulating current for the leg balancing control of DC-link voltages. The theoretical analysis and discussion were fully expressed. The related experiments were implemented on a downscaled prototype rated at 60-V 3-kVA. The experiment results show that the MMC system along with the proposed control method can works well under all load conditions even in an asymmetric power supply system while keeping the DC capacitor voltage equalized and stabilized. This control strategy can be put into practical use.

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