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A New Zero-Voltage-Switching Bridgeless PFC, Using an Active Clamp

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Abstract

This paper presents a new ZVS single phase bridgeless (Power Factor Correction) PFC, using an active clamp to achieve zero-voltage-switching for all main switches and diodes. Since the presented PFC uses a bridgeless rectifier, most of the time, only two semiconductor components are in the main current path, instead of three in conventional single-switch configurations. This property significantly reduces the conduction losses,. Moreover, zero voltage switching removes switching loss of all main switches and diodes. Also, auxiliary switch turns on zero current condition. The presented converter needs just a simple non-isolated gate drive circuitry to drive all switches. The eight stages of each switching period and the design considerations and a control strategy are explained. Finally, the converter operation is verified by simulation and experimental results.

Key words: Active clamp, Bridgeless PFC, PWM rectifier, Zero-Voltage-Switching (ZVS)

I. INTRODUCTION

In recent decades, some standards like IEC 6100 3-2 restricts the harmonic distortion of the electronic instruments input current [1]. Therefore, many ac-dc converters are presented to comply with such standards. Off-line switching power supplies use a large capacitor as front-end rectification which causes an excessive peak current and high current distortions, and can achieve a low power factor of about 0.5-0.7 [1]. Further increasing power factor of a diode bridge input is done by adding a boost converter to shape the input current as shown in Fig. 1(a) [2]-[4]. In such a configuration, the input current always passes through three semiconductors. To reduce the conduction losses, the bridgeless PFC is introduced, Fig. 1(b) [5]. In a bridgeless topology, the input current always passes through two semiconductors, which results in less conduction loss. Moreover, each reverse diode voltage drop and its loss is reduced by applying its switch gate voltage. On the other hand, to increase power density and decrease the input current distortions of a converter, switching frequency should be increased. Yet, this increases the switching losses and electromagnetic interference (EMI) noise.

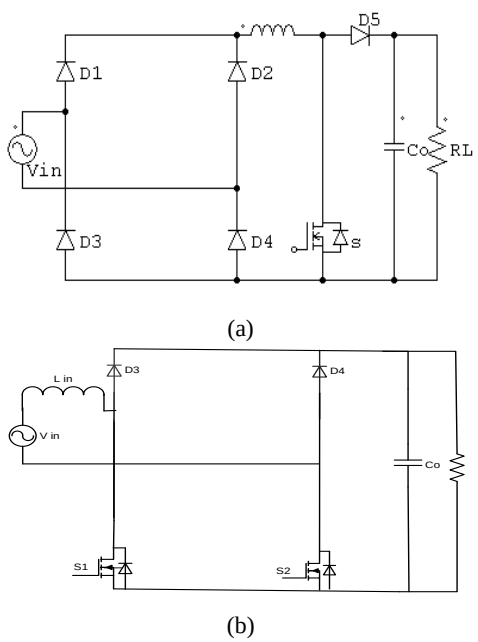

Fig. 1. (a) Conventional single-switch PFC. (b) bridgeless two switch PFC.

Thus, several zero voltage switching (ZVS) and zero current switching (ZCS) topologies have been presented to solve these

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problems [1], [7]-[26]. In ZVS condition, the drain-source capacitive losses are eliminated by holding its voltage at zero, during turn on. Therefore, this method is used for MOSFETs which have a big drain-source junction capacitor. The ZVS converter proposed in [7]-[15] uses an additional dc voltage source in order to be used in the auxiliary circuit. This voltage source is implemented by means of a voltage transformer. Its demagnetizing circuitry and a dc-dc converter , which increase the converter volume and complexity, [7]-[11]. [12]-[15] use the dc-dc converter to implement soft switching, which limits the converter voltage conversion ratio [16] . In [17] the main switches turn on and off in a ZVS condition. The auxiliary switch turns on in the ZCS conditions, but is not turned off in soft conditions. Although, the collector-emitter voltage of the auxiliary switch is clamped to the output voltage, it introduces some extra loss. Moreover, because of large dv/dt and di/dt these circuits have high EMI noises. In [1], the converter main switches operate in ZVS condition and the auxiliary switch operates in ZCS condition. In [18] the main switches turn on in ZCS condition and turn off in ZVS condition. Nevertheless, both converters [1], [18] require higher number of components.

One way to achieve ZVS condition is to use passive clampers which remove the switching energy losses from the switches. However, this removal decreases the overall efficiency of the converter.

This paper proposes an active clamp to deliver the absorbed energy to the load (instead of dissipating in passive clamps), which increases the converter efficiency as shown in Fig. 2(a). In this converter, all of the main switches and diodes operate in ZVS conditions, and the auxiliary switch (IGBT) turns on in Zero Current Switching, ZCS, and turns off in clamped voltage condition. Therefore, the switching loss of all switches and diodes are removed. In next sections, after analyzing the converter, a design strategy is presented. Finally, these analysis and designs are verified by simulation and experimental results.

II. Principle of the Proposed Zvs Bridgeless PFC

The proposed converter is shown in Fig. 2(a). The converter consists of L, $MOS_{1,2}$, $D_{1,2}$, C_o, as the main bridgeless PFC converter, and C_1, C_2,C_3, D_3, D_4, D_5, L_1, $IGBT_1$ as the auxiliary circuit to achieve soft switching . For simpler gating drives, the gate-driver signal drives the gates of both $MOS_{1,2}$, simultaneously. Therefore, both mosfets receive gate signals in every positive and negative half cycle of the input voltage. However, just one of the switches turns on in each half cycle of the input voltage. This is because the drain-source voltage of only one of the *MOSFETs* is positive at each power line half cycle. Therefore, in positive half cycle when the MOS_1 is on, the input current flows through MOS_1 in forward direction, the body diode of MOS_2 in reverse direction and charges the input

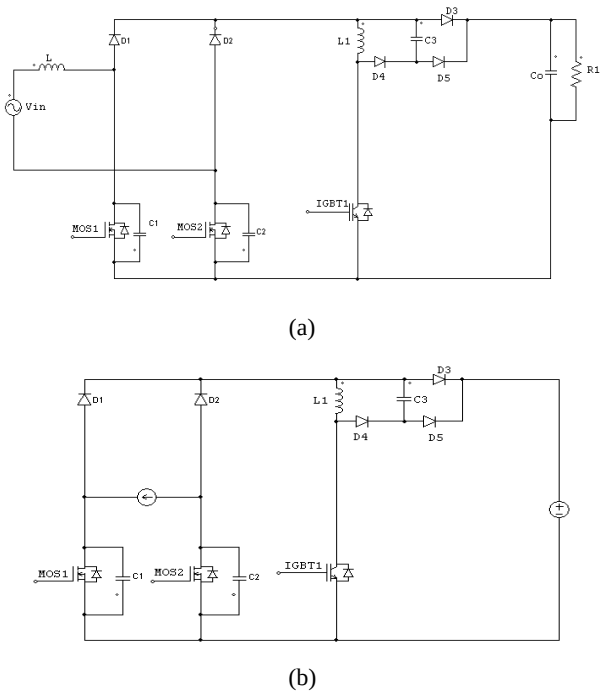

Fig. 2. (a) proposed bridgeless PFC. (b) equivalent circuit in one switching cycle.

inductance L. Also at this time, MOS_2 gate voltage is also on which cause less voltage drop and conduction losses on its reverse diode. When MOS_1 is turned off, L discharging-current flows to the load through D_1 , D_3 and the body diode of MOS_2. D_2 is off in the entire positive half cycle. In the negative half cycle of the input voltage, the converter operates in the same way, but the MOS_2 conducts in forward direction and MOS_1 conducts in reverse direction through its body diode.

D_2 conducts when MOS_2 is off. D_1 is off during the entire negative half cycle. To simplify the analysis, assume that the converter is in the steady state conditions, thus the output voltage and the input current is almost constant during one switching period. Therefore, we model the input current with a dc current source and output voltage with a dc voltage source, as illustrated in Fig. 2(b).

III. Operating Stages of the Proposed PFC

Each switching cycle of the converter can be divided into eight stages. The equivalent circuits of all stages are shown in Fig. 3, and the theoretical wave forms are shown in Fig. 4. Here, one switching periode stages during the positive half cycle of the input voltage are explained. Thus, MOS_2 is off and its body diode is on during the entire switching period. The switching stages in a negative half cycle stages are the same.

A. Stage 1 [Fig. 3(a),t0-t1]

During this stage, MOS1 is off and the input current flows to the load through D_1, D_3 and the body diode of MOS_2. During this stage, L discharges to the load.

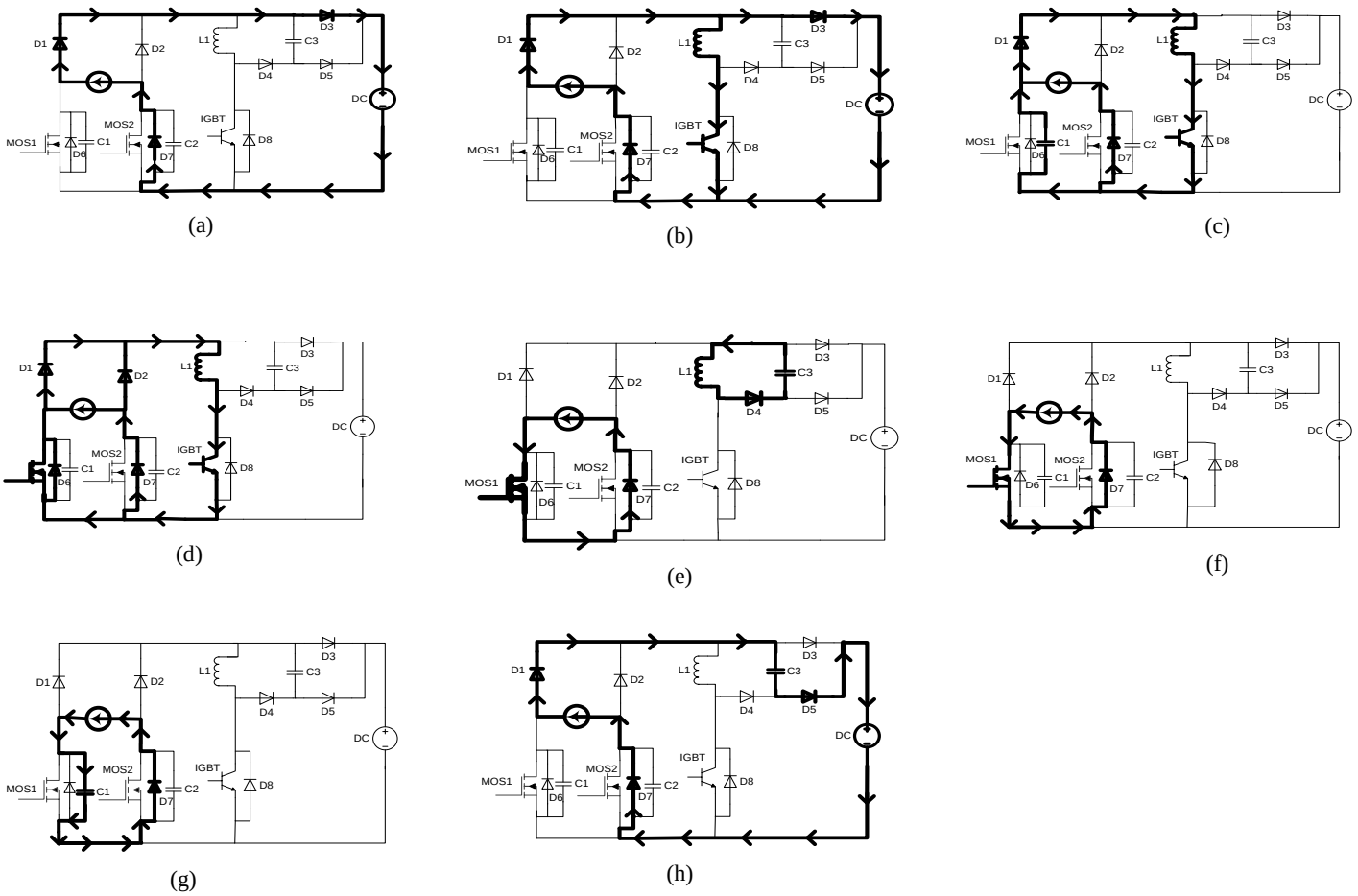

Fig. 3. Equivalent circuits of one switching stages, (a)stage1 ,(b)stage2 ,(c)stage3, (d)stage4 , (e)stage5, (f)stage6, (g)stage7, (h) stage8.

Stages 2 to 4 are to discharge C_1 and prepare ZVS condition for MOS_1 to turn on.

B. Stage 2 [Fig. 3(b), t1-t2]

This stage starts by turning on the auxiliary switch. Since inductor L_1 is in series with auxiliary switch *IGBT*, the switch current increases gradually. Therefore, this switch turns on in zero current (*ZCS*) conditions. The output voltage is applied to *L* and its current increases linearly. Since the input current is considered to be constant, by increasing the auxiliary switch current, D_3 current decreases with the same rate. Once the auxiliary switch current reaches the input current, D_3 turns off and the next stage starts. The auxiliary switch current during this stage is:

$$i_{Ax} = \frac{V_O}{L_1} t \tag{1}$$

C. Stage 3 [Fig. 3(c), t2-t3]

This stage starts when diode D_3 turns off. Then, a resonant current flows between C_1 and L_1. Therefore, L_1 current increases, while the C_1 voltage decreases. When the C_1 voltage reaches zero, the MOS_1 body diode turns on in zero voltage condition that ends this stage. During this stage the auxiliary switch current is:

$$i_{Ax} = i_{in} + \frac{V_o}{Z_{r1}} \sin(\omega_1 t) \tag{2}$$

while:

$$Z_{r1} = \sqrt{\frac{L_1}{C_1}} \tag{3}$$

$$\omega_1 = \frac{1}{\sqrt{L_1 C_1}} \tag{4}$$

D. Stage4 [Fig. 3(d), t3-t4]

This stage starts when the MOS_1 body diode turns on and freewheeling current flows through this diode, L_1, D_1 and the auxiliary switch. In this stage, MOS_1 can be turned on in zero voltage and zero current conditions. During this stage, the

auxiliary switch freewheeling current is:

$$i_{Ax} = i_{in} + \frac{V_o}{Z_{r1}} \tag{5}$$

E. Stage5 [Fig. 3(e), t4-t5]

This stage starts when the auxiliary switch turns off. Thus, MOS_1 current jumps to the value of input current and L_1 current follows into C_1 through D_4. During this and the next stages, the input inductance is charged via input voltage source.

F. Stage6 [Fig. 3(f), t5-t6]

During this stage the MOS_1 is on. The input current flows through it in its forward direction and the MOS_2 body diode. The duration of this stage, ton, (in each switching period) controls the input current. At the end of this stage, the converter controller turns the switch off.

G. Stage7 [Fig. 3(g),t6-t7]

This stage starts when MOS_1 is turned off. Because of drain-source parallel capacitor C_1, the switch voltage increases gradually. Therefore, the switch turns off in ZVS condition. Since the input current is almost constant, C_1 voltage increases linearly. The time duration of this stage is:

$$t_7 - t_6 = \frac{C_1 v_o}{i_{in}} \tag{6}$$

H. Stage8 [Fig. 3(h), t7-t8]

This stage starts when the voltage across the capacitor C_1 reaches the output voltage. At this time, D_1 turns on in zero voltage condition. Since C_3 has some charge from the previous stages, the voltage across D_3 is positive which keeps it off. The input current flows through C_3, D_1 and D_5 to the load. The C_3 voltage reduces linearly and this stage ends when this voltage reaches zero. At this moment, D_5 turns off, and D_3 turns on in zero voltage condition and the converter returns back to the first stage. The ideal wave forms of this converter in one switching cycle are shown in fig.4.

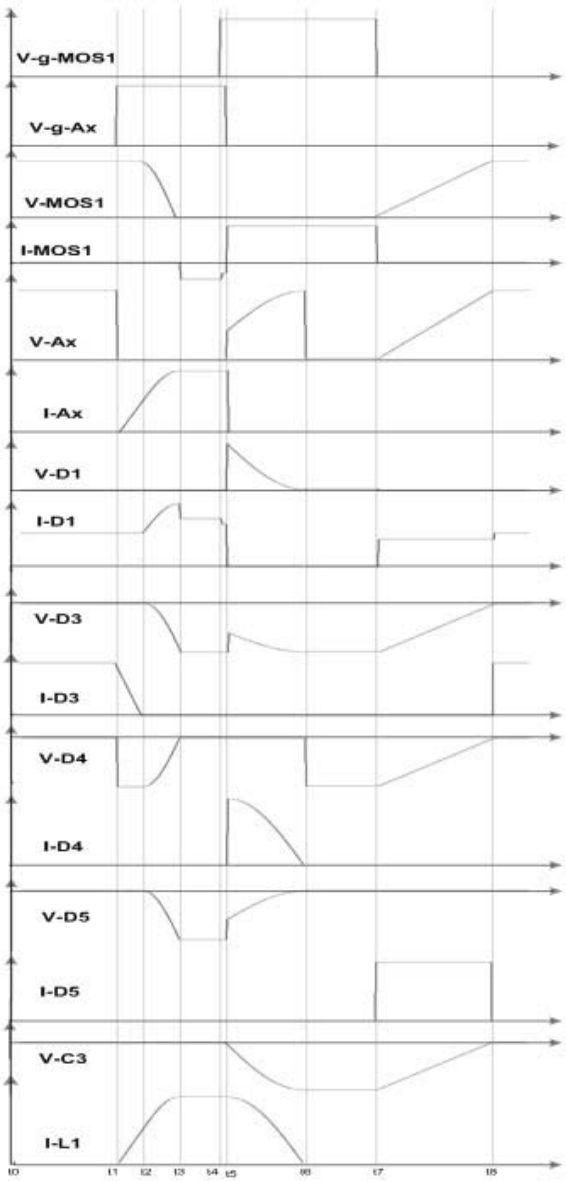

Fig. 4. Theoretical wave forms of one switching stages frequency.

IV. Design Steps

The PFC converter can be designed in the following 4 step procedure.

A. STEP 1.

Input voltage, output voltage and output current should be given. The RMS value of input voltage can vary from 96 to 265 volts, the output dc voltage is 400 volts and maximum output power is 1000 watts.

B. STEP 2.

The switching frequency should be selected much higher than the input voltage frequency, to reduce input current low-frequency distortion. For this converter the switching frequency is chosen *80 kHz*, by selecting the maximum input current ripple of *10%*, the maximum input current, which is the maximum current stress of the switches $MOS_{1,2}$, can be calculated.

$$i_{in.\max} = \frac{\sqrt{2}\,p_{0.\max}}{v_{in.\min}} + \frac{\Delta i_{in}}{2} \tag{7}$$

The maximum voltage stress of these switches and diodes is not larger than the output voltage, which is an advantage of this converter. With the rating values of the converter, which are specified in step1, the calculated maximum input current is ($i_{in,max}$=*16.5 A*) and the switches and diodes voltage stress is 400 volts.

C. STEP 3.

The resonant parameters are calculated in this step. To minimize the effect of the auxiliary circuit on the main converter. The sum of stages 5 and 6 periods should be negligible compared with the switching frequency period, thus

$$t_3 - t_1 << \frac{1}{F_{sw}} \Rightarrow \frac{i_{in,Max} L_1}{V_O} + \frac{\sqrt{L_1 C_1}}{4} << \frac{1}{80000} \quad (8)$$

C_1 and C_2 should be selected large enough to provide a capacitor charge time for the maximum input current.

$$\frac{i_{in,MAX} t_f}{V_O} < C_{1,2} \quad (9)$$

Selecting the maximum of $i_{Lr1} = 1.2\ i_{in,max}$ from Eq. (5) the L_{r1} can be selected as:

$$L_1 = \left(\frac{5V_o}{i_{in,\max}}\right)^2 C_1 \quad (10)$$

Where $i_{in,max}$ is the maximum input current.

Using the above equations, $C_{1,2}$ and L_1 are selected as 5×10^{-9} *(F)* and 40×10^{-6} *(H)*, respectively. Values here are over designed to show the results, clearly. The maximum voltage stress across the AX_{sw} is Vo and its maximum current can be calculated from Eq(5).

The peak current of diodes $D_{1,2,4}$ is the same as that of i_{L1}, and their maximum voltage is V_o. The maximum possible current stress for diodes $D_{3,5}$ is the same as the input current and their voltage rating is equal to the output voltage.

B. STEP 4.

By choosing *10%* input current ripple and minimizing the output voltage ripple, using [29], L_{in} and C_o are calculated as L_{in}*=650(μH)* and C_o *=940(μF)*, respectively.

V. Control Strategy

The proposed converter employs peak current mode controller. Fig. 5 shows a simplified diagram of the peak current controller. The converter can also be controlled using a conventional average current PFC controller IC, such as UC3854. This controller has two feedback loops: a voltage feedback loop to control the average output voltage; and a current feedback loop to shape the input current. The voltage control loop has a limited bandwidth, small enough to cancel the effect of output voltage ripple on the controller. For *50 Hz* input voltage frequency, it is necessary to select the bandwidth of the voltage control loop much less than *100 Hz* [27]. The input voltage is sensed and its absolute value is used as synchronous signal. This synchronous signal is multiplied by the voltage-controller output signal, to make the current reference signal. The input current is also sensed and its absolute value is compared with the current reference signal, using a comparator. This comparator output is used as the *"Set"* signal for an asynchronous rising-edge triggered *S-R* flip-flop. An oscillator is used to reset this *S-R* flip-flop, which also determines the switching frequency. The flip-flop output is used as the input of a simple logic circuit to produce the switching signals for $MOS_{1,2}$ and AX_{sw}. The main switches' ($MOS_{1,2}$) must be turned on after an appropriate delay after AX_{sw} is closed, to let stages 2 and 3 be passed. This delay is produced by a time delay block in the controller. After this delay, the main switch can be turned on and the auxiliary switch can be turned off. The AX_{sw} gating turn-on signal (T_{on}, AX_{sw}) is produced by a rising edge triggered mono-stable. The duration of its on-time should be long enough to let the stage 2 and 3 to pass. According to these assumptions, the durations t_{delay} and T_{on}, AX_{sw} are selected to be *2.2×10-6 (sec)* and *2.1×10-6 (sec)*, respectively.

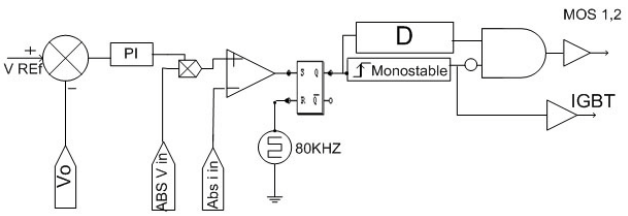

Fig. 5. Peak Current Controller.

VI. Simulation Results

The proposed converter is simulated; using *PSIM*. The parameters settings are set as calculated in section III. The simulation parameters and quantities are chosen as: step size: *1×10-8 (sec)*; input voltage: *220 Vrms, 50 Hz*; the output voltage: *400 V DC*; the output power: *1000* Watts; and the switching frequency f_{sw}: 80 *kHz*. The converter wave-forms are as shown in Fig. 6. Fig 6(a) shows that the input current is very close to sinusoidal and is in phase with the input voltage. Fig. 6(b) shows the input current harmonics which are below the "IEC 6 1000-3-2 class A" level [28]. Fig. 6(c) and (d) show soft-switching of the main diode and switch respectively. The main switch turns off in ZVS condition and turns on in ZVZCS conditions. Fig. 7(e) shows the AX_{sw} voltage, current and it's ZCS turn on. Fig. 7(f) shows the resonant inductors current and the C_3 voltage.

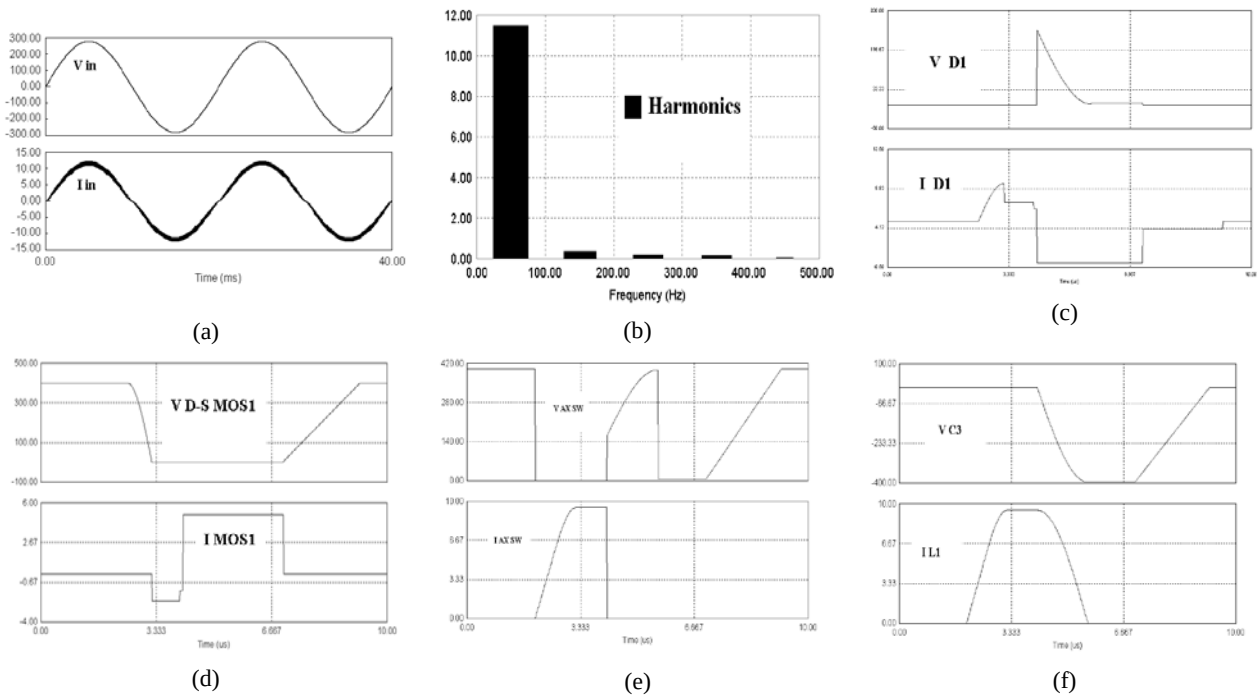

Fig. 6. (a) Input voltage and input current, (b) input current harmonics, (c) diode D_1 voltage and current, (d) MOS_1 voltage and current, (e) voltage and current of AX_{sw} (f) L_1 current and C_3 voltage.

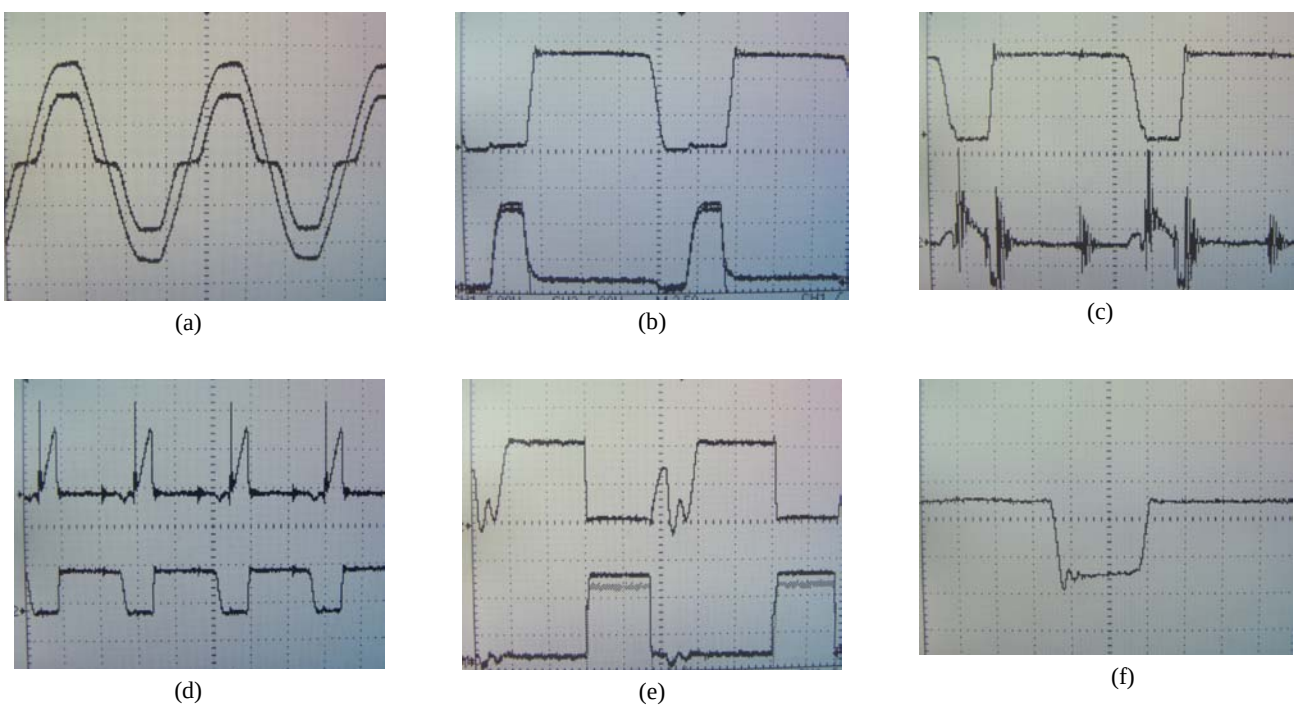

Fig. 7. (a) Input voltage and input current *50v/div* and *6A/div*, time:*5m(SEC)/div*. (b) MOS_1 Drain-Source voltage *250 v/div* and its gate signal, time:*2μ(SEC) /div*. (c) MOS_1 current *6A/div*, time:*2μ(SEC) /div*. (d) Diode D_1 voltage and current *250v/div* and *6A/div*, time:*2 μ(SEC) /div*. (e) AX_{sw} voltage *250v/div* and its base signal, time:*1 μ(SEC) /div*.

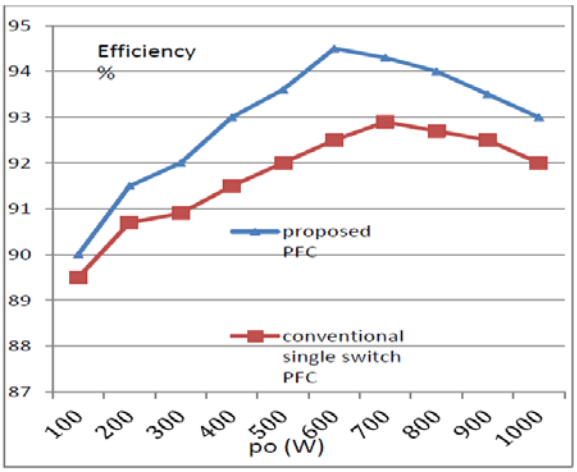

Fig. 8. Measured efficiency comparison of proposed PFC and conventional single- switch PFC.

VII. Experimental Results

It is clear that this switch turns on and off in ZVS condition. Fig. 7(c) shows the MOS_1 current and its gate signal. It can be seen that this switch turns on in ZCS condition. Therefore, MOS_1 turns on in ZVZCS conditions and turns off in ZVS condition. As mentioned in section (II), the MOS_2 operates in the same way as MOS_1, due to the circuit symmetry. Fig. 7(d) shows the soft switching of diode D_1. Fig 7(e) shows the base signal and the voltage across the AX_{sw}. Fig 7(f) shows the C_3 voltage. The converter measured efficiency at input voltage of*120 Vrms* versus output power is shown in Fig. 8. This Fig. shows that the efficiency is higher than a conventional single-switch PFC.

VIII. Conclusion

This paper presents a new ZVS, bridgeless, PFC converter. This converter uses an active clamp, to achieve soft-switching condition for all switches and diodes. All of the main switches and diodes operate in ZVS condition and the auxiliary switch AX_{sw} turns on in ZCS condition and turns off while its voltage is clamped by capacitor C_3, which removes most of its switching losses. In addition, since the proposed PFC converter is bridgeless, the converter conduction loss is lower than the conventional single-switch PFC converters. Since in most of the times there are only two semiconductors in the main current path (instead of three in the conventional ones) it has lower conduction losses. Moreover, the proposed converter has no extra voltage and/or current stress on main switches. Furthermore, a simple non-isolated drive circuit can be used to drive all switches. The switching stages are explained, and design steps have been described in this paper. A control strategy is also presented. The theoretical results have been verified with simulation and experimental results. The estimated (via simulation) converter efficiency at input voltage of 120Vrms and different load conditions is between 90.5% and 95.5%. The measured power factor at the 400 W output power is 0.93.

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