

Interleaved Boost-Flyback Converter with Boundary Conduction Mode for Power Factor Correction

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Abstract

This paper presents a new interleaved pulse-width modulation (PWM) boost-flyback converter to achieve power factor correction (PFC) and regulate DC bus voltage. The adopted boost-flyback converter has a high voltage conversion ratio to overcome the limit of conventional boost or buck-boost converter with narrow turn-off period. The proposed converter has wide turn-off period compared with a conventional boost converter. Thus, the higher output voltage can be achieved in the proposed converter. The interleaved PWM can further reduce the input and output ripple currents such that the sizes of inductor and capacitor are reduced. Since boundary conduction mode (BCM) is adopted to achieve power factor correction, power switches are turned on at zero current switching (ZCS) and switching losses are reduced. The circuit configuration, principle operation, system analysis, and design consideration of the proposed converter are presented in detail. Finally, experiments conducted on a laboratory prototype rated at 500W were presented to verify the effectiveness of the converter.

Key words: Interleaved PWM, PFC, ZCS

I. INTRODUCTION

Recently high voltage step-up converters have been proposed for fuel-cell based DC converter [1]-[3], battery-discharged DC converter in UPS system [4]-[5], car auxiliary power supplies [6], automobile HID headlamps [7], [8], and medical equipment. The conventional boost converter cannot realize high voltage step-up due to the narrow allowed duty cycle. If the high duty cycle is used in the boost converter, the nonlinear voltage conversion characteristic due to the parasitic resistance is difficult to regulate output voltage. The conduction loss of power MOSFET also depends on the duty cycle. Cascade boost converters in [9]-[11] and the coupled-inductor converters in [12]-[16] have proposed for non-isolated circuit applications. Therefore, the drawback of the conventional boost converter can be overcome by these circuit topologies with high voltage step-up applications. In order to reduce the environmental power pollution and save energy waste, Environment Protection Agency (EPA) and Climate Saver Computing

Initiative (CSCI) have been proposed to increase circuit efficiency for modern power supply units. Therefore, power factor correction (PFC) techniques [17]-[23] have been demanded for power converters with $P_o \geq 75W$. Thus, the reactive power and line current harmonics are eliminated, and a sinusoidal line current is drawn from utility side.

This paper presents a new circuit topology to achieve high voltage step-up characteristic compared to the conventional boost converter and flyback converter. Since the adopted converter is operated in boundary conduction mode and interleaved pulse-width modulation (PWM), the input line current can be controlled to be a sinusoidal waveforms and the input ripple current can be partially cancelled each other. Therefore, input power factor can be controlled to be unity and total harmonic distortion of line current is reduced. The input inductance can also be reduced due to the interleaved PWM scheme. The boost and flyback converters with one MOSFET are connected in series at output side. The output voltage is the summation of these three voltages so that the converter has high output voltage. The advantages of the proposed converter are easy to be implemented with the commercial PWM IC such as UCC28061, high voltage step-up, less power switch count and wide duty cycle control. Experiments, taken from a laboratory prototype rated at 500W, are presented to demonstrate the circuit performance and verify the feasibility of the converter.

Manuscript received Jan. 7, 2011; revised Jun. 13, 2012

Recommended for publication by Associate Editor Byung-Cho Choi.

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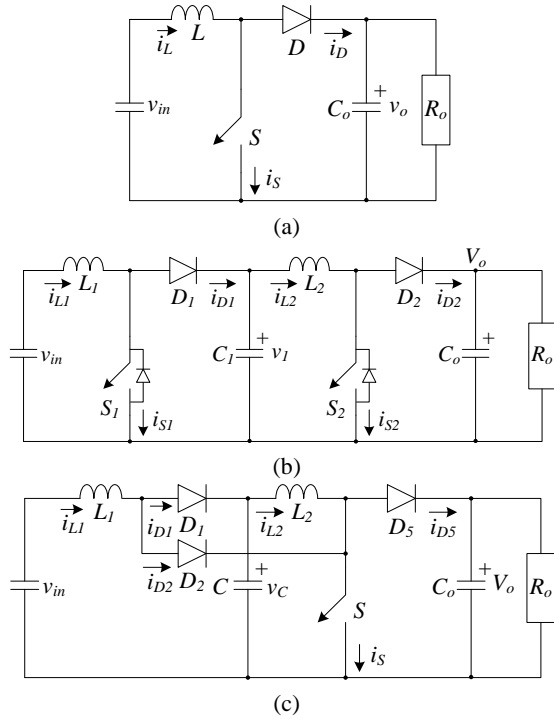


Fig. 1. Circuit configurations, (a) Traditional boost converter. (b) cascade boost converter. (c) Cascade boost converter with single switch.

II. CIRCUIT CONFIGURATION

Fig. 1(a) gives the circuit configuration of the conventional boost converter. The boost converter can step-up the input voltage $V_o/V_{in}=1/(1-\delta)$, where δ is the duty cycle of switch S . Generally the high step-up voltage gain is required in many emerging applications. But the boost converter should be operated at high duty cycle to achieve high voltage gain. Therefore, power is delivered to output load during a short period. This will result in low circuit efficiency. Fig. 1(b) gives the circuit configuration of the cascade boost converter. The voltage conversion ratio of the cascade boost converter is $V_o/V_{in}=1/(1-\delta)^2$. The main disadvantages of the cascade boost converter are more circuit components and complex control scheme. In order to reduce power components and to simplify the control scheme, switches S_1 and S_2 in Fig. 1(b) can be reduced to only one switch as shown in Fig. 1(c). Therefore, the general PWM IC can be used to regulate the output voltage with high step-up gain. Fig. 2 shows the circuit configuration of the proposed converter with high step-up voltage conversion. There are two circuit modules in the proposed converter to achieve DC/DC power conversion, output voltage regulation and partially ripple current cancellation. In each module, the DC bus voltages of boost circuit, including L_1 , S_1 , D_1 and C_1 , and flyback circuit, including T_1 , S_1 , D_2 and C_2 , are connected in series to step-up output voltage. If the turns ratio of T_1 and T_2 is unity,

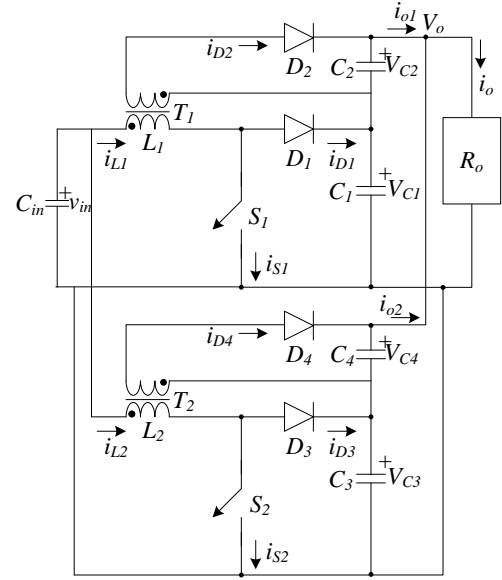


Fig. 2. Circuit configuration of the proposed converter.

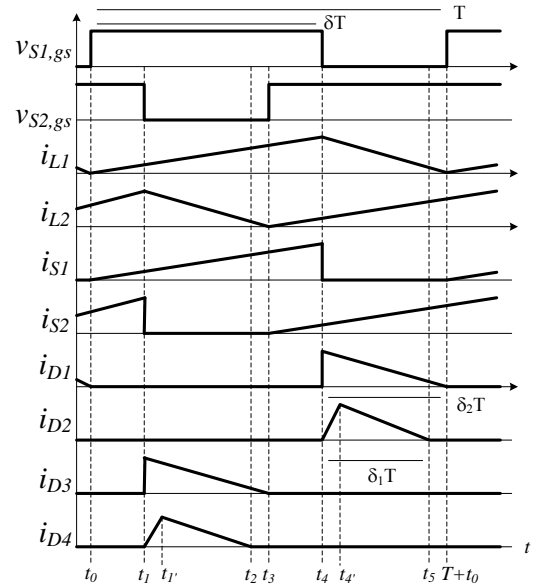


Fig. 3. Key waveforms of the proposed converter.

the total conversion ratio between DC bus voltage and input voltage is greater than or equal to $(1+\delta)/(1-\delta)$ with DCM or CCM operation, respectively. This voltage conversion ratio is larger than the DC voltage conversion ratio of the conventional boost converter and flyback converter with unity turns ratio. Since the input inductor currents are interleaved by one-half of the switching period, the input ripple current is partially cancelled each other. Thus the input capacitance can be reduced.

III. OPERATION PRINCIPLE

In order to simplify the circuit analysis, some assumptions are made. Capacitances of $C_1 \sim C_4$ are large enough such that

voltages $V_{C1} \sim V_{C4}$ are constant. Magnetizing inductances of T_1 and T_2 are identical $L_1 = L_2 = L_m$. The turns ratio of T_1 and T_2 is $n = n_p/n_s$. All power semiconductors are ideal. The leakage inductances of T_1 and T_2 are identical. Based on the above assumptions, the proposed converter has six operation modes in a switching cycle. Fig. 3 shows the time sequence of key waveforms in the proposed converter. Before time t_0 , S_1 is off and S_2 is on. Diode currents $i_{D2} \sim i_{D4}$ are all zero.

Mode 1 [$t_0 \leq t < t_1$]: At time t_0 , switch S_1 is turned on. Thus diode D_1 is reverse biased. The voltage across inductor L_1 is equal to v_{in} . Since both switches S_1 and S_2 are in the on-state. Inductor currents i_{L1} and i_{L2} increase with the slope rate of V_{in}/L_m . The secondary winding voltages of T_1 and T_2 are negative such that diodes D_2 and D_4 are reverse biased. Since diodes D_2 and D_4 are off, we can obtain $i_{L1} = i_{Lm1}$ and $i_{L2} = i_{Lm2}$. The switch currents $i_{S1} = i_{L1}$ and $i_{S2} = i_{L2}$. Output capacitors $C_1 \sim C_4$ are discharged to supply load current. This mode ends at time t_1 when switch S_2 is turned off.

Mode 2 [$t_1 \leq t < t_2$]: At time t_1 , switch S_2 is turned off. The energy stored in inductor L_2 is released to charge capacitances C_3 and C_4 . Diodes D_3 and D_4 are conducting. The magnetizing inductance voltage $v_{Lm2} = -nV_{C4}$. Thus, the magnetizing current i_{Lm2} decreases as following.

$$i_{Lm2}(t) = i_{Lm2}(t_1) - \frac{nV_{C4}}{L_m}(t - t_1) \quad (1)$$

where n is the turns ratio between the primary winding and the secondary winding of T_1 and T_2 . The inductor current i_{L2} also decreases.

$$i_{L2}(t) = i_{L2}(t_1) + \frac{v_{in} + nV_{C4} - V_{C3}}{L_{lk}}(t - t_1) \quad (2)$$

Thus, the diode current i_{D4} is given as:

$$i_{D4}(t) = n[i_{Lm2}(t) - i_{L2}(t)] \quad (3)$$

In time interval [$t_1 \leq t < t_1'$], diode current i_{D4} increases from zero ampere. After time t_1' , the diode current i_{D4} decreases from its maximum value due to that i_{Lm2} and i_{L2} are both decreasing. In converter cell 1, the inductor current i_{L1} continuously increases in this mode. The time interval ends at time t_2 when diode current i_{D4} is decreased to zero. Then, diode D_4 is turned off at ZCS. There is no reverse recovery loss in diode D_4 .

Mode 3 [$t_2 \leq t < t_3$]: At time t_2 , diode D_4 is turned off at ZCS. Thus, the diode current i_{D3} is given as:

$$i_{D3}(t) = i_{D3}(t_2) + \frac{v_{in} - V_{C3}}{L_{lk} + L_m}(t - t_2) \quad (4)$$

Since $v_{in} < V_{C3}$, diode current i_{D3} continuously decreases in this mode. In converter cell 1, the inductor current i_{L1} continuously increases in this mode. This mode ends at time t_3 when diode current i_{D3} is decreasing to zero. Then switch S_2 is turned on at this instant to achieve ZCS turn-on.

Mode 4 [$t_3 \leq t < t_4$]: This mode starts at time t_3 when diode current $i_{D3} = 0$ and S_2 is turned on. Thus, the circuit operation is the same as the circuit operation in mode 1. Both inductor

currents i_{L1} and i_{L2} increase in this mode and diodes $D_1 \sim D_4$ are all reverse biased. This mode ends at time t_4 when switch S_1 is turned off.

Mode 5 [$t_4 \leq t < t_5$]: At time t_4 , switch S_1 is turned off. The energy stored in inductor L_1 is released to charge capacitances C_1 and C_2 . Diodes D_1 and D_2 are conducting. The magnetizing voltage $v_{Lm1} = -nV_{C2}$. Thus, the magnetizing current i_{Lm1} decreases as following.

$$i_{Lm1}(t) = i_{Lm1}(t_4) - \frac{nV_{C2}}{L_m}(t - t_4) \quad (5)$$

The inductor current i_{L1} also decreases.

$$i_{L1}(t) = i_{L1}(t_4) + \frac{v_{in} + nV_{C2} - V_{C1}}{L_{lk}}(t - t_4) \quad (6)$$

The diode current i_{D2} is given as:

$$i_{D2}(t) = n[i_{Lm1}(t) - i_{L1}(t)] \quad (7)$$

In time interval [$t_4 \leq t < t_4'$], diode current i_{D2} increases from zero ampere. After time t_4' , the diode current i_{D2} decreases from its maximum value due to that i_{Lm1} and i_{L1} are both decreasing. In converter cell 2, the inductor current i_{L2} increases in this mode. At time t_5 , diode current i_{D2} is decreased to zero. Then diode D_2 is turned off at ZCS. There is no reverse recovery loss in diode D_2 .

Mode 6 [$t_5 \leq t < T + t_0$]: This mode starts at time t_5 when diode current $i_{D2} = 0$. Then diode D_2 is off at ZCS. The diode current i_{D1} is given as:

$$i_{D1}(t) = i_{D1}(t_5) + \frac{v_{in} - V_{C1}}{L_{lk} + L_m}(t - t_5) \quad (8)$$

Since $v_{in} < V_{C1}$, diode current i_{D1} is decreasing in this mode. The inductor current i_{L2} continuously increases in this mode. At time $T + t_0$, diode current i_{D1} is decreased to zero. Then switch S_1 is turned on at this instant to achieve ZCS turn-on. Then, the operation mode in this switching cycle is completed and the circuit goes to the next switching operation.

IV. STEADY STATE ANALYSIS

In steady state analysis, transformers T_1 and T_2 are modeled as the magnetizing inductors L_1 and L_2 and leakage inductors L_{lk} . Based on the voltage-second balance on the primary sides of T_1 and T_2 , we can derive the average voltages V_{C1} and V_{C3} .

$$V_{C1} = V_{C3} = \frac{v_{in}}{1 - \delta} \quad (9)$$

where δ is the duty cycle of switches S_1 and S_2 . In the same manner, the average voltages V_{C2} and V_{C4} can be obtained due to the voltage-second balance on the secondary sides of T_1 and T_2 .

$$V_{C2} = V_{C4} = \frac{k[v_{in}(1 - \delta_1) - V_{C1}(1 - \delta - \delta_1)]}{n\delta_2(1 + k)} \quad (10)$$

where $k = L_m / L_{lk}$, $(\delta_1 T)$ is the turn-on time of diodes D_2 and D_4 and $(\delta_2 T)$ is the turn-on time of diodes D_1 and D_3 .

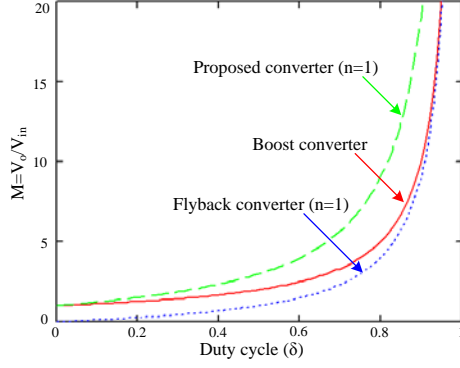


Fig. 4. Comparisons of the voltage conversion ratios of the proposed converter, boost converter and flyback converter with unity turns ratio.

Thus the DC voltage conversion ratio of the proposed converter is derived as:

$$M = \frac{V_o}{V_{in}} = \frac{V_{C1} + V_{C2}}{v_{in}} = \frac{1}{1-\delta} + \frac{k[(1-\delta_1) - V_{C1}(1-\delta-\delta_1)/v_{in}]}{n\delta_1(1+k)} \quad (11)$$

If we assumed that the leakage inductance is neglected and the turn-on time is $\delta_1 T = T - \delta T$, then the DC voltage conversion ratio in (11) can be further expressed as:

$$M = \frac{V_o}{V_{in}} = \frac{1}{1-\delta} + \frac{\delta}{n(1-\delta)} = \frac{n+\delta}{n(1-\delta)} \quad (12)$$

Fig. 4 shows the theoretical voltage conversion ratio of boost converter, flyback converter and the proposed converter. It is clear that the proposed converter has higher voltage step-up gain. In time interval $[t_0-t_4]$, S_1 is in the on-state. The following equations can be derived:

$$i_{L1}(t_4) = i_{Lm1}(t_4) = \frac{v_{in}\delta T}{L_m + L_{lk}} \quad (13)$$

In mode 5 $[t_4-t_5]$, D_1 and D_2 are conducting. Thus, the leakage inductor voltage can be derived as:

$$v_{Lk} = v_{in} + nV_{C2} - V_{C1} < 0 \quad (14)$$

The inductor current i_{L1} in mode 5 is given as:

$$i_{L1}(t) = i_{L1}(t_4) + \frac{v_{in} + nV_{C2} - V_{C1}}{L_{lk}}(t - t_4) = \frac{v_{in}\delta T}{L_m + L_{lk}} + \frac{v_{in} + nV_{C2} - V_{C1}}{L_{lk}}(t - t_4) \quad (15)$$

The magnetizing current of T_1 in mode 5 is given as:

$$i_{Lm1}(t) = i_{Lm1}(t_4) - \frac{nV_{C2}}{L_m}(t - t_4) = \frac{v_{in}\delta T}{L_m + L_{lk}} - \frac{nV_{C2}}{L_m}(t - t_4) \quad (16)$$

The diode current i_{D2} is expressed as:

$$i_{D2}(t) = n[i_{Lm1}(t) - i_{L1}(t)] \quad (17)$$

The voltage stresses of diodes are given as:

$$v_{D1, stress} = v_{D3, stress} = V_{C1} = \frac{v_{in}}{1-\delta} \quad (18)$$

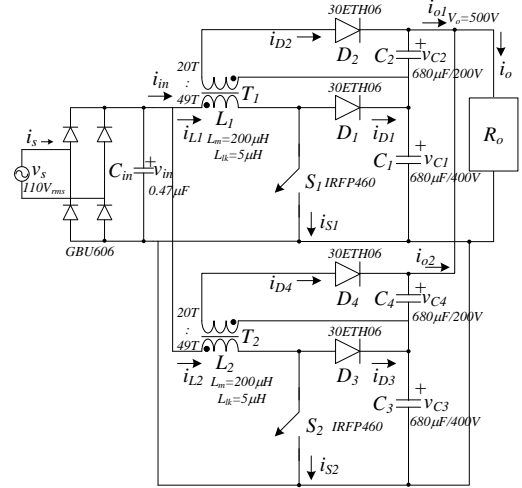


Fig. 5. Circuit configuration and specifications of the prototype circuit.

$$v_{D2, stress} = v_{D4, stress} = v_{in} / n + V_{C2} \quad (19)$$

The voltage stress of switches S_1 and S_2 is given as:

$$v_{S1, stress} = v_{S2, stress} = \frac{v_{in}}{1-\delta} \quad (20)$$

V. EXPERIMENTAL RESULTS

The proposed converter with BCM operation for high step-up voltage conversion was built and tested to achieve unity power factor, line current harmonics reduction and partially ripple current cancellation at input and output sides. Experimental results based on a laboratory 500W prototype are provided to verify the effectiveness of the proposed converter. Fig. 5 gives the circuit configuration of the prototype circuit. An interleaved BCM mode control IC UCC28061 is adopted to generate two PWM signals and regulate output voltage. The design procedure of the boost PFC with BCM scheme can be found in the application notes from Texas Instruments website. Since the adopted converter is operated at BCM mode, an input capacitor C_{in} is added after the diode rectifier to filter high frequency harmonic current. Fig. 6 shows the measured line voltage v_s and line current i_s at 30% and 100% load conditions. It is clear that line current is a sinusoidal waveform. The measured power factor is 0.98 and total harmonic distortion of line current is 18.9%. Fig. 7 gives the measured results of $v_{S1,gs}$, i_{in} , i_{L1} and i_{L2} at 30% and 100% load conditions. The input current i_{in} has twice switching frequency compared to the frequency of i_{L1} and i_{L2} . Thus, the boost inductances L_1 and L_2 can be reduced. Fig. 8 gives the measured results of $v_{S1,gs}$, $v_{S2,gs}$, i_{S1} and i_{S2} at 30% and 100% load conditions. Fig. 9 shows the measured results of $v_{S1,gs}$, $v_{S2,gs}$, i_{D1} and i_{D3} at 30% and 100% load conditions. Fig. 10 gives the measured waveforms of $v_{S1,gs}$, $v_{S2,gs}$, i_{D2} and i_{D4} at 30% and 100% load conditions. From Figs. 7-10, we can see that the inductor currents and diode currents are interleaved each other. Thus input and output ripple currents are reduced such that the input and

output capacitances can be reduced. Since BCM operation is adopted in the proposed converter, all diodes are turned off at ZCS. Thus, there is no reverse recovery loss on each diode. Two power switches are turned on at ZVS. The measured circuit efficiencies of the proposed converter are shown in Fig. 11. The proposed converter has better circuit efficiency compared with the conventional interleaved boost converter with BCM scheme.

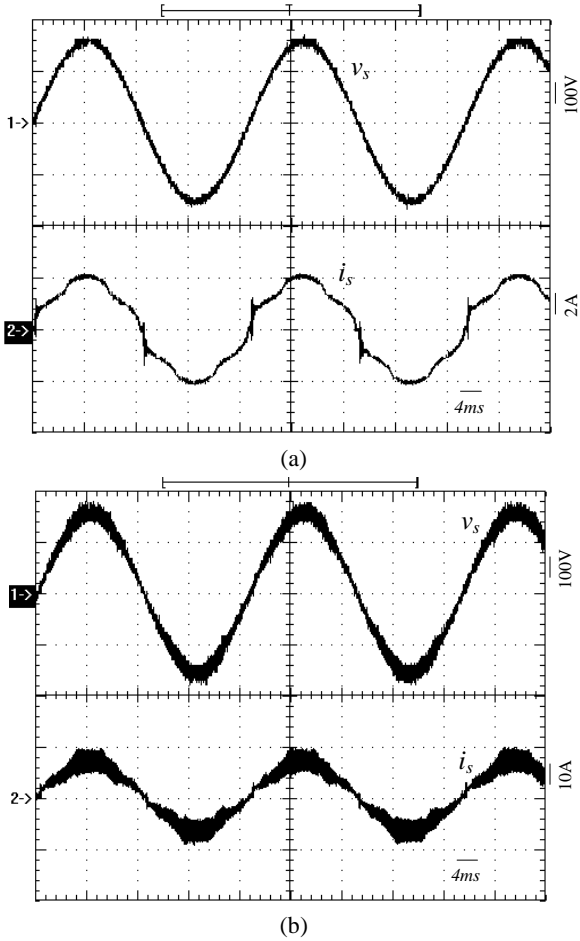


Fig. 6. Measured line voltage v_s and line current i_s at (a) 30% load (b) full load.

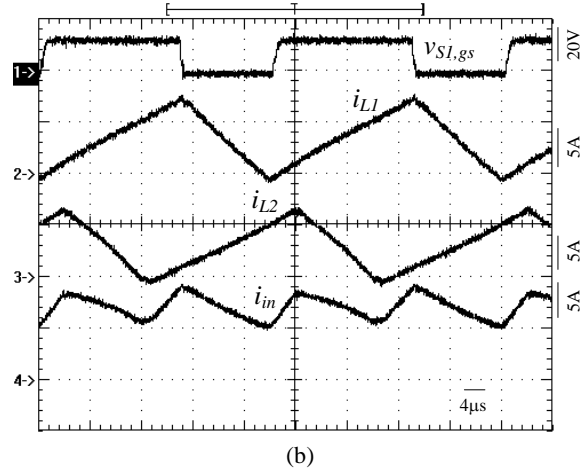
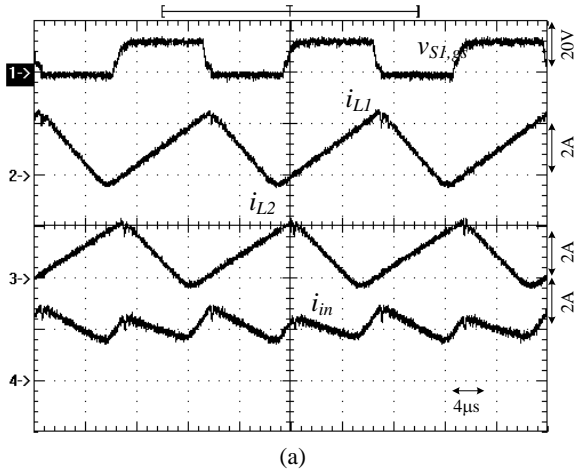


Fig. 7. Measured results of $v_{S1,gs}$, i_{in} , i_{L1} and i_{L2} at (a) 30% load (b) full load.

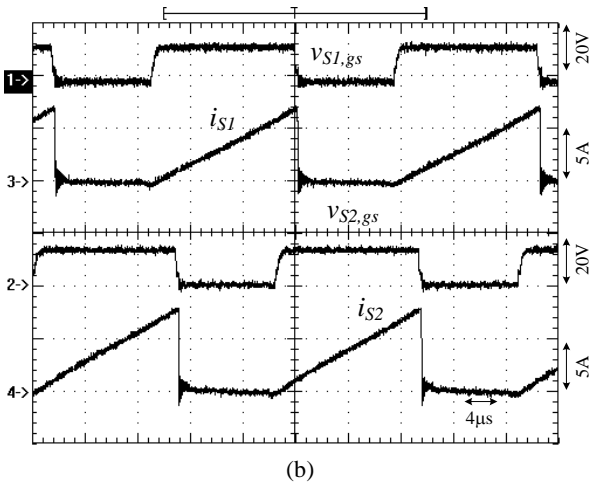
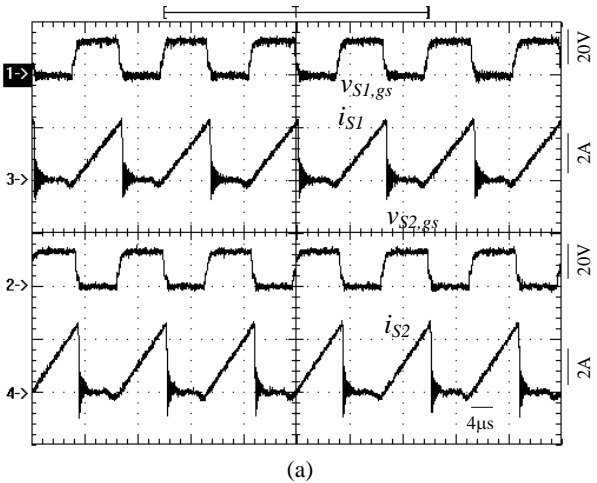
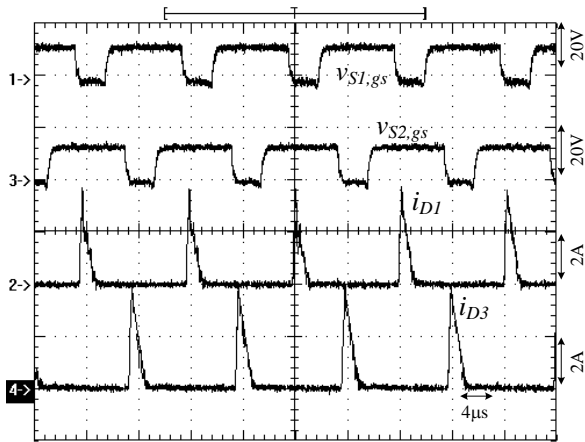
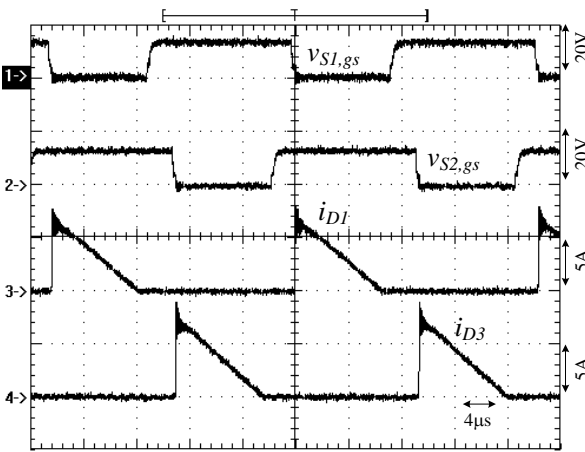


Fig. 8. Measured results of $v_{S1,gs}$, $v_{S2,gs}$, i_{S1} and i_{S2} at (a) 30% load (b) full load.

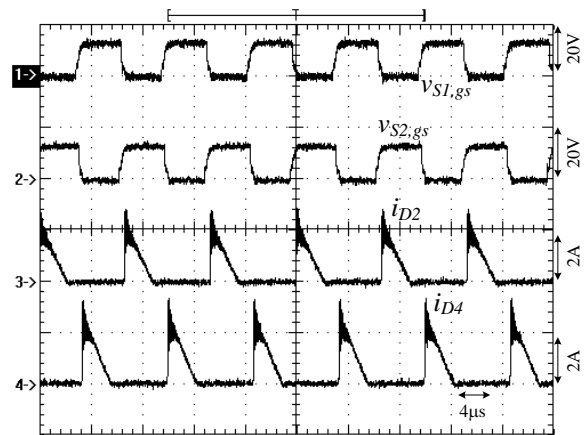


(a)

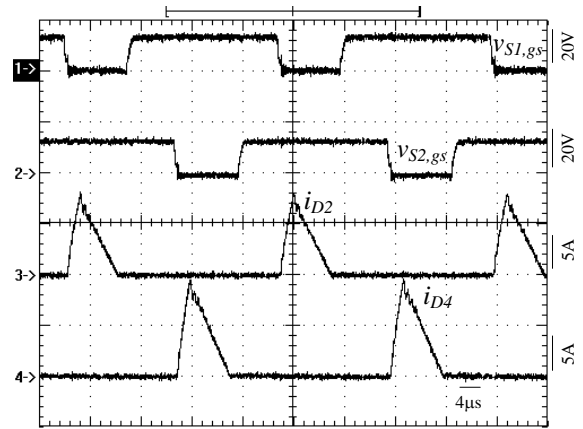


(b)

Fig. 9. Measured results of $v_{S1,gs}$, $v_{S2,gs}$, i_{D1} and i_{D3} at (a) 30% load (b) full load.



(a)



(b)

Fig. 10. Measured results of $v_{S1,gs}$, $v_{S2,gs}$, i_{D2} and i_{D4} at (a) 30% load (b) full load.

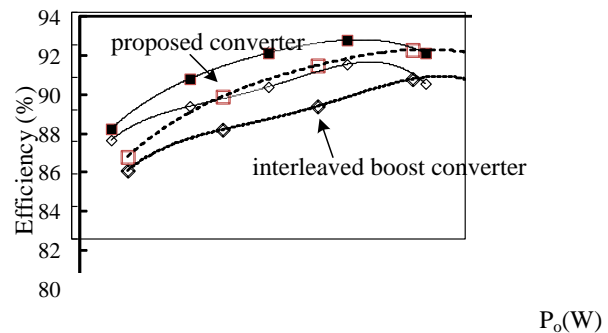


Fig. 11/ Measured circuit efficiencies of the proposed converter and interleaved boost converter with BCM operation.

VI. CONCLUSION

An interleaved boost-flyback converter operated in BCM mode is presented to achieve nearly unity power factor, low total harmonic distortion and high voltage step-up features. All diodes are turned off at ZCS and switches are turned on at ZCS. There is no reverse recovery loss on the rectifier diodes and the low cost fast recovery diodes can be used in the adopted circuit. The adopted converter can be used in fuel cell system, PV cell system, battery discharge system for DC-AC converter with high voltage step-up function. The adopted converter can also be used for high output voltage application with utility mains input and high input power factor demanded. The circuit configuration, operation principle and steady state analysis are demonstrated as well. Finally the performance of the proposed converter is verified from the experiments based on a laboratory prototype.

ACKNOWLEDGMENT

This paper is supported by the National Science Council of Taiwan under Grant NSC 99-2221-E-224-083-MY2.

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