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Effects of Imperfect Sinusoidal Input Currents on the Performance of a Boost PFC Pre-Regulator

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Abstract

This paper investigates the effects of applying different input current waveshapes on the performance of a continuous-conduction-mode (CCM) power-factor-correction (PFC) boost pre-regulator. It is found that the output voltage ripple of the pre-regulator can be reduced if the input current is modified to include controlled amount of higher order harmonics. This finding allows us to balance the performance of output regulation and the harmonic current emission when coming to the design of the pre-regulator. An experimental PFC boost pre-regulator prototype is constructed to verify the analysis and show the benefit of the pre-regulator operating with input current containing higher order harmonics.

Key words: Average current-mode control, Boost converter, Continuous-conduction-mode (CCM), Harmonic distortion, Load transient, Power factor correction

I. INTRODUCTION

Power factor correction has become a mandatory design criterion for switching mode power supplies. Boost type power-factor-correction (PFC) pre-regulators have become the most widely used power converters to achieve power factor correction [1]-[5]. To maintain a very low harmonic current distortion, the input current of PFC pre-regulators is generally controlled to be sinusoidal and in phase with the input voltage. The consequence is that the output voltage of PFC pre-regulators inevitably contains a second-harmonic (100 Hz or 120 Hz) voltage ripple [6], [7], and that the dynamic response of the pre-regulator becomes sluggish due to the placement of a very low frequency pole in the output voltage control loop [8], [9]. However, most international standards of harmonic current emissions limits, such as IEC 61000-3-2 [10], do allow a small amount of input current harmonics, and it is therefore unnecessary to achieve perfect sinusoidal input current. Some helpful hints to select a PFC solution for single-phase PFC switching regulators that meet the IEC 61000-3-2 standard have been provided by Fernández *et al.* [11]. A survey on the design cost and quality of input current of PFC switching regulators has been reported by García *et al.* [12]. It has been shown in [13]-[15] that pre-regulators drawing imperfect sinusoidal input current can effectively reduce the second harmonic output ripple voltage without increasing their output capacitor. This reduced output ripple voltage arrangement can lead to more stable operation of the pre-regulators [16] and provide possibility of expanding the gain of the output voltage control loop for enhancing the static output voltage regulation. However, in these papers, the relationship between the output ripple voltage and the dynamic characteristics of a pre-regulator drawing imperfect sinusoidal input current has not been fully investigated or reported. It is felt that a systematic design procedure is necessary so that their relationship can be fully exploited. Understanding this relationship not only benefits the design of pre-regulators but also the design of some specific applications of non-cascading PFC switching regulators that require high conversion efficiency [17]-[19].

In this paper, we will study these relationships for a boost CCM PFC pre-regulator that is operated under average

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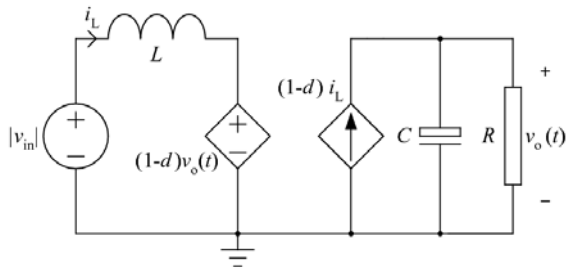


Fig. 1. State-space model for CCM boost converter.

current mode control. We will also present different design issues that can be used to optimize power factor, value of output capacitor, and dynamic response of the pre-regulator under imperfect sinusoidal input current conditions. The rest of the paper is organized as follows. In Section II, the CCM boost converter as employed in typical PFC applications is modeled by using time-scale separations [20]. Based on this model, two descriptions of the CCM boost PFC pre-regulator are presented. One addresses the relationship between the output voltage and the different waveshapes of the input current, and the other focuses on the dynamic behavior of the output voltage. Section III verifies the derived model by PSPICE simulation and presents the salient findings. Finally, Section IV presents the design of an experimental prototype and verification by experimental results.

II. Analysis of CCM Boost PFC Pre-regulator

A. Derivation of Output Voltage Ripple of CCM Boost PFC Pre-Regulator

The CCM boost converter is the most popular topology for PFC pre-regulators [3]. Non-pulsating input current and low current stress in semiconductor devices are the advantages of using the CCM boost converter as a PFC pre-regulator. For brevity and without confusion, we simply refer the CCM boost PFC pre-regulator to as the *pre-regulator*. Fig. 1 shows a standard state-space model for the pre-regulator [21] and the

$$\frac{dv_o}{dt}=\frac{1}{C}\left[i_L(1-d)-\frac{v_o}{R}\right] \tag{1}$$

$$\frac{di_L}{dt}=\frac{1}{L}\left[|v_{in}|-v_o(1-d)\right] \tag{2}$$

where d is the duty cycle, v_o is the output voltage, i_L is the inductor current, C is the output capacitance, and L is the inductance.

We consider the single-phase power conversion application here. The input voltage v_{in} and the input current i_{in} of the pre-regulator are taken as ideal sinusoids. Assuming that the inductor current is controlled to follow closely the rectified sinusoidal input voltage, the following equations describe the input voltage, input current, and inductor current waveforms.

$$v_{in}=V\sin\omega t$$
$$i_{in}=I_1\sin\omega t$$
$$i_L=I_1|\sin\omega t|$$

where V is the peak input voltage, I_1 is the peak value of the fundamental input current, and ω is the angular frequency of the ac mains. Inserting $i_L=I_1|\sin\omega t|$ to (2), and using the result to eliminate $(1-d)$ from (1) gives

$$\frac{dv_o}{dt}=\frac{VI_1(1-\cos 2\omega t)}{2v_oC}-\frac{\omega LI_1^2|\sin 2\omega t|}{2v_oC}-\frac{v_o}{RC} \tag{3}$$

Comparing the magnitudes of the three terms on the right-hand side of (3), since $V>>\omega LI_1$, the overall converter's dynamic response is mainly governed by the first and the third term. Hence, (3) can be simplified to (4) with a small error involved[1]. The same equation can be obtained by applying singular perturbation theory to (1) and (2) as had been demonstrated by Wall and Jackson [22] for boost PFC systems.

$$2v_o\frac{dv_o}{dt}\approx\frac{VI_1}{C}(1-\cos 2\omega t)-\frac{2v_o^2}{RC} \tag{4}$$

We denote the nonlinear term v_o^2 as variable x, and (4) is rewritten as

$$\frac{dx}{dt}+\frac{2x}{RC}=\frac{VI_1}{C}(1-\cos 2\omega t) \tag{5}$$

The general solution of $x(t)$ is

$$x(t)=e^{\frac{-2t}{RC}}\left[\int e^{\frac{2t}{RC}}\frac{VI_1}{C}(1-\cos 2\omega t)\,dt\right]$$
$$=\frac{VI_1}{C}Ae^{\frac{-2t}{RC}}+\frac{VI_1R}{2}\left(1-\frac{\cos 2\omega t+\omega RC\sin 2\omega t}{1+(\omega RC)^2}\right)$$

where A is a constant depending on the initial condition. The general solution of $v_o(t)$ is given by

$$v_o(t)=\sqrt{\frac{VI_1}{C}Ae^{\frac{-2t}{RC}}+\frac{VI_1R}{2}\left(1-\frac{\cos 2\omega t+\omega RC\sin 2\omega t}{1+(\omega RC)^2}\right)} \tag{6}$$

For $v_o(0)=0$, A is given by

$$A=-\frac{RC}{2}\left(1-\frac{1}{1+(\omega RC)^2}\right) \tag{7}$$

The first term of (6) will vanish when $t\geq RC/2$, hence $v_o(t)$ can be further simplified as

[1] In the boost PFC circuit proposed in this paper, $V=220\sqrt{2}$ V, $L=1$ mH and $I_1=\frac{2P_o(=200\text{ W})}{V}=1.3$ A, therefore the approximation of (3) by (4) with a small error involved is justified.

$$v_o(t)=\sqrt{\frac{VI_1R}{2}\left(1-\frac{\sin(2\omega t+\phi)}{1+(\omega RC)^2}\right)} \tag{8}$$

where ϕ is equal to $\arctan(1/\omega RC)$ and represents the time delay generated by the output capacitor C and the load resistor R.

As mentioned earlier, international standards for harmonic current emissions, such as IEC 61000-3-2 [10], allows a certain amount of harmonic current to be drawn to the input of the pre-regulator. Possible tradeoff between the input current waveform and the output capacitor size of the pre-regulator has been studied in [13]-[15]. In this paper, an analytical solution for the output voltage ripple of the pre-regulator drawing imperfect sinusoidal input current is provided to predict the relationship between the imperfect sinusoidal input current and the output voltage ripple level. Since only odd harmonic current components contribute to reduce the output voltage ripple of the pre-regulator, we consider imperfect sinusoidal input current of the following form:

$$i_{L_{HD}}=\left|I_1\left(\sin\omega t+\sum_{n=1}^{\infty}\beta_{2n+1}\sin(2n+1)\omega t\right)\right| \tag{9}$$

where β_{2n+1} is the peak amplitude ratio of the odd harmonic current to the fundamental current; and 2n + 1 denotes the harmonic order. To simplify the calculation, we consider only the third, fifth and seventh harmonic current components of the output voltage ripple. Combining (9) with (3), we obtain the output voltage of the pre-regulator drawing imperfect sinusoidal input current as

$$\begin{aligned}\frac{dx_{HD}}{dt}+\frac{2x_{HD}}{RC}=\frac{VI_1}{C}(&1-\cos2\omega t+\beta_3\cos2\omega t\\&-\beta_3\cos4\omega t+\beta_5\cos4\omega t\\&-\beta_5\cos6\omega t+\beta_7\cos6\omega t\\&-\beta_7\cos8\omega t)\end{aligned} \tag{10}$$

The steady-state solution of the output voltage of the pre-regulator drawing imperfect sinusoidal input current is given by

$$\begin{aligned}v_{oHD}(t)=\Bigg[\frac{VI_1R}{2}\Bigg(&1-(1-\beta_3)\frac{\sin(2\omega t+\phi_1)}{\sqrt{1+(\omega RC)^2}}\\&-(\beta_3-\beta_5)\frac{\sin(4\omega t+\phi_2)}{\sqrt{1+(2\omega RC)^2}}\\&-(\beta_5-\beta_7)\frac{\sin(6\omega t+\phi_3)}{\sqrt{1+(3\omega RC)^2}}\\&-\beta_7\frac{\sin(8\omega t+\phi_4)}{\sqrt{1+(4\omega RC)^2}}\Bigg)\Bigg]^{\frac{1}{2}}\end{aligned} \tag{11}$$

where Φ_1, Φ_2, Φ_3, and Φ_4 are equal to $\arctan(1/\omega RC)$, $\arctan(1/2\omega RC)$, $\arctan(1/3\omega RC)$, and $\arctan(1/4\omega RC)$, respectively. A detailed comparison of the output voltage ripple of the pre-regulator drawing sinusoidal input current and that drawing imperfect sinusoidal input current will be shown in Section III.

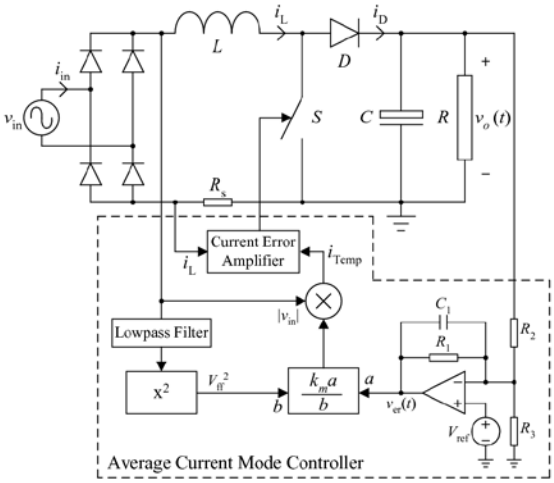


Fig. 2. CCM boost converter under average current-mode control.

B. Derivation of Output Voltage Dynamics of CCM Boost PFC Pre-Regulator

In this subsection, we study the output voltage dynamics of the pre-regulator under average current-mode control by using the circuit shown in Fig. 2 [1]. The inductor current i_L is programmed by the current template signal i_{Temp} to follow the rectified input voltage. Here, i_{Temp} is generated by an analog multiplier that multiplies the rectified input voltage by the voltage error amplifier output $v_{er}(t)$.

Thus, $v_{er}(t)$ effectively adjusts the inductor current to control the amplitude of i_{Temp}. Assume that i_L is driven by the current error amplifier to follow i_{Temp} accurately. From Fig. 2, i_L is generated by the multiplier with three inputs, i.e.,

$$i_L=\frac{k_m v_{er}(t)|v_{in}|}{V_{ff}^2}=\frac{k_m v_{er}(t)V|\sin\omega t|}{\left(V/\sqrt{2}\right)^2} \tag{12}$$

where V_{ff} is generated by a low-pass filter and represents the root-means-square value of the ac mains voltage; V_{ff}^2 is a feedforward signal for compensating the disturbances in the ac mains input voltage; $|v_{in}|$ provides the waveshape such that i_L synchronizes with the rectified input voltage; and k_m represents the gain of the analog multiplier. In some commercially available PFC average current-mode control ICs, such as UC3854 and ML4824, k_m is pre-determined by the pre-regulator design and is chosen as $V/2$ in this paper. Therefore, i_L corresponds to

$$i_L=v_{er}(t)|\sin\omega t| \tag{13}$$

where $v_{er}(t)$ is continually adjusted by a voltage error amplifier to maintain the desired output voltage. Obviously, to maintain i_L as a rectified sinusoid, a low-pass type

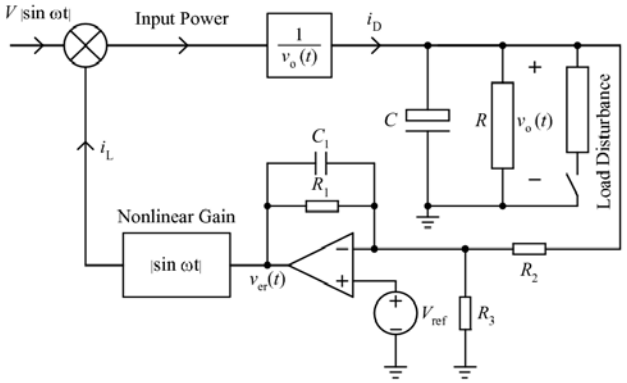


Fig. 3. Simplified block diagram for evaluating the load transient response of the average current-mode controlled pre-regulator.

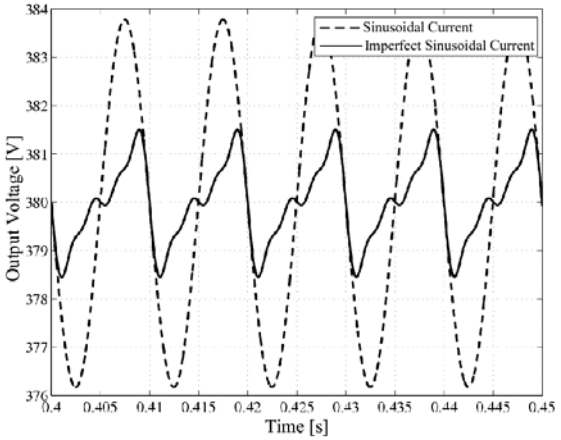


Fig. 4. Output voltages by a sinusoidal input current and an imperfect sinusoidal input current obtained from (8) and (11).

feedback circuit is used to generate a nearly fixed $v_{er}(t)$. Referring to Fig. 2, the control equation for $v_{er}(t)$ is given by

$$\tau \frac{dv_{er}(t)}{dt} + v_{er}(t) = -G(v_o - V_{ref}) + \left(\frac{R_1}{R_3} + 1\right)V_{ref} \qquad (14)$$

where V_{ref} is the reference voltage from the average current mode controller, $\tau = R_1C_1$ is the time constant of the feedback circuit, and $G = R_1/R_2$ is the dc gain of the feedback circuit. By substituting (13) into (1), the closed loop output voltage dynamics of the pre-regulator drawing a sinusoidal input

current can be expressed as

$$2v_o\frac{dv_o}{dt} + \frac{2v_o^2}{RC} = \frac{Vv_{er}(t)}{C}(1-\cos 2\omega t) \qquad (15)$$

Now, (14) and (15) fully describe the closed-loop output voltage dynamics of the pre-regulator drawing a sinusoidal input current under average current-mode control. Fig. 3 shows a simplified block diagram based on (14) and (15). For the case of imperfect sinusoidal input current, the function $|\sin\omega t|$ in the nonlinear gain block can be replaced by $\left|\left(\sin\omega t + \sum_{n=1}^{\infty}\beta_{2n+1}\sin(2n+1)\omega t\right)\right|$. Since the system is nonlinear and subject to large variation in the input voltage, the usual averaging and linearization analysis [23] is not capable of capturing the dynamical behavior accurately. A numerical approach is employed to solve (14) and (15) for identifying the output voltage dynamics of the pre-regulator, as elaborated in the next section.

III. Effects of Imperfect Sinusoidal Input Current on Output Voltage Ripple and Voltage Dynamics

The foregoing derivations are based on a set of nonlinear

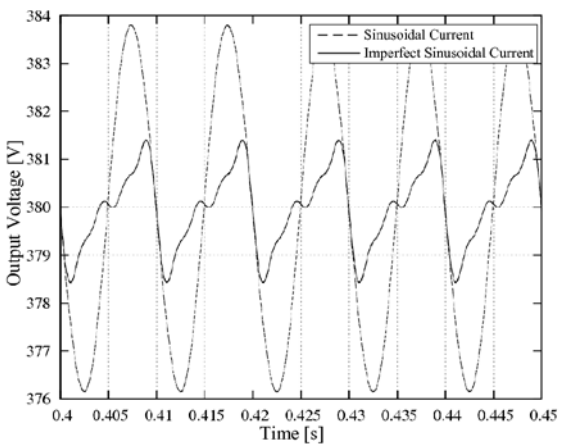


Fig.5. Output voltages by a sinusoidal input current and an imperfect sinusoidal input current obtained by PSCIPE simulations.

differential equations that are derived from the standard state-space boost converter model. The derived analytical models cannot predict the details of the pre-regulator, especially for frequency range close to the switching frequency. In this section, we will first verify the derivations by PSPICE for a boost converter controlled by an average current-mode controller UC3854. The analytical models are then used in PSPICE to evaluate the behavior of the actual circuit. Subsequently, the effects of imperfect sinusoidal input current on the voltage ripple and voltage dynamics of the pre-regulator are identified by PSPICE simulations. To visualize the effects of imperfect sinusoidal input current on the output voltage ripple and dynamics of the pre-regulator, we set the input current to including harmonic components at the maximum allowable levels defined by the IEC 61000-3-2 Class D standard and the ratios between the first three odd harmonic current amplitudes and the fundamental current amplitude as

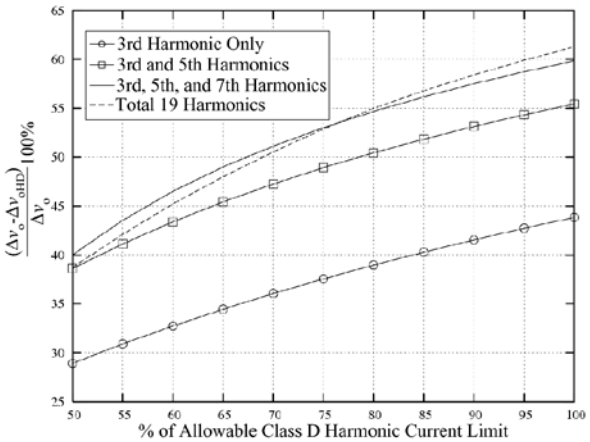


Fig. 6. Numerical relationships between the percentage reduction of voltage ripple and different current harmonics at 200W output power for vin=220 Vrms, Vo=380 V, C=440 μF, and Δvo=3.8 V.

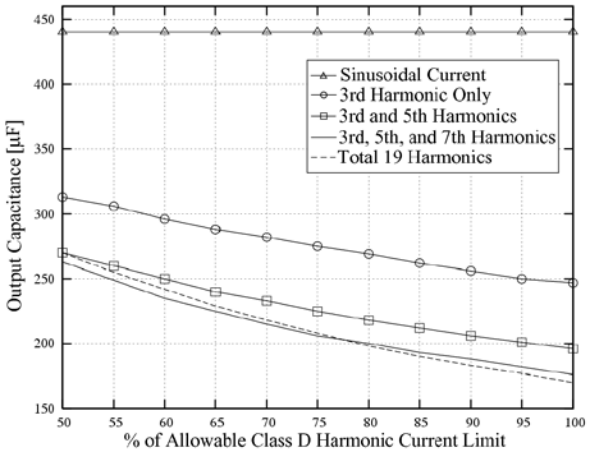


Fig. 7. Numerical relationships between the output capacitance and different current harmonics at 200W output power for vin=220 Vrms, Vo=380 V, and Δvo=3.8 V.

$$\beta_3 = \frac{V}{\sqrt{2}} 3.4 \times 10^{-3}$$
$$\beta_5 = \frac{V}{\sqrt{2}} 1.9 \times 10^{-3} \qquad (16)$$
$$\beta_7 = \frac{V}{\sqrt{2}} 1.0 \times 10^{-3}$$

The output voltages are then calculated by (11) and the results are shown in Fig. 4 along with those obtained by (8) for a sinusoidal input current. As shown, the results are closely matched to those obtained by PSPICE simulations in Fig. 5. It is interesting to see that, for the same values of output capacitor, output voltage, and output power, the pre-regulator drawing imperfect sinusoidal input current

gives smaller output voltage ripple (with a reduction of about 60%). The percentage reduction in voltage ripple by imperfect sinusoidal input currents can be calculated according to (11) for different levels of current harmonics by

$$\%\ \text{reduction of}\ \Delta v_o = \frac{\Delta v_o - \Delta v_{oHD}}{\Delta v_o} \times 100\% \qquad (17)$$

where Δv_o is the peak-to-peak output voltage ripple for a sinusoidal input current and Δv_{oHD} is the peak-to-peak output voltage ripple for an imperfect sinusoidal input current. Fig. 6 shows the relationship between the percentage reduction in the peak-to-peak output voltage ripple and the level of harmonic current injected into the inductor current, where the harmonic current level is expressed as the percentage of allowable Class D harmonic current limit. The harmonic current levels (β_3, β_5, β_7, etc.) are inserted into (11) and the corresponding output voltage waveform is generated and the output voltage ripple measured. It can be seen that, in general, the percentage reduction in the output voltage ripple increases as the number of harmonics increases and their levels

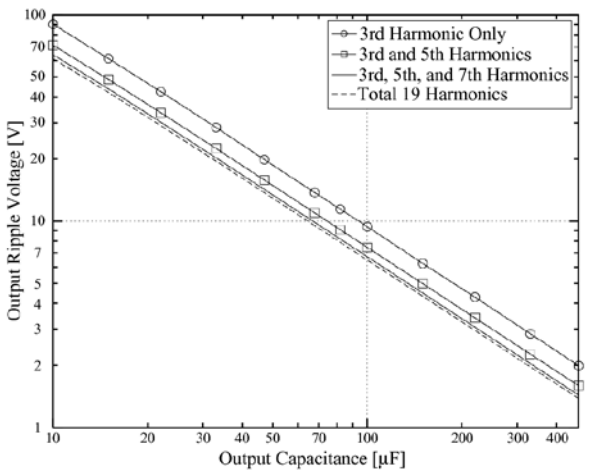


Fig. 8. Numerical relationships between the peak-to-peak output voltage ripple and output capacitance for different maximum harmonic current limits at 200W output power for vin=220 Vrms and Vo=380 V.

increase towards the allowable limits. At the maximum allowed total harmonic current contents, i.e., total of 19 harmonic components, the output voltage ripple reduces by 61.3 %. Fig. 7 shows the relationship between the required output capacitance for achieving $\Delta v_o = 3.8$ V and the level of harmonic current injected into the inductor current, where the harmonic current level is expressed as the percentage of allowable Class D harmonic current limit. The curves are generated by inserting various pre-determined harmonic current levels (β_3, β_5, β_7, etc.) into (11) and finding the corresponding output capacitances required for achieving $\Delta v_o = 3.8$ V. It can be seen that smaller output capacitances are required to keep the same output voltage ripple as the number of harmonics increases and their levels increase towards the allowable limits. For example, for v_{in} =

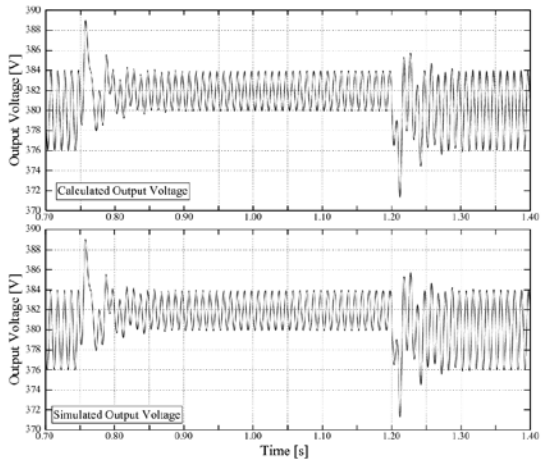


Fig. 9. Output voltage waveforms for sinusoidal input current for load stepping between 200W and 100W for verification of (14) and (15).

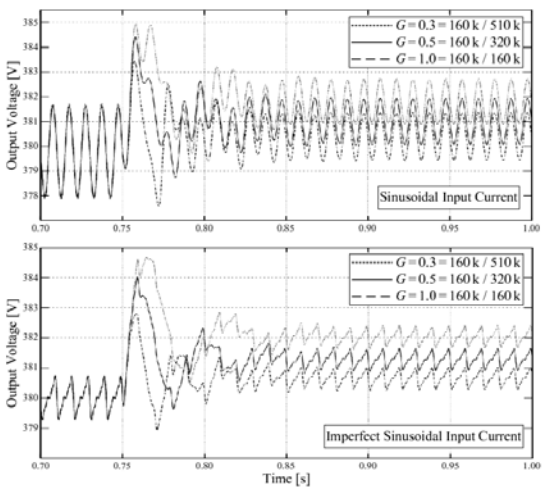


Fig. 10. Output voltage waveforms to illustrate the effect of G with C fixed at 470μF and output power stepping between 200W and 100W.

220 V_{rms}, V_o = 380 V, and Δv_o = 3.8 V, according to (8), the value of the output capacitance for a sinusoidal input current is required to be 440 μF at P_o = 200 W. However, the value of the output capacitance for an imperfect sinusoidal input current is significantly reduced to 176 μF under the same condition. Fig. 8 shows the relationship between the output voltage ripple and the output capacitance for v_{in} = 220 V_{rms}, V_o = 380 V, and P_o = 200 W. For these calculations, the harmonic current levels are set as the maximum allowable limits by the IEC 61000-3-2 Class D standard. As expected, for the same output capacitance, the output voltage ripple decreases as the number of harmonics increases.

As studied in Section II-B, two nonlinear differential equations have been derived to describe the output voltage dynamics of the pre-regulator. A comparison is made between the results obtained by (14) and (15) and those by PSPICE simulation under a load transient condition. Fig. 9 reveals that the two results are closely matched for a load stepping between 100 W and 200 W. The output voltage dynamics are further investigated under the influence of different dc gains (G) of the feedback circuit and different RC time constants of the output circuit for a sinusoidal input current and an imperfect sinusoidal input current, respectively. In both cases, we keep the time constant τ of the feedback circuit five times longer than the ac mains cycle in order to maintain a low input current distortion [1], [2], [7]-[9]. Fig. 10 shows the output voltage waveforms for different values of G with the output capacitance fixed at 470 μF and output power stepping from 200 W to 100 W. It can be seen that the output voltage ripple for the case of imperfect sinusoidal input current is relatively smaller compared to the case of sinusoidal input current. It also shows that increasing G generally improves the static output voltage regulation for both types of input current. Nevertheless, increasing G also causes extra input current harmonics [7] and can lead to instability problem in the pre-regulator [16]. These problems become more severe for the sinusoidal input current. For the case of imperfect sinusoidal input current, the effects of G and C are further illustrated by Fig. 11. In general, the settling time decreases with increasing G and decreasing C, whereas the voltage undershoot decreases with increasing both C and G.

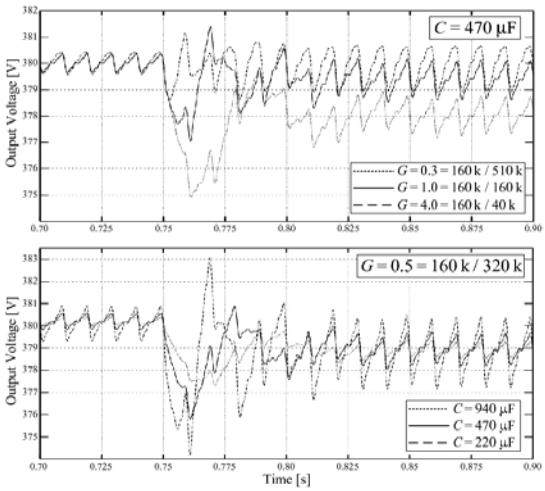


Fig. 11. Output voltage waveforms for imperfect sinusoidal input current to show the effect of G (upper figure) and the effect of C (lower figure). Output power is stepped from 100W to 200W.

IV. EXPERIMENTAL VERIFICATION

To verify the theoretical analysis discussed in the previous sections, a prototype boost PFC pre-regulator is designed to meet the following design specifications: the input voltage is 220 V_{rms}, the ac mains frequency is 50 Hz, the output voltage is 380 V, the maximum output power is 200 W, and the input current is imperfect sinusoidal satisfying the IEC 61000-3-2

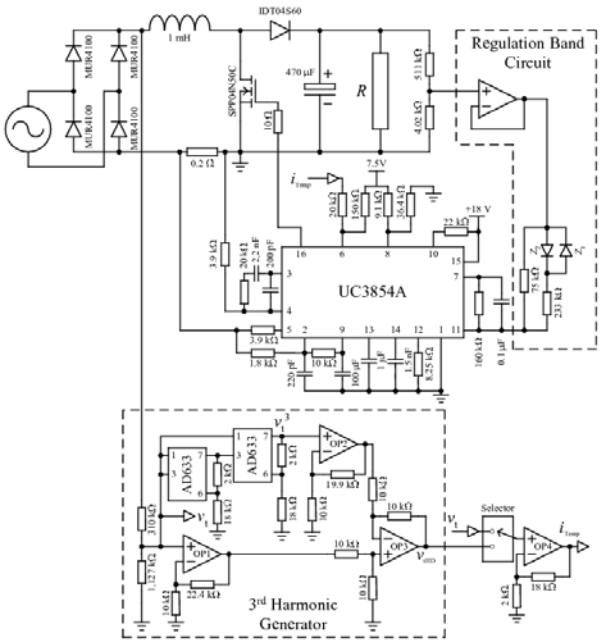


Fig. 12. Full schematic diagram of the proposed single-converter PFC power supply including third harmonic generator.

Class D standard. Fig. 12 shows the schematic diagram of the prototype with a third harmonic generator [15] and the regulation band circuit for achieving a fast dynamic response. The average current-mode controller UC3854 is employed to provide PFC function. The voltage template (equivalent to i_{Temp}) for shaping the inductor current is synthesized by the third harmonic generator. The third harmonic generator is constructed from two analog multipliers and a few operational amplifiers. The input current drawn by the prototype is described by

$$i_{\text{LHD}} = \left| I_1 \left(\sin \omega t + 0.748 \sin 3\omega t \right) \right| \tag{18}$$

where I_1 is controlled by the output voltage of the voltage error amplifier. Therefore, the voltage template for the imperfect sinusoidal input current is

$$v_{\text{tHD}} = \left| \left(3.244 \sin \omega t - 2.992 \sin^3 \omega t \right) \right| \tag{19}$$

The operational amplifiers provide the voltage gains and subtraction function required for synthesizing v_{tHD}. The voltage gain of OP1 and OP2 is set to 3.244 and 2.992, respectively. OP3 provides the subtraction function. OP4 provides a voltage gain of 10 for satisfying the signal requirement of UC3854. The effect of the input current with third harmonic on the output voltage ripple is examined.

Fig. 13 shows the experimental waveforms at full-load condition when i_{Temp} takes the waveshape of the rectified input voltage. The measured output voltage ripple (peak-to-peak) is about 7.5 V. Fig. 14 shows the experimental waveforms at full-load condition when i_{Temp} is synthesized by the third harmonic generator. The measured output voltage ripple (peak-to-peak) is about 4.6 V. It can be seen that the input current with third harmonic can effectively reduce the

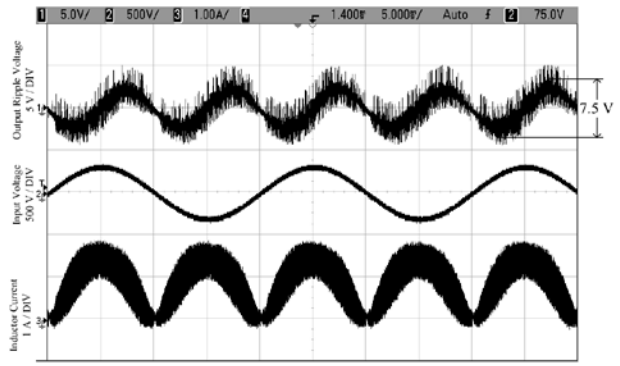


Fig. 13. Measured waveforms at full-load condition with the rectified input voltage as the inductor current reference: output voltage ripple (upper trace), input voltage (middle trace), and inductor current (lower trace). Time =5ms/div.

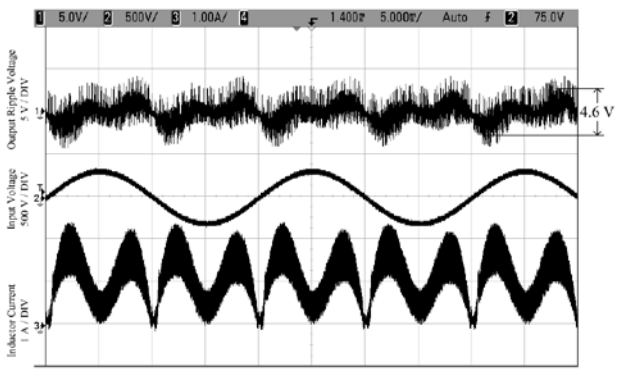


Fig. 14. Measured waveforms at full-load condition with the 3rd harmonic i_{Temp} as the inductor current reference: output voltage ripple (upper trace), input voltage (middle trace), and inductor current (lower trace). Time =5ms/div.

output voltage ripple. This can be explained by comparing the inductor current waveforms shown in Figs. 13 and 14. For the same average input current, the presence of higher harmonics causes the modified inductor current waveform in Fig. 14 to be significantly attenuated in the middle and broadened on the edges. The output capacitor is forced to undergo two charge/discharge cycles (compared to only one in the case depicted in Fig. 13) per input voltage's half cycle. The charge/discharge action of the output capacitor at doubled frequency causes the amplitude of the output voltage ripple (in response to inductor current's variation) to be more effectively damped by the output capacitor.

A XiTRON 2551 single-phase general purpose power analyzer is used to measure the total harmonic distortion. Fig. 15 shows the measured harmonic contents for both cases of i_{Temp} at full-load condition. A comparison is made between the harmonic components present in the input current and the limits of the IEC 61000-3-2 Class D standard for both cases of i_{Temp} under full-load (200 W) condition. Based on the measurement results, the amplitudes of all harmonic components are below the limits of the IEC 61000-3-2 Class D standard.

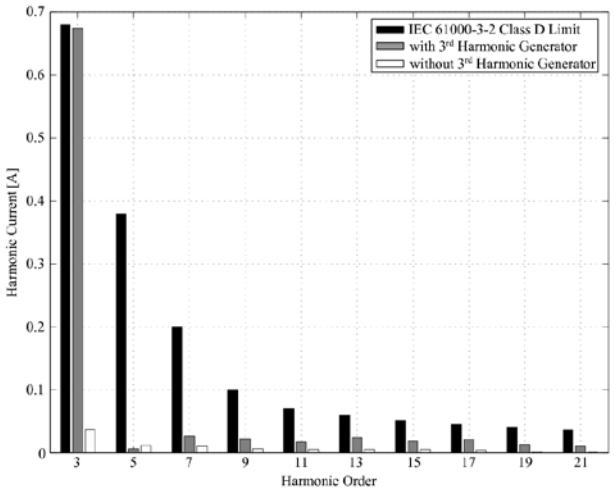


Fig. 15. Measured harmonic current amplitudes for the two cases of i_{Temp}.

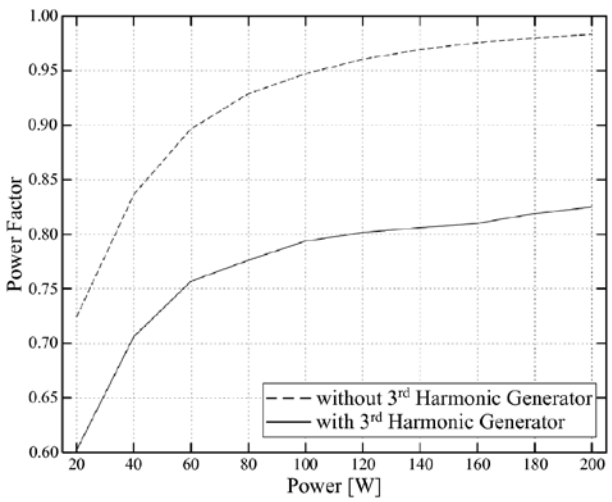


Fig. 16. Power factor versus output power for the two cases of i_{Temp}.

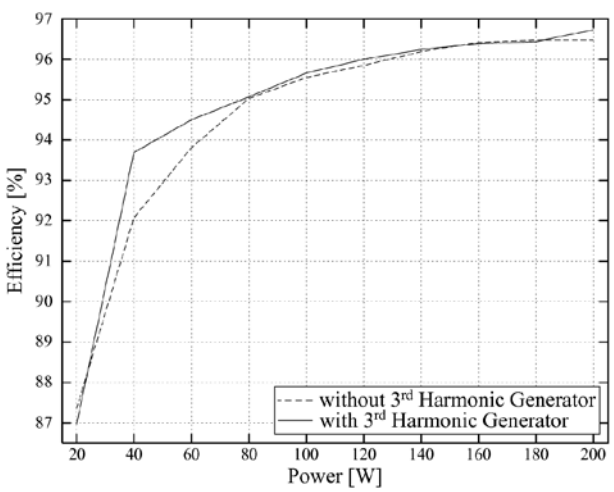
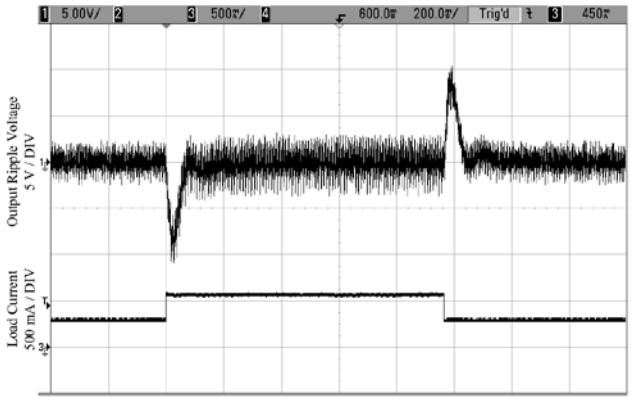
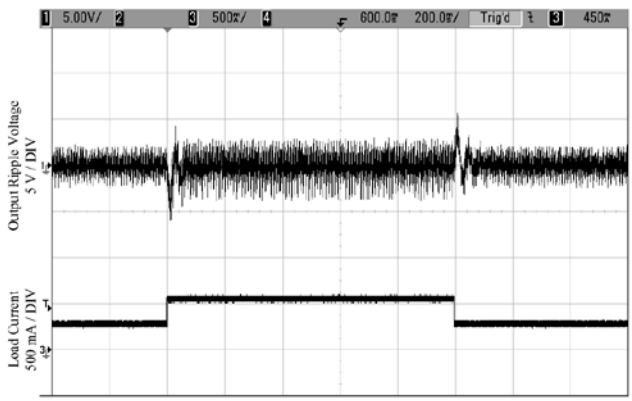


Fig. 17. Efficiency versus output power for the two cases of i_{Temp}.



(a)



(b)

Fig. 18. Measured output voltage ripple (upper trace) and load current (lower trace): (a) without regulation band circuit and (b) with regulation band circuit. Time scale =200 ms/div.

Fig. 16 shows the measured power factor for the two cases of i_{Temp}. When read together with Figs. 13 and 14, it is clear that smaller output voltage ripple is achieved in the case of i_{Temp} with third harmonic at the expense of a poorer input power factor. Fig. 17 shows the measured power efficiency of the prototype over a range of 20 W to 200 W. The measured full-load efficiency is 96.7% and it is similar for both cases of i_{Temp} under study. The dynamic response of the pre-regulator with and without the regulation band circuit is also tested by imposing a load stepping between 100 W and 200 W. Fig. 18 shows that the settling time, voltage overshoot and voltage undershoot are reduced by using a larger dc gain realized by the regulation band circuit.

In applications where a moderately fast output voltage's dynamic response is adequate [7], [9], [24], [25], the proposed prototype drawing an imperfect sinusoidal input current can be an all-in-one power supply solution that provides PFC, low output voltage ripple, and adequately fast dynamic response.

V. CONCLUSIONS

This paper provides a detailed analysis of the output voltage ripple characteristic and dynamic response of a boost PFC pre-regulator that draws an imperfect sinusoidal input current. The equation describing the output voltage ripple behavior under an imperfect sinusoidal input current is derived and verified against PSPICE simulations. A prototype including third harmonic generator and regulation band circuit is constructed to verify the effects of imperfect sinusoidal input current on the performance of a boost PFC pre-regulator. Experimental results show that the output voltage ripple of the prototype can be reduced by drawing an imperfect sinusoidal input current, and the dynamic response of the pre-regulator can be improved by using a larger dc gain realized by the regulation band circuit.

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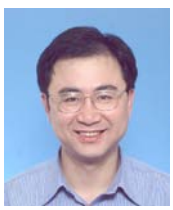

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