ADCL 버퍼를 이용한 단열 논리회로용 AC 전원과 동기화된 저전력 클럭 발생기 설계

조승일* · 김성권** · 하라다 토모치카* · 요코야마 미치오*

Design of Low-power Clock Generator Synchronized with the AC Power Source Using the ADCL Buffer for Adiabatic Logics

Seung-Il Cho* · Seong-Kweon Kim** · Tomochika Harada* · Michio Yokoyama*

요 약

본 논문에서는 ADCL(adiabatic dynamic CMOS logic) buffer를 이용한 단열 논리회로용 AC 전원과 동기화된 저전력 클럭 발생기를 제안한다. CMOS 논리회로의 전력 손실을 줄이고 ADCL의 저전력 동작을 위해서, 논리회로의 clock 신호는 AC 전원 신호와 동기화 되어야 한다. 설계된 Schmitt trigger 회로와 ADCL buffer를 사용한 ADCL 주파수 분주기를 이용하여 AC 신호와 단열동작을 위한 clock 신호가 발생된다. 제안된 저전력 클럭 발생기의 소비전력은 3kHz와 10MHz에서 각각 1.181uW와 37.42uW으로 시뮬레이션에서 확인하였다.

ABSTRACT

In this paper, the low-power clock generator synchronized with the AC power signal using the adiabatic dynamic CMOS logic (ADCL) buffer is proposed for adiabatic logics. To reduce the power dissipation in conventional CMOS logic and to maintain adiabatic charging and discharging with low power for the ADCL, the clock signal of logic circuits should be synchronized with the AC power source. The clock signal for an adiabatic charging and discharging with the AC power signal was generated with the designed Schmitt trigger circuit and ADCL frequency divider using the ADCL buffer. From the simulation result, the power consumption of the proposed clock generator was estimated with approximately 1.181uW and 37.42uW at output 3kHz and 10MHz respectively.

키워드

synchronization, low-power clock generator, adiabatic dynamic CMOS logic(ADCL) buffer, Schmitt trigger circuit, frequency divider
동기화, 저전력 클럭 발생기, ADCL 버퍼, 슈미트트리거 회로, 주파수 분주기

Ⅰ. Introduction

Recently, the device dimension of transistors has been scaled toward the nanometer region to increase circuit performance and operating speed as well as to reduce the silicon cost with next generation of the large scale integrated circuits (LSI) technologies. The power supply voltage of

* Yamagata Univ. Graduate School of Science and Engineering(tye91221l@st.yamagata-u.ac.jp)
** 교신저자 : 서울과학기술대학교(kim12632@seoultech.ac.kr)
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chips in the nano-scale complementary metal-oxide semiconductor (CMOS) process has been also decreased for low-power consumption. Furthermore, a lot of studies have been performed in part of circuit design to implement complex functions of consumer products ; personal digital assistant (PDA), smart phone, and tablet PC, etc[1][2][3].

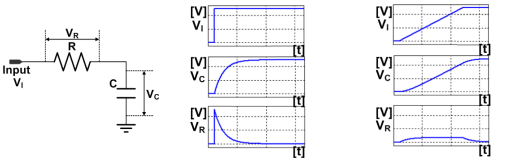
The adiabatic logics have been studied to reduce the power dissipation in conventional CMOS logic for low power design of logic circuits[4][5][6][7]. In particular, the adiabatic dynamic CMOS logic circuit (ADCL) achieves ultra low energy dissipation by restricting current to flow across devices with low voltage drop and by recycling the energy stored on their capacitors. It is known that output voltage of the ADCL gates is synchronized with the power supply voltage[8][9][10].

A synchronous circuit is needed for adiabatic charging when an alternate current (AC) power supply and a clock generator are respectively designed. The conventional phase locked loop (PLL) and delay lock loop (DLL) are used for the synchronization of each AC signal. However, the conventional PLL and DLL have a problem of large power consumption[11][12][13][14][15][16]. Hence, the power part which has both synchronization and low-power operation should be designed for the ADCL.

In this paper, low-power clock generator synchronized with the AC power signal is proposed using the ADCL buffer for the ADCL system. This clock generator using the designed Schmitt trigger circuit and novel ADCL frequency divider with the ADCL buffer is introduced.

II. Adiabatic logic

2.1 Adiabatic charging



(a) RC circuit (b) The DC signal (c) The adiabatic charging

Fig. 1 Operation of a RC circuit

During a sudden transition, between high and low level of input voltage, the load capacitor cannot be charged and discharged. The power dissipation is incurred by resistive component of logic circuit in the conventional CMOS logic circuits, because this logic circuit uses a constant voltage; the direct current(DC) power supply. In order to minimize the energy dissipation, adiabatic charging with the AC power is one of promising candidate techniques, which makes rising and falling time of input signals slower than charging and discharging time of the load capacitor [4][5][6].

Figure 1 shows the instance of operations of DC signal and adiabatic charging at the normal RC circuit. During an operation on the DC supply voltage, voltage waveforms are shown in Fig. 1(b). When voltage is changed from low to high level, the energy dissipation is incurred at the load R until the end of the charging at the load C.

In this case, the current $i(t)$, the voltage $v_R(t)$ of resistance and power dissipation $P_R(t)$ at Fig. 1(a) are expressed, respectively,

$$i(t)=\frac{V_I}{R}e^{-\frac{t}{CR}} \quad (1)$$

$$v_R(t)=V_I e^{-\frac{t}{CR}} \quad (2)$$

$$P_R(t)=\frac{V_I^2}{R}e^{-\frac{2t}{CR}} \quad (3)$$

On the other hand, Figure 1(c) shows another the voltage waveforms during an operation on the AC supply voltage that have slower rising time

than the time constant of RC circuit. The energy dissipation is reduced at the load R because most of the voltage is charged at the load C.

In this case, the current $i(t)$, the voltage $v_R(t)$ of resistance and power dissipation $P_R(t)$ at Fig.1(a) are calculated, respectively,

$$i(t)=\frac{CV_I}{\tau}\left[\left(1-e^{-\frac{t}{CR}}\right)-\left(1-e^{-\frac{t-\tau}{CR}}\right)u(t-\tau)\right] \quad (1)$$

$$v_R(t)=\frac{RCV_I}{\tau}\left[\left(1-e^{-\frac{t}{CR}}\right)-\left(1-e^{-\frac{t-\tau}{CR}}\right)u(t-\tau)\right] \quad (2)$$

$$P_R(t)=R\left[\frac{CV_I}{\tau}\left[\left(1-e^{-\frac{t}{CR}}\right)-\left(1-e^{-\frac{t-\tau}{CR}}\right)u(t-\tau)\right]\right]^2 \quad (3)$$

where τ is rising time of input and $u(t)$ is unit step function[4].

2.2 Adiabatic dynamic CMOS logic(ADCL)

The ADCL consists of the CMOS logic, AC power and two diodes for the adiabatic charging as it is applied to the CMOS logic[8][9][10]. An ADCL inverter gate is shown in Fig. 2(a). In this circuit, since the output voltage of the ADCL gate is synchronized with the power supply V_{phi}, the operating speed of the ADCL circuits is determined by the frequency of V_{phi}. The principle of ADCL inverter is shown in Fig. 2(b) and (c).

Principle(a) input : H → L

In Fig. 2(b), the pMOS and the nMOS are ON and OFF, respectively. In this case, the supply current path is generated and the load capacitor C is charged by V_{phi}.

Principle(b) input : L → H

In this condition, conversely, the pMOS and the nMOS are OFF and ON, respectively. It leads that the current path as shown in Fig. 2(c) is generated and the charge in C is redown into V_{phi}.

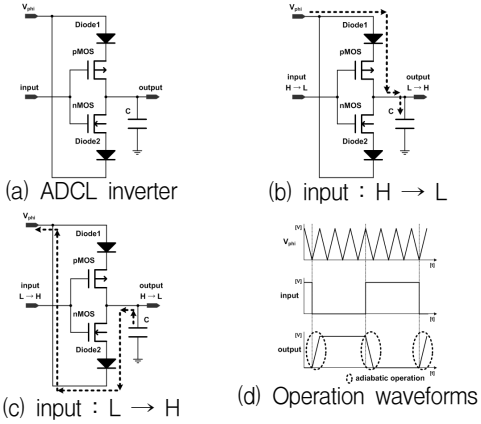


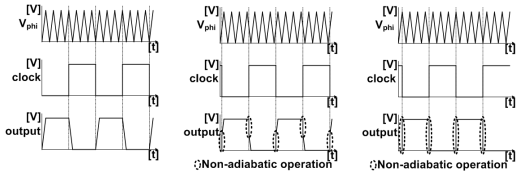
Fig. 2 ADCL inverter and operation waveforms

When the circuit is operated with the basis on Principles (a) and (b), this circuit functions as ADCL inverter. However, if the difference between V_{phi} and the voltage across C is large, adiabatic operation will not be established and power will be largely dissipated. Consequently, ADCL inverter works in the adiabatic mode as delineated in Fig 2(d).

The ADCL operates the adiabatic charging whenever logic level of the output is changed from high level to low and conversely and the charge can be reused because the charge reverts to the power source at discharging of load C. However, the output voltage is delayed by 0.5 peried per gate of V_{phi} in the ADCL circuit. Also, the AC power supply which can synchronize with the input signal(or clock signal) and reuse the charge is needed.

2.3 Adiabatic dynamic CMOS logic(ADCL)

The clock signal of ADCL should be synchronized with the AC power supply for adiabatic charging. Figure 3 shows the synchronized and unsynchronized waveforms. If the clock signal is unsynchronized with the AC power supply, non-adiabatic operation is realized at the



(a) Synchronized waveforms (phase diff. 180°) (b) Unsynchronized waveforms (phase diff. 270°) (c) Unsynchronized waveforms (phase diff. 0°)

Fig. 3 The relation of synchronization between AC power signal and clock signal

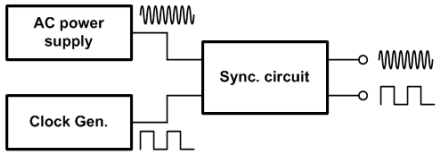


Fig. 4 The power source with a synchronizer

output. Therefore, a scheme of synchronous circuit for adiabatic charging is designed as shown in Fig. 4, when an AC power supply and a clock generator are used.

The conventional PLL and DLL are used for the synchronization of each AC signal. However, the power consumptions of PLL and DLL are very large; dozens of mW[14][15][16]. The power source which has both synchronization and low-power operation should be designed for the ADCL.

III. Design of low-power clock generator for ADCL system

In this section, low-power clock generator synchronized with the AC power signal was proposed using the ADCL buffer for the ADCL system. The minimum energy consumption in an ADCL is realized when the phase difference between the AC power supply and the input signal is 180°. In this case of synchronization, the adiabatic charging and low power can be achieved in the ADCL.

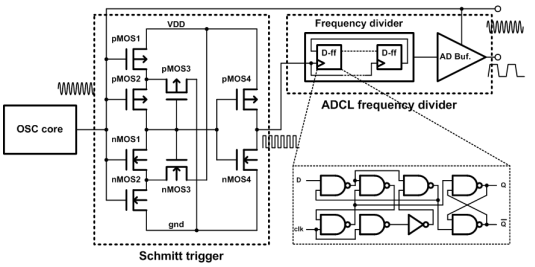
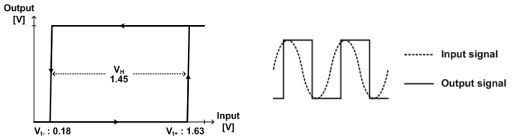


Fig. 5 Proposed low-power clock generator synchronized with the AC power signal for ADCL system



(a) Transfer characteristic (b) Waveforms of the Schmitt trigger circuit

Fig. 6 The designed Schmitt trigger circuit

Figure 5 shows the proposed low-power clock generator using the designed Schmitt trigger circuit and novel ADCL frequency divider for the ADCL system. This generator makes the AC power signal of OSC core output into the clock signal synchronized with the AC power signal. The low-power clock generator is designed using 174 MOS transistors.

3.1 Schmitt trigger circuit

The Schmitt trigger circuit is designed, which makes the AC power signal into clock signal and shifts phase of clock signal. Figure 6 shows operation, transfer characteristic, and input/output signals of designed Schmitt trigger circuit. When the input voltage is higher than the threshold voltage of V_{t+}; 1.63V, the output becomes high.

When the input is below a lower chosen threshold voltage of V_{t-}; 0.18V, the output is low.

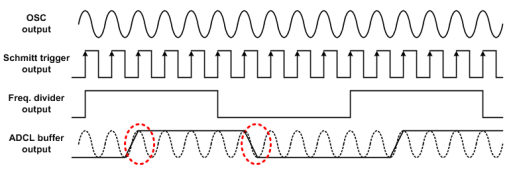


Fig. 7 Timing chart of the novel ADCL frequency divider

When the input is between V_{t+} and V_{t-}. the output retains its value. The hysteresis voltage, V_H ofdesigned Schmitt trigger is 1.45V for phase difference.

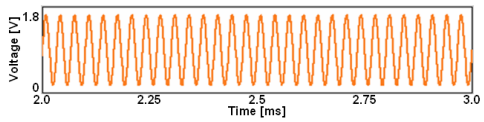
3.2 Novel ADCL frequency divider

In order to divide frequency and synchronize, the ADCL frequency divider is designed. Frequency ratio between the AC power signal and clock signal should be 'odd:1' for the ADCL. Therefore, output signal of the Schmitt trigger circuit should be a divide-by-odd. However, an odd-divider is usually very complex schematic and has large power consumption. Hence, we design novel ADCL frequency divider. The ADCL frequency divider consists of an even frequency divider and an ADCL buffer. Because of performance characteristics of the ADCL buffer, output signal of ADCL buffer is automatically synchronized with the OSC output, though output signal of the frequency divider is not synchronized with the OSC output. The designed ADCL frequency divider leads to simple structure and quite low-power operation. Figure 7 shows timing chart of designed ADCL frequency divider.

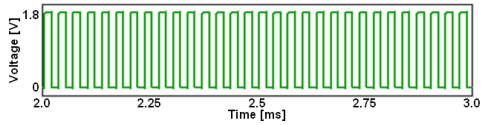
Ⅳ. The result of hspice simulation

The proposed low-power clock generator synchronized with the AC power signal using the ADCL buffer for the ADCL system has been simulated using a 0.18um standard CMOS technology and hspice. Figure 8 shows the result of simulation. The operations of designed Schmitt trigger circuit and ADCL frequency divider have been confirmed by simulation. The ADCL frequency divider operates adiabatic charging/discharging for low power(Fig. 8(c)). Furthermore, output signal of the designed clock generator synchronized with the OSC core output is confirmed for the ADCL in Fig. 8(d).

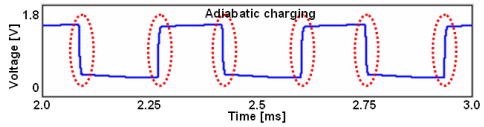
Table 1 summarizes power consumptions of propose the clock generator. As shown in table 1,



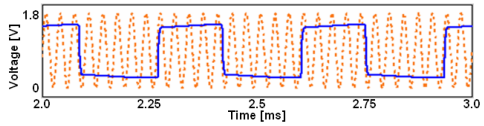
(a) Output waveform of the OSC core



(b) Output waveform of the designed Schmitt trigger



(c) Output waveform of designed novel ADCL frequency divider



(d) An overlap between (a) and (c)

Fig. 8 The result of simulation of proposed low-power clock generator

Table 1. Power consumptions of the proposed clock generator

Input freq. [Hz]	Output freq. [Hz]	Power supply [V]	Power con. [uW]
30k	3k	1.8	1.181
100M	10M	1.8	37.42

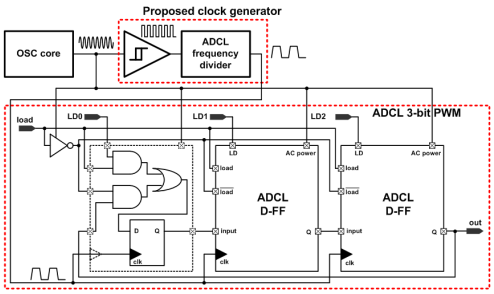
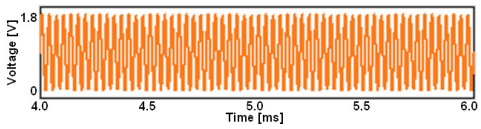
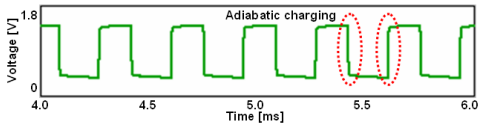


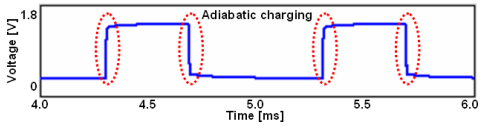
Fig. 9 ADCL 3-bit PWM system with proposed clock generator



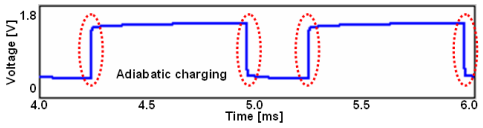
(a) Output waveform of the OSC core



(b) Output waveform of the proposed low-power clock generator



(c) Output waveform of the ADCL 3-bit PWM(input bit 100)



(d) Output waveform of the ADCL 3-bit PWM(input bit 110)

Fig. 10 The result of simulation of ADCL 3-bit PWM system with proposed clock generator

the power consumptions of proposed clock generator was approximately 1.181uW and 37.42uWat output 3kHz and 10MHz respectively.

In order to confirm operation of total ADCL system, the proposed clock generator and the

Table 2. Comparison of power consumptions

Paper	Type	Power Supply[V]	Freq. [Hz]	Power con.
[11]	Clock Gen.	1.2~2.4	37.5M	120uA
[12]		1.8	31.25k	0.2uA(0.36uW)
[13]		1	200M	140uW
[14]	Sync. Circuit	1.8	133M	53mW
[15]		1.8	100M ~1G	16mW@100MHz 64mW@1GHz
[16]		1.8	120M ~2.16G	16.2mW@2.16GHz
This work		1.8	3k	1.181uW
			10M	37.42uW

ADCL 3-bit PWM of Ref. [10] were simulated using a 0.18um standard CMOS technology and hspice as shown in Fig. 9. Operation of proposed clock generator and the ADCL system has been confirmed as shown in Fig. 10.

Power consumption of the proposed low-power clock generator for the ADCL is compared with that of other synchronization system. Table 2 summarizes several specifications of clock generators in Clock Gen. group and synchronous circuits in Sync. circuit group. It shows that the summation of power consumption both the Schmitt trigger circuit and the frequency divider is lower than that of both the lowest in Clock Gen. group; [12] 0.36uW and the lowest in Sync. circuit group;[15] 16mW. Therefore, proposed clock generator has been found to consume less power than the others.

Ⅴ. Conclusion

In order to reduce the power dissipation in conventional CMOS logic and operate adiabatic charging/discharging with low power for the ADCL, the clock signal of logic circuits should be synchronized with the AC power signal. If an AC

power supply and a clock generator are individually designed, therefore, a synchronous circuit will be needed for adiabatic charging. Although, conventional PLL and DLL are usually used for the synchronization of each AC signal, those have very complex schematic and large power consumptions.

To solve this problem, a novel low-power clock generator synchronized with the AC power signal has been proposed using the ADCL buffer for the ADCL system. The Schmitt trigger circuit has been designed to make the AC power signal into clock signal and synchronize for adiabatic charging. Furthermore, the ADCL frequency divider has been designed not only to divide frequency of output signal of the Schmitt trigger but also to synchronize and adiabatic charging with low power using the ADCL buffer. The power consumptions of the clock generator for the ADCL are approximately 1.181uW and 37.42uW at output 3kHz and 10MHz respectively. Proposed clock generator was found to be less power consumption than the others.

감사의 글

The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Rohm Corporation and Toppan Printing Corporation.

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저자 소개

조승일(Seung-Il Cho)

2006년 목포해양대학교 해양전자통신공학부 졸업 (공학사)
2008년 동대학교 대학원 해양전자공학과 졸업(공학석사)
2008~2010년 TOMATOLSI R&D사업부 주임연구원
2010년~현재 일본 YAMAGATA대학교 이공학연구과 박사과정
※ 관심분야 : 아날로그 디지털 mixed 회로설계, 저전력 회로설계, 고주파 회로설계

김성권(Seong-Kweon Kim)

2002년 일본 TOHOKU대학교 대학원 전자공학과(공학박사)
2002~2004년 일본 TOHOKU대학교 전기통신연구소 Assistant Professor & Research Fellow
2004~2009년 목포해양대학교 해양전자통신공학부 2009년~현재 서울과학기술대학교 전자 IT미디어 공학과 부교수
※ 관심분야 : 음향신호처리, 아날로그 저전력 회로설계, 무선통신용 LSI 설계, 고주파 회로설계, 차세대 무선통신시스템

하라다 토모치카 (Tomochika Harada)

2000년 일본 TOHOKU대학교 대학원 정보공학과(공학박사)
2000~2003년 일본 CHUO대학교 technical staff
2003~현재 일본 YAMAGATA대학교 이공학연구과 Assistant Professor
※ 관심분야 : ultra-low power mixed signal circuits, semiconductor sensors based on MOSFET

요코야마 미치오 (Michio Yokoyama)

1994년 일본 TOHOKU대학교 대학원 전자공학과(공학박사)
1994~2001년 일본 TOHOKU대학교 전기통신연구소
2001~현재 일본 YAMAGATA대학교 이공학연구과 Associate professor
※ 관심분야 : RF-MOS, RF system package, low-power design, bio-system engineering