

Digital Control Strategy for Single-phase Voltage-Doubler Boost Rectifiers

Younghoon Cho[†], Hyungsoo Mok^{**}, Jun-Keun Ji^{***}, and Jih-Sheng Lai^{*}

[†]Dept. of Electrical and Computer Engineering, Virginia Tech, Blacksburg, USA

^{**}Dept. of Electrical Engineering, Konkuk University, Seoul, Korea

^{***}Dept. of Electrical and Communication Engineering, Soonchunhyang University, Asan, Korea

Abstract

In this paper, a digital controller design procedure is presented for single-phase voltage-doubler boost rectifiers (VDBR). The model derivation of the single-phase VDBR is performed in the s -domain. After that the simplified equivalent z -domain models are derived. These z -domain models are utilized to design the input current and the output dc-link voltage controllers. For the controller design in the z -domain, the traditional K-factor method is modified by considering the nature of the digital controller. The frequency pre-warping and anti-windup techniques are adapted for the controller design. By using the proposed method, the phase margin and the control bandwidth are accurately achieved as required by controller designers in a practical frequency range. The proposed method is applied to a 2.5 kVA single-phase VDBR for Uninterruptible Power Supply (UPS) applications. From the simulation and the experimental results, the effectiveness of the proposed design method has been verified.

Key words: Voltage-Doubler Boost Rectifier, Power factor correction, Digital current controller, z -domain modelling, zero-order hold, digital delays

I. INTRODUCTION

Single-phase power factor correction (PFC) boost rectifiers have been used in many applications such as uninterruptible power supplies (UPS), telecommunications, computers, and so on, due to the intensification of regulations in power systems [1–6]. Among the many single-phase PFC circuits, the voltage-doubler boost rectifier (VDBR) has been used in some applications in where a higher dc-link voltage is necessary, because it can achieve high output voltages with a unity power factor input current at a low distortion, which is comparable to a standard boost PFC rectifier [7]. Basically, the controller of these VDBR consists of inner input current and outer dc-link

voltage loops, and this configuration is similar to that of general boost PFC rectifiers. Hence many previous studies for general boost PFC rectifiers can be adapted for the control of VDBR as follows. In [8], [9], average current mode control methods without input voltage sensing have been proposed for general and dual boost PFC rectifiers. A dc-link voltage sensorless method has been proposed in [10]. In [11]–[13], duty feed-forward strategies have been proposed to improve the response and stability of boost PFC rectifiers by compensating the admittance component of the entire control system. Reference [14] proposes a multiple controller technique to improve the total harmonic distortion (THD) by considering multiple control models according to the magnitude of the input voltage. On the other hand, many studies about the digital control of PFC converters have been conducted because their interface is flexible in digital control system [15]–[18]. In [16], a diode current sampling technique is proposed to simplify the signal conditioning circuit and to achieve digital average current mode control. Reference [17] studies a discontinuous conduction mode (DCM) mode detector and digital predictive control techniques. A digital nonlinear carrier control strategy

Manuscript received Nov. 18, 2011; revised May 3, 2012

Recommended for publication by Associate Editor Se-Kyo Chung.

[†]Corresponding Author: yhcho98@vt.edu

Tel: +1-540-808-6100, Virginia Tech

^{*}Dept. Electrical and Computer Engineering, Virginia Tech, USA

^{**}Dept. of Electrical Engineering, Konkuk University, Korea

^{***}Dept. of Electrical and Communication Engineering, Soonchunhyang University, Korea

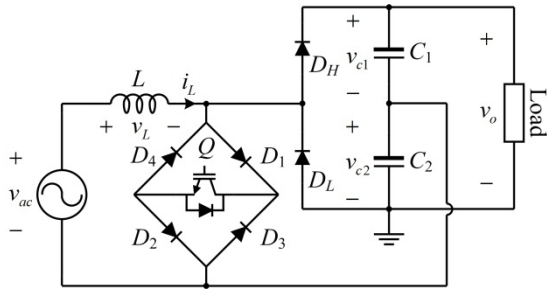


Fig. 1. Single phase voltage doubler boost rectifier.

has been proposed to implement the low cost digital control system in [18]. In [19], [20], the modeling and control of VDBRs are discussed.

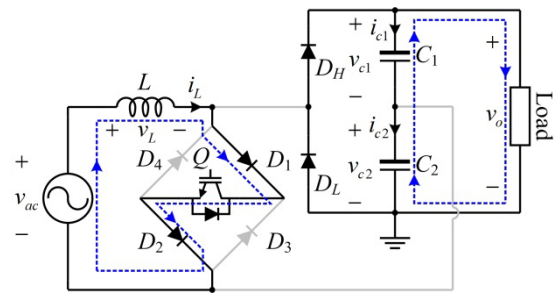
In this paper, a digital controller design methodology is presented for single-phase VDBRs. To accomplish this, an average modeling of a VDBR is performed, and equivalent z -domain models are derived. These derived z -domain models are utilized to design the input current and the dc-link voltage controllers. For controller design in the z -domain, the traditional K-factor method is modified by considering the nature of the digital controller. Frequency pre-warping and anti-windup techniques are adapted for the controller design. By using the proposed method, the phase margin and the control bandwidth are accurately achieved as required by controller designers in a practical frequency range. The proposed method is applied to a 2.5 kVA single-phase VDBR for Uninterruptible Power Supply (UPS) applications. From the simulation and the experimental results, the effectiveness of the proposed design method has been verified. This paper is organized as follows. In Section II, the model derivation of the single-phase VDBR is addressed. In Section, the modified K-factor design approach and the controller design methodology are introduced. Simulation and experimental results on a digitally controlled 2.5 kVA VDBR are given in Sections IV and V. Conclusions are provided in Section VI.

II. MODELING OF THE SINGLE-PHASE VDBR

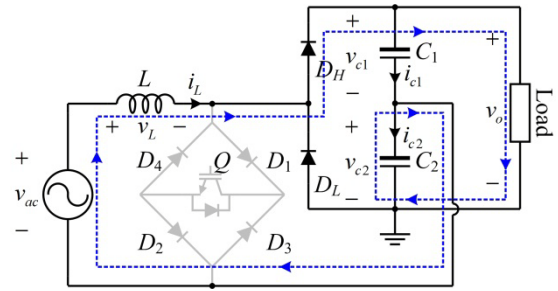
Fig. 1 shows the circuit diagram of the VDBR dealt with in this paper. The VDBR consists of two fast recovery diodes, D_H and D_L , four rectification diodes, D_1 , D_2 , D_3 , and D_4 , one inductor L , and two dc-link capacitors, C_1 and C_2 . In this section, an average model of this converter is derived in the s - and z -domain.

A. Small Signal Model Derivation

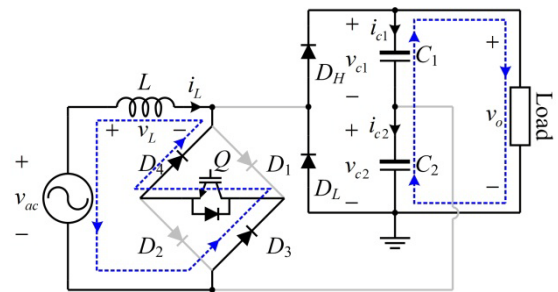
In order to derive a model of the VDBR, some analysis of the circuit operation is necessary. In Fig. 2, the operation mode of the circuit, according to the direction of the input voltage v_{ac} and the status of the switch Q , is shown. If v_{ac} is positive and Q is 1, the energy is stored in the input inductor L , and the load is supplied by the dc-link capacitors, as shown in Fig. 2(a). In this case, the state equations can be written as:



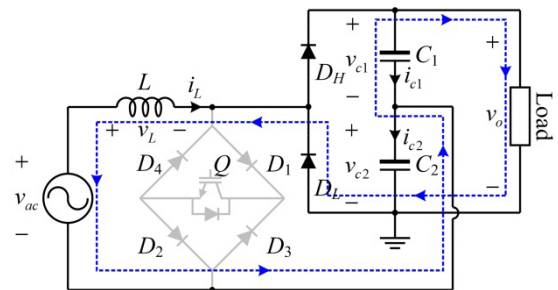
(a) $v_{ac} \geq 0$ and $Q = 1$



(b) $v_{ac} \geq 0$ and $Q = 0$



(c) $v_{ac} < 0$ and $Q = 1$



(d) $v_{ac} < 0$ and $Q = 0$

Fig. 2. Operation mode of the VDBR.

$$\frac{d}{dt} \begin{bmatrix} i_L \\ v_{c1} \\ v_{c2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & -\frac{1}{R_o C_1} & -\frac{1}{R_o C_1} \\ 0 & -\frac{1}{R_o C_2} & -\frac{1}{R_o C_2} \end{bmatrix} \begin{bmatrix} i_L \\ v_{c1} \\ v_{c2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix} v_{ac} \quad (1)$$

When v_{ac} is positive and Q is 0, the current path through the diode rectifier and Q is blocked, and the input power and the stored power in L are simultaneously supplied to the dc-link

TABLE I
 SIMULATION PARAMETERS

Input voltage rms (V_g)	120 V
dc-link voltage (V_o)	380 V
dc-link capacitance (C_1, C_2)	1 mF
Input inductance (L)	430 μ H
Load resistance (R_o)	54 Ω
Switching frequency (f_{sw})	40 kHz

capacitor C_1 and the load, while the lower side capacitor C_2 is discharging, as shown in Fig. 2(b). In this situation, the state equations can be established as:

$$\frac{d}{dt} \begin{bmatrix} i_L \\ v_{c1} \\ v_{c2} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} & 0 \\ \frac{1}{C_1} & -\frac{1}{R_o C_1} & -\frac{1}{R_o C_1} \\ 0 & -\frac{1}{R_o C_2} & -\frac{1}{R_o C_2} \end{bmatrix} \begin{bmatrix} i_L \\ v_{c1} \\ v_{c2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix} v_{ac} \quad (2)$$

For the negative cycles of v_{ac} , if Q is 1, the state equation becomes same as (1). If Q is 0 and v_{ac} is less than zero, the state equation can be written as:

$$\frac{d}{dt} \begin{bmatrix} i_L \\ v_{c1} \\ v_{c2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{1}{L} \\ 0 & -\frac{1}{R_o C_1} & -\frac{1}{R_o C_1} \\ \frac{1}{C_2} & -\frac{1}{R_o C_2} & -\frac{1}{R_o C_2} \end{bmatrix} \begin{bmatrix} i_L \\ v_{c1} \\ v_{c2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix} v_{ac} \quad (3)$$

In all of the cases, the output voltage v_o is represented as:

$$v_o = \begin{bmatrix} 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ v_{c1} \\ v_{c2} \end{bmatrix} \quad (4)$$

By using the equations, the small signal control-to-inductor current model $G_{id}(s)$ is derived as:

$$G_{id}(s) = \frac{\tilde{i}_L(s)}{\tilde{d}(s)} = \frac{V_g}{D} \frac{s(C_1 \Delta(s) + C_2)}{Ls^2(C_1 \Delta(s) + C_2) + \Delta(s)D^2} \quad (5)$$

$$\Delta(s) = R_o C_2 s + 1 \quad D = 1 - D$$

where V_g , D , \tilde{i}_L , and \tilde{d} refer to the magnitude of the input voltage, the duty cycle at the moment, the perturbation of the inductor current and the duty cycle, respectively. Equation (5) is a third order control-to-inductor current model for the VDBR.

The capacitances of C_1 and C_2 are large enough to be constant in a PWM switching cycle, and the values are almost same. By using these facts, it can be assumed that C_2 is a voltage source rather than a capacitor during positive cycles. For negative cycles, C_1 can be considered as a voltage source. Then, the number of states in (1) to (4) shrinks from 3 to 1. For positive cycles, i_L and v_{c1} are used. On the other hand, i_L and

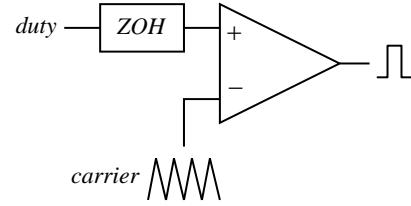


Fig. 3. Uniformly sampled PWM.

v_{c2} are used in negative cycles. By considering the reduced states and the fact that C_1 and C_2 have the same capacitance C , $G_{id}(s)$ is simplified to a second order model as in:

$$G_{id}(s) = \frac{V_g}{D} \frac{(\Delta_c(s) + 1)}{(\Delta_c(s) L s + R_o D^2)} \quad \Delta_c(s) = R_o C s + 1 \quad (6)$$

In practice, a more simplified transfer function as in (7) can be utilized by approximating the high frequency components [13].

$$G_{id}(s) \approx \frac{V_g}{D} \frac{1}{Ls} \quad (7)$$

B. Equivalent z-domain Model Derivation and Verification

In this section, the frequency responses of the three derived models are compared. For this comparison, the utilized parameters are shown in Table I. If the positive or negative cycle is considered only, the voltage gain of the VDBR is the same as that obtained with a typical boost converter except that the output voltage is double. Then, the minimum duty cycle in the steady state is:

$$D = 1 - \frac{V_g}{0.5V_o} \approx 0.3684 \quad (8)$$

By using those values, the transfer functions are derived as:

$$G_{id}^3(s) = \frac{441845.7369(s + 37.04)}{(s + 18.53)(s^2 + 18.51s + 9.274e^5)} \quad (9)$$

$$G_{id}^2(s) = \frac{441845.7369(s + 37.04)}{s^2 + 18.52s + 9.277e^5} \quad (10)$$

$$G_{id}^1(s) = \frac{190}{4.3e^{-4}s} \quad (11)$$

where $G_{id}^1(s)$, $G_{id}^2(s)$, and $G_{id}^3(s)$ are derived from first, second, and third order models. The voltage and the current controller are implemented in a digital controller. Consequently, the control-to-inductor current models should be evaluated in the z-domain. In order to obtain them in the z-domain, a zero order hold (ZOH) block is assumed through the path between the duty cycle and the comparator for the PWM operation [22]. By taking a ZOH approximation of (9), (10), and (11), their equivalent z-domain models are obtained as follows:

$$G_{idz}^3(z) = \frac{11.05z^2 - 22.08z + 11.03}{z^3 - 2.998z^2 + 2.998z - 0.9991} \quad (12)$$

$$G_{idz}^2(z) = \frac{11.05z - 11.04}{z^2 - 1.999z + 0.9995} \quad (13)$$

$$G_{idz}^1(z) = \frac{11.05}{z - 1} \quad (14)$$

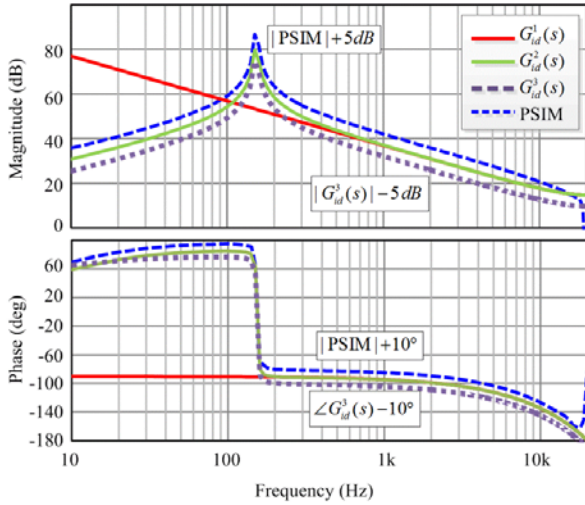


Fig. 4. Frequency responses of the transfer functions.

One simple method to obtain the transfer functions in numerical form is to use a software tool such as the *c2d* function in Matlab. Fig. 4 compares the frequency responses of the derived z -domain models and the switching model with the parameters built into the PSIM simulation software. To clearly show the tendencies of each response, the magnitude and the phase offsets of $G_{id}^3(s)$ and the PSIM switching model are intentionally added. The frequency ranges from 10 Hz to 20 kHz, where the frequency is same with the Nyquist frequency of the sampled system. The switching model also matches well with $G_{id}^2(s)$ and $G_{id}^3(s)$ until 10 kHz, except near the resonant point. From 10 kHz to 15 kHz, the magnitudes of the derived three transfer functions boost slightly because of the side effect of the ZOH block while one of the switching models is decreasing. Above 15 kHz, the response of the switching model is not convincing because of the numerical error in the simulation routine. However, errors above the 10 kHz range among the models may be ignored, because in practice the current controller bandwidth which is crucial for determining the control performance will be located at less than 10 kHz. For this reason, at less than 300 Hz, the response difference between $G_{id}^1(s)$ and the others can also be ignored to design the current controller. From the analysis, it is supposed that the derived z -domain models can be applicable to the design of the current controller.

C. DC Link Model Derivation

The small signal model of the dc-link and the load is given by:

$$G_{vd}(s) = \frac{\tilde{v}_o(s)}{\tilde{i}_L(s)} = \frac{R_o}{R_o \frac{C_1 + C_2}{2} s + 1} \quad (15)$$

If the capacitances of C_1 and C_2 are equal so that the value is given by C , (15) can be rewritten as:

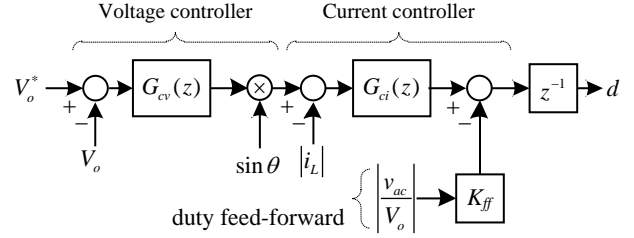


Fig. 5. Control structure for the single-phase VDBR.

$$G_{vd}(s) = \frac{R_o}{R_o C s + 1} \quad (16)$$

III. DIGITAL CONTROLLER DESIGN

Fig. 5 shows the control structure including the voltage and the current controller for the single-phase VDBR. The entire controller consists of the voltage and the current controller. In this section, the design procedure for the controller is described in detail.

A. Consideration of the Digital Delay Effect

In digitally controlled PFC, there are mainly two additional digital delay factors when compared to analog control. One is the effect of the digital PWM (DPWM). This factor is already considered as the ZOH block in the previous section. Another factor is the unit sample delay caused by the iteration timing of the software routine. In this study, the software routine is iterated once in a sampling instant, and the sampling instant is synchronized to the peak or valley points of the PWM carrier. Hence, the unit sampling delay is modeled as z^{-1} , as shown in Fig. 5. To simplify the design process of the current controller, the simple first order model $G_{id}^1(z)$ is utilized. Here, the unit sample delay z^{-1} should be considered as:

$$G_{idc}(z) = z^{-1} G_{idc}^1(z) = \frac{11.05}{z(z-1)} \quad (17)$$

The derived transfer function $G_{idc}(z)$ in (17) is used for the current controller design.

If the period of the PWM switching cycle is represented as T_{sw} , the delay induced from the ZOH block is $0.5T_{sw}$. By considering the unit sampling delay and the DPWM delay, which is modeled as the ZOH block, the total digital delay in the digitally controlled VDBR corresponds to $1.5T_{sw}$.

B. Digital Current Controller Design

The digital current controller consists of feed-forward and feedback controllers. In addition a unidirectional current control scheme is employed. The role of the feed-forward controller is to pre-compensate the duty variance according to the regular input voltage swing. The feed-forward compensator $G_{ff}(z)$ is implemented as:

$$G_{ff}(z) = -K_{ff} \left| \frac{V_{ac}}{V_o} \right| \quad (18)$$

where K_{ff} is the gain of the feed-forward controller. Ideally, K_{ff} is chosen as 2 by considering the effect of the voltage doubling. By applying the feed-forward controller, it is expected that the

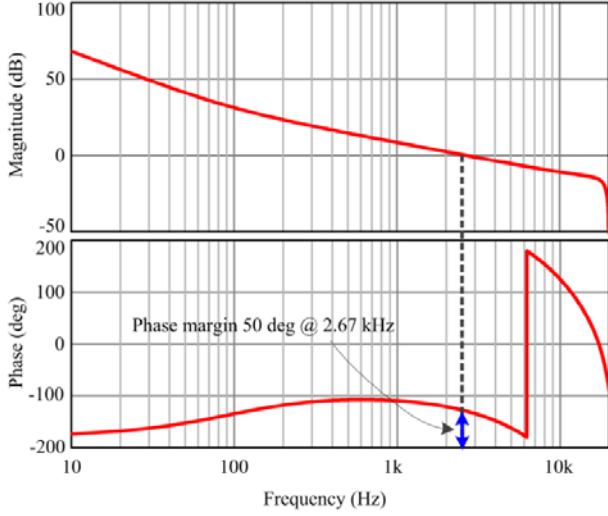


Fig. 6. Loop-gain of the current control system with the designed compensator.

portion of the feedback controller in the entire duty components is reduced and that the undesired admittance components in the feedback path are compensated. Consequently, the dynamic properties of the converter are improved [11]-[13].

The design of the feedback controller is more complicated than the design of the feed-forward controller. Here, the modified type II K -factor design approach was applied [23]. Assume that the specifications of the bandwidth f_c and the phase margin PM are as follows:

$$\begin{aligned} f_c &= f_s / 15 = 2.67 \text{ kHz} \\ PM &= 50 \text{ deg} \end{aligned} \quad (19)$$

By considering the frequency pre-warping for the digital control implementation, the pre-warped frequency of f_c is calculated as,

$$\omega_{c_pw} = \frac{2}{T_{sw}} \tan(f_c T_{sw} \pi) \quad (20)$$

By using (17), the magnitude and the phase at ω_{c_pw} are calculated as:

$$\begin{aligned} |G_{idc}(z)| &= 26.57 \text{ dB @ } \omega_{c_pw} \\ \angle G_{idc}(z) &= -125.9 \text{ deg @ } \omega_{c_pw} \end{aligned} \quad (21)$$

Then the desired gain boost G_b and the phase boost ϕ_b are evaluated as:

$$\begin{aligned} G_b &= 10^{-28.48/20} \approx 0.03767 \\ \phi_b &= 125.9 \text{ deg} \end{aligned} \quad (22)$$

From (19) and (22), the K -factor for this system is calculated as:

$$K = \sqrt{\frac{1 + \sin\left(\left(PM - (90^\circ - \phi_b)\right) \frac{\pi}{180}\right)}{1 - \sin\left(\left(PM - (90^\circ - \phi_b)\right) \frac{\pi}{180}\right)}} \approx 28.57 \quad (23)$$

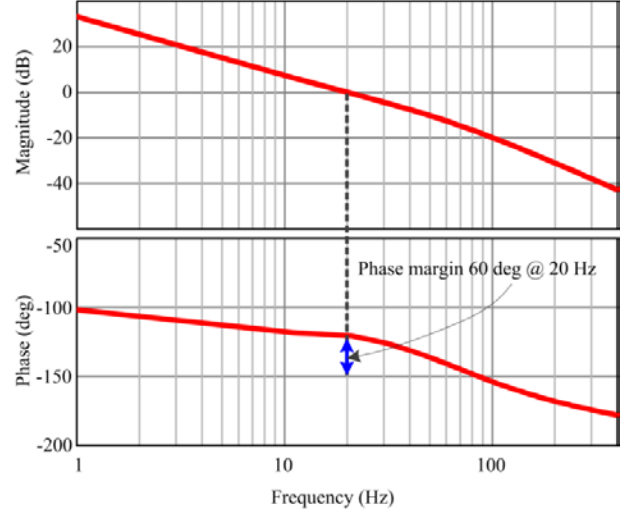


Fig. 7. Loop-gain of the voltage control system with the designed compensator.

By considering the frequency pre-warping for the digital control implementation, the pre-warped frequency of f_c is calculated as:

$$\omega_{c_pw} = \frac{2}{T_{sw}} \tan(f_c T_{sw} \pi) \quad (24)$$

Finally, the controller $G_{cz}(z)$ is given by:

$$\begin{aligned} G_{cz}(z) &= \omega_{c_pw} \frac{G_b T_{sw}}{K} \frac{(z+1)}{2(z-1)} \frac{\left(1 + K \frac{2(z-1)}{\omega_{c_pw} T_{sw} (z+1)}\right)}{\left(1 + \frac{2(z-1)}{K \omega_{c_pw} T_{sw} (z+1)}\right)} \\ &= \frac{0.032552(z+1)(z-0.9852)}{(z-1)(z+0.7172)} \end{aligned} \quad (25)$$

In order to evaluate the performance of the entire system with the controller, the loop-gain of the current control system is shown in Fig. 6. As can be seen in the figure, the bandwidth

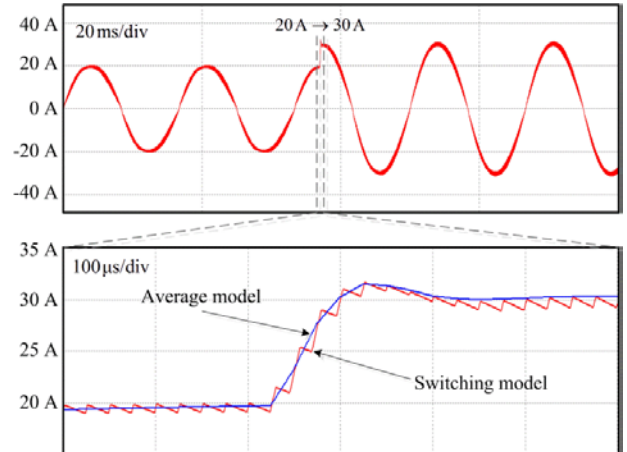


Fig. 8. Comparison of the transient responses in the switching and the average models.

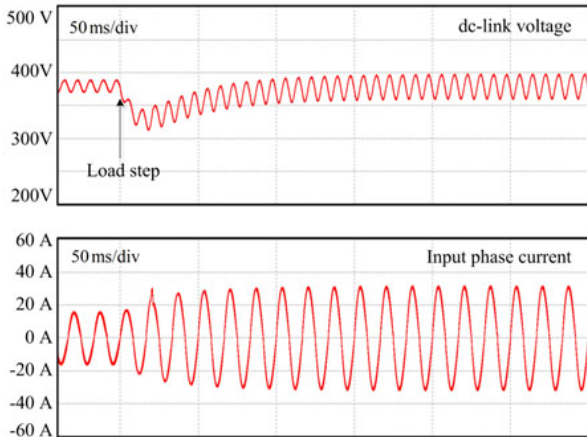


Fig. 9. Simulation result of the step load variance.

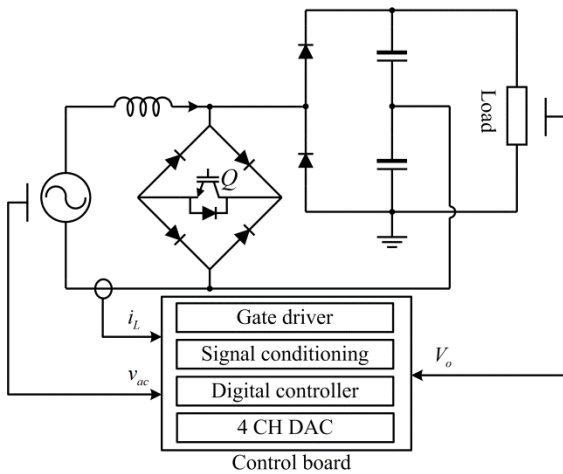


Fig. 10. Experimental setup.

and the phase margin are an exact match with the given specification in (19).

C. Digital Voltage Controller Design

Unlike the current controller design, the voltage controller for a single-phase VDBR requires a lower bandwidth to avoid the 120Hz frequency ripple issue. In this study, the target bandwidth and the phase margin are chosen as 20 Hz and 60 deg. In order to design the voltage controller, (16) is utilized to analyze the system response. Similar to the design of the current controller, the voltage controller is designed as:

$$G_{vc}(z) = \frac{0.0005753(z+1)(z-0.9989)}{(z-1)(z-0.9909)} \quad (26)$$

As can be seen in Fig. 7, (25) satisfies the desired control specification.

IV. SIMULATION RESULTS

A PSIM simulation model is built to verify the designed current and voltage controllers for a single-phase VDBR. The maximum power rating of the converter is 2.5 kW. The parameters in Table I are also used for the simulation. The

control structure is also same as that shown in Fig. 5. In order to verify the accuracy of the derived average model in section II, both the switching model and the average model in (14) are simulated simultaneously. In addition, the same voltage and current controllers designed in section III are applied to both of the models. The reference phase angle is provided by a phase locked loop (PLL). Fig. 8 compares the transient responses in the switching and the average current models. In the figure, the peak current reference was changed from 20 A to 30 A. In the zoomed-in section in Fig. 8, the current responses from the switching model and the average model are shown. Except for the switching ripple component, the tendencies of both of the waveforms are almost coincident. From this simulation result, it is supposed that the derived average model and the switching model match well.

Fig. 9 shows the time-domain simulation results of the dc-link voltage and the input phase current. At $t = 0.05$ s, the load is step changed from 50% to 100%. As shown in the figure, the dc-link recovers its reference value, 380 V, in 0.2 s while the peak of the current reference is increased from 15 A to 30 A. In Fig. 9, the voltage ripple, whose frequency is twice that of the fundamental frequency 60 Hz, is monitored. This voltage ripple is caused by the nature of the single-phase system, where the electrical power fluctuates.

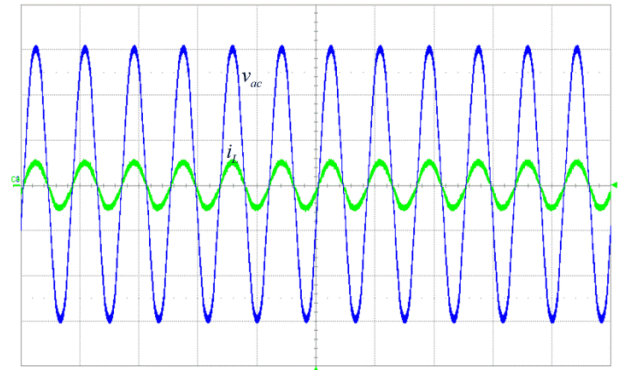


Fig. 11. Input voltage and current. (v_{ac} : 50 V/div, i_L : 20 A/div, x-axis: 20 ms/div)

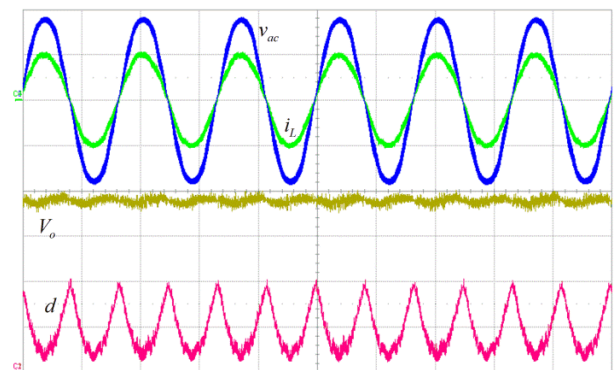


Fig. 12. Experimental result with 1.6 kW operation. (v_{ac} : 100 V/div, i_L : 20 A/div, V_o : 100 V/div, d : 0.5/div, x-axis: 10 ms/div)

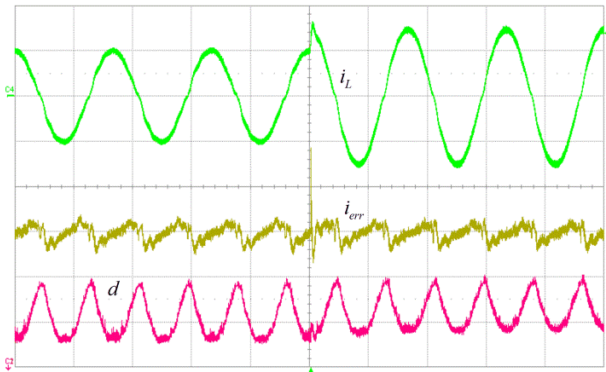


Fig. 13. Step response test. (i_L : 20 A/div, i_{err} : 5 A/div, d : 0.5/div, x-axis: 10 ms/div)

V. EXPERIMENTAL RESULTS

Experiments have been carried out to verify the designed current controller. Fig. 10 shows the experimental configuration. The control board consists of a gate driver, a signal conditioning circuit, a 32 bit digital signal processor (DSP) with interface circuitries, and a 4 channel digital-to-analog converter (DAC). In order to measure the input and output voltages and the input current, a LEM's closed-loop type Hall effect LV-20P voltage sensor and a LA-50P current sensor have been employed.

Fig. 11 shows the input voltage and the input current when the output power is about 800W. The input voltage is assumed to be in a 10% undervoltage condition. As can be seen in the figure, the input current is well regulated and without a severe distortion.

Fig. 12 shows the input voltage, the input current, the output voltage, and the duty reference. The output power is about 1.6 kW which is almost 65% of the rated power. Similar to the previous condition, the input current regulation is performed very well so that the shape of the current is almost a pure sinusoidal waveform. At the output voltage, the well-known double frequency power fluctuation occurs. By using the DAC in the control board, the duty reference is monitored. Note that the maximum value of the duty reference is 1.0 near the zero crossing points of the input voltage and the input current.

In order to show the dynamic characteristics of the converter, the step response results are shown in Fig. 13. To see the effect of the current controller, no voltage controller is assumed. At $t = 0.05$ s, the maximum magnitude of the current reference is changed from 20 A to 30 A. In this case, the output power is varied from 65% to 100% of the rated power. As shown in the figure, no severe ringing is found during the transient. In the figure, the error between the current reference and the input current is represented as i_{err} , which is monitored by using the DAC. Note that the amount of the maximum current error at the steady state does not change very before or after the step response. In fact, this error is caused by the DCM operation of the converter near the zero crossing points, where the converter states are acting as variables. To overcome this distortion, some special control techniques which are beyond the scope of this paper may be necessary.

From the test results, it is supposed that the designed digital controller operates very well without instability such

as ringing or subharmonics which usually occur when a s -domain controller is directly converted into the z -domain. Therefore, the design procedure described in this paper is convincing.

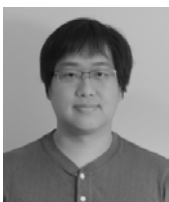
VI. CONCLUSION

In this paper, a digital controller design methodology has been described for single-phase VDBRs. To design the digital controller directly, the z -domain models of the converter were derived with consideration of the ZOH effect. By using the derived model, the digital current controller was designed with the modified K-factor approach. The advantage of the proposed method is that the bandwidth and the phase margin can be accurately designed as long as the converter is operating in physical ranges. The proposed method has been verified by simulation and experimental results from a 2.5 kVA single-phase VDBR for UPS applications.

REFERENCES

- [1] F. Musavi, W. Eberle, and W. G. Dunford, "A High-Performance Single-Phase Bridgeless Interleaved PFC Converter for Plug-in Hybrid Electric Vehicle Battery Chargers," *IEEE Trans. Ind. Appl.*, Vol. 47, No. 4, pp. 1833-1843, Jul./Aug. 2011.
- [2] M. M. Jovanovic and Y. Jang, "State-of-the-Art, Single-Phase, Active Power-Factor-Correction Techniques for High-Power Applications-An Overview," *IEEE Trans. Ind. Electron.*, Vol. 52, No. 3, pp. 701-708, Jun. 2005.
- [3] S. Kim and P. N. Enjeti, "A Modular Single-Phase Power-Factor-Correction Scheme With a Harmonic Filtering Function," *IEEE Trans. Ind. Electron.*, Vol. 50, No. 2, pp. 328-335, Apr. 2003.
- [4] Y.-K. Lo, S.-Y. Ou, and H.-J. Chiu, "On Evaluating the Current Distortion of the Single-Phase Switch-Mode Rectifiers With Current Slope Maps," *IEEE Trans. Ind. Electron.*, Vol. 49, No. 5, pp. 1128-1137, Oct. 2002.
- [5] X. Yang, Y. Ying, and W. Chen, "A Novel Interleaving Control Scheme for Boost Converters Operating in Critical Conduction Mode," *Journal of Power Electronics*, Vol. 10, No. 2, pp. 132-137, Mar. 2010.
- [6] T. Meng, and *et al*, "Novel Passive Snubber Suitable for Three-Phase Single-Stage PFC Based on an Isolated Full-Bridge Boost Topology," *Journal of Power Electronics*, Vol. 11, No. 3, pp. 264-270, May 2011.
- [7] J. C. Salmon, "Circuit Topologies for Single-Phase Voltage-Doubler Boost Rectifiers," *IEEE Trans. Power Electron.*, Vol. 8, No. 4, pp. 512-529, Oct. 1993.
- [8] J. Rajagopalan, F. C. Lee, and P. Nora, "A General Technique for Derivation of Average Current Mode Control Laws for Single-Phase Power-Factor-Correction Circuits Without Input Voltage Sensing," *IEEE Trans. Power Electron.*, Vol. 14, No. 4, pp. 663-672, Jul. 1999.
- [9] G.-G. Park, K.-Y. Kwon, and T.-W. Kim, "PFC Dual Boost Converter Based on Input Voltage Estimation for DC Inverter Air Conditioner," *Journal of Power Electronics*, Vol. 10, No. 3, pp. 293-299, May 2010.
- [10] T. Ohnishi and M. Hojo, "DC Voltage Sensorless Single-Phase PFC Converter," *IEEE Trans. Power Electron.*, Vol. 19, No. 2, pp. 404-410, Mar. 2004.
- [11] D. M. Van de Sype, and *et al*, "Duty-Ratio Feedforward for Digitally Controlled Boost PFC Converters," *IEEE*

- Trans. Ind. Electron.*, Vol. 52, No. 1, pp. 108-115, Feb. 2005.
- [12] M. Chen and J. Sun, "Feedforward Current Control of Boost Single-Phase PFC Converters," *IEEE Trans. Power Electron.*, Vol. 21, No. 2, pp. 338-345, Mar. 2006.
- [13] K. P. Louganski and J.-S. Lai, "Current Phase Lead Compensation in Single-Phase PFC Boost Converters With a Reduced Switching Frequency to Line Frequency Ratio," *IEEE Trans. Power Electron.*, Vol. 22, No. 1, pp. 113-119, Jan. 2007.
- [14] F. Tahami, S. Poshtkouhi, and H. M. Ahmadian, "Piecewise Affine Control Design for Power Factor Correction Rectifiers," *Journal of Power Electronics*, Vol. 11, No. 3, pp. 327- 334, May 2011.
- [15] V. M. Rao, and *et al*, "Experimental Comparison of Digital Implementations of Single-Phase PFC Controllers," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 1, pp. 67- 78, Jan. 2008.
- [16] J.-W. Shin, B.-C. Hyeon, and B.-H. Cho, "Digital Control of a Power Factor Correction Boost Rectifier Using Diode Current Sensing Technique," *Journal of Power Electronics*, Vol. 9, No. 6, pp. 903- 910, Nov. 2009.
- [17] F.-Z. Chen and D. Maksimovic, "Digital Control for Improved Efficiency and Reduced Harmonic Distortion Over Wide Load Range in Boost PFC Rectifiers," *IEEE Trans. Power Electron.*, Vol. 25, No. 10, pp. 2683-2692, Oct. 2010.
- [18] B. A. Mather and D. Maksimovic, "A Simple Digital Power-Factor Correction Rectifier Controller," *IEEE Trans. Power Electron.*, Vol. 26, No. 1, pp. 9-19, Jan. 2011.
- [19] D. Borgonovo and S. A. Mussa, "Single-Phase Boost PFC Voltage-Doubler Self-Controlled Using FPGA," in *Proc. IEEE PESC'08*, pp. 4457- 4463, Jun. 2008.
- [20] F. J. C. Padilha and M. D. Bellar, "Modeling and Control of the Half-Bridge Voltage-Doubler Boost Converter," in *Proc. IEEE ISIE'03*, pp. 741-745, Jun. 2003.
- [21] Y.-K. Lo, C.-T. Ho, and J.-M. Wang, "Elimination of the Output Voltage Imbalance in a Half-Bridge Boost Rectifier," *IEEE Trans. Power Electron.*, Vol. 22, No. 4, pp. 1352- 1360, Jul. 2007.
- [22] D. M. Van de Sype, K. D. Gussemé, F. M. L. L. De Belie, A. P. Van den Bossche, and J. A. Melkebeek, "Small-Signal z-Domain Analysis of Digitally Controlled Converters," *IEEE Trans. Power Electron.*, Vol. 21, No. 2, pp. 470- 478, Mar. 2006.
- [23] Y. Cho, H. Miwa, and J.-S. Lai, "A Digital Single-loop Control of Multiphase DC-DC Converter for Fuel Cell Powered Truck Auxiliary Power Unit," *IEEE Trans. Ind. Electron.*, To be published.



Younghoon Cho was born in Seoul, Korea, in 1980. He received his B.S. in Electrical Engineering from Konkuk University, Seoul, Korea, in 2002, and his M.S. in Electrical Engineering from Seoul National University, Seoul, in 2004. He is currently working toward his Ph.D. at Virginia Tech, Blacksburg, VA, USA. From 2004 to 2009, he was an Assistant Research Engineer at the Hyundai MOBIS R&D Center, Yongin, Korea. His current

research interests include high power converters, multilevel converters, soft switching inverters, and digital control techniques.



Hyungsoo Mok received his B.S., M.S., and Ph.D. in Electrical Engineering from Seoul National University, Korea, in 1986, 1988, and 1992, respectively. From 1993 to 1997, he was with the Department of Control and Instrumentation Engineering, Seoul National Polytechnic University, Seoul, Korea. Since 1997, he has been with the Department of Electrical Engineering, Konkuk University, Seoul, Korea. His current teaching and research interests include electric machines, electric machine drive systems, and power electronic control for industrial and power systems.



Jun-Keun Ji received his B.S., M.S., and Ph.D. in Electrical Engineering from Seoul National University, Seoul, Korea, in 1986, 1988, and 1994, respectively. From 1991 to 1994, he was a Research Engineer with KESRI. Since 1994, he has been a faculty member in the Department of Electrical Engineering, Soonchunhyang University, Choongnam, Korea. Currently, he is an Associate Editor of the Journal of Power Electronics. His research interests include electric machine drives, power converter control techniques, power quality issues, and motion control applications.



Jih-Sheng Lai received his M.S. and Ph.D. in Electrical Engineering from the University of Tennessee, Knoxville, TN, USA, in 1985 and 1989, respectively. From 1980 to 1983, he was the Head of the Electrical Engineering Department, Ming-Chi Institute of Technology, Taipei, Taiwan, where he initiated a power electronics program and received a grant from his college and a fellowship from the National Science Council to study abroad. In 1986, he became a staff member at the University of Tennessee, where he taught control systems and energy conversion courses. In 1989, he joined the Electric Power Research Institute (EPRI) Power Electronics Applications Center (PEAC), where he managed EPRI-sponsored power electronics research projects. From 1993, he worked as the Power Electronics Lead Scientist at the Oak Ridge National Laboratory, where he initiated a high power electronics program and developed several novel high power converters including multilevel converters and soft-switching inverters. His work has brought him several distinctive awards including a Technical Achievement Award on Lockheed Martin Award Night, three

IEEE IAS Conference Paper Awards, and Best Paper Awards from IECON-97, IPEC-05, and PCC-07. In 1996, he joined the Virginia Polytechnic Institute and State University. He is currently a Professor and the Director of the Future Energy Electronics Center. His current research interests include high efficiency power electronics conversions for high power and high energy applications. He has published more than 240 technical papers and 2 books and received 20 U.S. patents. Dr. Lai chaired the 2000 IEEE Workshop on Computers in Power Electronics (COMPEL 2000), the 2001 IEEE/DOE Future Energy Challenge, and the 2005 IEEE Applied Power Electronics Conference and Exposition (APEC 2005).