A Novel Control Strategy for Input-Parallel-Output-Series Inverter System

Chun-Wei Song*, Rong-Xiang Zhao*, Wang-Qing Lin*, and Zheng Zeng*

Abstract – This paper presents a topology structure and control method for an input-parallel-output-series(IPOS) inverter system which is suitable for high input current, high output voltage, and high power applications. In order to ensure the normal operation of the IPOS inverter system, the control method should achieve input current sharing(ICS) and output voltage sharing(OVS) among constituent modules. Through the analysis in this paper, ICS is automatically achieved as long as OVS is controlled. The IPOS inverter system is controlled by a three-loop control system which is composed of an outer common-output voltage loop, inner current loops and voltage sharing loops. Simulation results show that this control strategy can achieve low total harmonic distortion(THD) in the system output voltage, fast dynamic response, and good output voltage sharing performance.

Keywords : Inverter, Input-parallel, Output-series, Input current sharing, Output voltage sharing

1. Introduction

System integration technology in power electronics has developed greatly since the beginning of this century. As integration technology has a very high application value, it has become one of the most popular topics in the field of power electronic research in recent years. Power electronic system integration can be divided into component-level integration, module-level integration and system-level integration [1]. We can make standardized modules for DC-DC converters or inverters. Then, these standardized modules, which are characterized by low power ratings and low stress of voltage or current, are grouped together through certain connection modes such as parallel or series. This series/parallel conversion system embodies the idea of system-level integration technology. According to different combination forms, the series/parallel system can be divided into the following four categories:input-parallel-output-parallel(IPOP) inverter system, input-parallel-output-series(IPOS) inverter system, input-series-output-parallel(ISOP) inverter system, and input-series-output-series(ISOS) inverter system. The series/parallel conversion system in which the basic modules are DC-DC converters has been studied extensively, for example in [2-6]. This paper, on the other hand, focuses on the DC-AC series/parallel inverter system. A lot of research has been done on IPOP inverter systems, for example in [7]. In order to solve current sharing, a number of control strategies, such as wireless-parallel control, master-slave control, and distributed-logic control, have been put forward. The ISOP inverter system has been analyzed in depth in [8]. The three-loop control, including input voltage loop, current loop in each module, and input voltage sharing loop, is used to control an ISOS inverter system in [9]. This control strategy has two control objectives. One is input voltage sharing (IVS) among modules. The other is equality of phase in both output voltage and current. OVS is automatically achieved as long as these two objectives are controlled. Meanwhile, few studies have been done for IPOS inverter systems. In this paper, a novel control strategy for the IPOS inverter system is presented.

The topology structure of the IPOS inverter system is presented in Section 2. This topology structure can not only reduce current stress of switching devices in the DC-DC converter, but can also reduce voltage stress of switching devices in the inverter. It is suitable for high-input-current, high-output-voltage and high-power applications. Through the analysis in Section 3, we find ICS is automatically achieved as long as OVS is controlled. The control strategy used in this paper is described in detail in Section 4. It is composed of an outer common-output voltage loop, inner current loops, and voltage sharing loops. Simulation results, shown in Section 5, show that this control strategy achieves low THD in the system output voltage, fast dynamic response, and good OVS performance.

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2. Topology Structure of IPOS Inverter System

The presented topology structure of the IPOS inverter system is made up of N identical modules. The simplified diagram of this system is shown in Fig.1. In Fig.1, E is the input voltage of the system, i_{in} is the total input current, i_{in1}, i_{in2}, …, i_{inN} are the input currents of the modules, u_0 is the total output voltage, and u_{01}, u_{02}, …, u_{0N} are the output voltages of the modules. All input ports of the modules are connected together in parallel. The high-voltage output is obtained by connecting all output ports of the modules together in series.

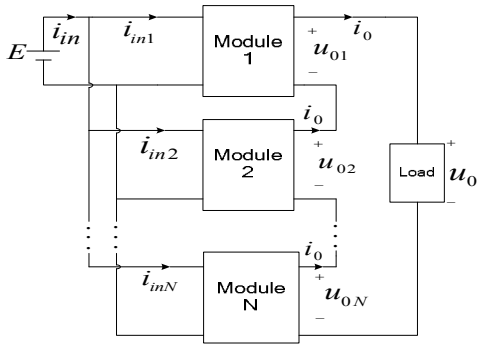

Fig. 1. Simplified diagram of IPOS inverter system

The specific circuit structure of each module is composed of a single-phase full-bridge DC-DC converter with LC low pass filter and a single-phase full-bridge inverter with output filter made up of inductor L_f and capacitor C_f. Module 1, with low pass filter L_1C_1, inductor L_{f1}, and capacitor C_{f1}, is shown in Fig.2. The output of each DC-DC converter is the DC side of an inverter. So the voltage of the DC side of the inverter can be regulated by the converter. According to the volt-second characteristic of both ends of the inductor L_1, we have

$$E_1' = 2 \cdot D \cdot E \cdot N_s / N_p \tag{1}$$

where E_1' is the output voltage of the converter, D is the conduction ratio of switching devices, N_P is the turns of the transformer primary winding, and N_S is the turns of the transformer secondary winding [10].

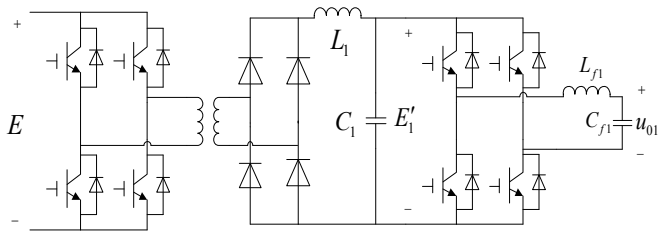

Fig. 2. Power circuit of Module 1

The volume of the high-frequency isolation transformer in the DC converter decreases with the increase of switching frequency so that the power density of the IPOS inverter system can be improved. In addition, the high-frequency isolation transformers isolate the low-voltage input ports from the total output voltage. There is no short circuit and no loop current between each module because of the existence of the high-frequency isolation transformers.

3. Relationship between ICS and OVS

We first assume that every module is a linear two-terminal circuit and that the circuit parameters of the modules are equal. Then, based on the reciprocal theorem for Module 1 and Module 2 we have

$$E \cdot i_{in2} + u_{01} \cdot i_0 = E \cdot i_{in1} + u_{02} \cdot i_0 \tag{2}$$

where i_0 is the output current of the IPOS inverter system. According to (2), we can obtain

$$E(i_{in2} - i_{in1}) = i_0(u_{02} - u_{01}) \tag{3}$$

Similarly, combining the relationship between Module i and Module i+1, for $2 \le i < N$, we have

$$\begin{cases} E(i_{in2} - i_{in1}) = i_0(u_{02} - u_{01}) \\ E(i_{in3} - i_{in2}) = i_0(u_{03} - u_{02}) \\ \vdots \\ E(i_{inN} - i_{in(N-1)}) = i_0(u_{0N} - u_{0(N-1)}) \end{cases} \tag{4}$$

If the OVS condition is met (including voltage amplitude and phase angle), we have

$$u_{01} = u_{02} = \cdots = u_{0N} \tag{5}$$

Substitution of (5) into (4), yields

$$\begin{cases} E(i_{in2} - i_{in1}) = 0 \\ E(i_{in3} - i_{in2}) = 0 \\ \vdots \\ E(i_{inN} - i_{in(N-1)}) = 0 \end{cases} \tag{6}$$

From (6), we have

$$i_{in1} = i_{in2} = \cdots = i_{inN} \tag{7}$$

Therefore, if the output voltage is shared evenly among the modules, so is the input instantaneous current. However, in the actual system, the circuit parameters of the modules are not exactly equal. Every module consisting of power electronic devices is a nonlinear two-terminal circuit. Even if the OVS condition is met, we cannot ensure that input instantaneous current sharing is achieved. But, if the output voltage is shared by the modules, i.e., u_{01}=u_{02}=...=u_{0N}, then,

based on the following analysis, output active power sharing among the modules is achieved. The output active power of each module is expressed as

$$P_{ox} = \int_0^{t_0} i_0 \cdot u_{0x} d(t) \quad (x = 1, 2, \cdots N) \tag{8}$$

Substitution of (5) into (8) yields

$$P_{o1} = P_{o2} = \cdots = P_{oN} \tag{9}$$

So, the output active powers of the modules are equal.

Suppose the efficiency of each module is 100%. Then, by power conversion, the input active power P_{inx} *(x=1,2,...,N)* of each module equals its output active power. Thus, we have

$$P_{inx} = \int_0^{t_0} E \cdot I_{inx} d(t) = P_{ox} \quad (x = 1, 2, \cdots N) \tag{10}$$

Substitution of (9) into (10) yields

$$\int_0^{t_0} E \cdot i_{in1} d(t) = \int_0^{t_0} E \cdot i_{in2} d(t) = \cdots = \int_0^{t_0} E \cdot i_{inN} d(t) \tag{11}$$

The average input current of each module is expressed as

$$I_{inx} = \frac{1}{t_0} \int_0^{t_0} i_{inx} d(t) \quad (x = 1, 2, \cdots N) \tag{12}$$

From (11), we have

$$\frac{1}{t_0} \int_0^{t_0} i_{in1} d(t) = \frac{1}{t_0} \int_0^{t_0} i_{in2} d(t) = \cdots = \frac{1}{t_0} \int_0^{t_0} i_{inN} d(t) \tag{13}$$

According to (12), (13):

$$I_{in1} = I_{in2} = \cdots = I_{inN} \tag{14}$$

So, we can conclude that if OVS is achieved, the average input currents of the modules must be equal.

4. Control Strategy

The goal of the control strategy is OVS. Each DC-DC converter is controlled by open-loop control. The conducting ratio of the switching element is 0.5. The cascaded inverters are controlled by three-loop control as is shown in Fig.3. The input u_r is the given reference voltage. G_{V0} is the voltage PI regulator in the outer loop. G_{i1}, G_{i2}, …, G_{iN} are current PI regulators in the inner current loops. G_{V1}, G_{V2}, …, G_{VN} are voltage sharing PI regulators in the voltage sharing loops. L_{f1}, L_{f2}, …, L_{fN} are the values of the filter inductors. C_{f1}, C_{f2}, …, C_{fN} are the values of the filter capacitors.

The outer control loop, which uses the output voltage as feedback, controls the output voltage and frequency of the IPOS inverter system. i_{ref0} (the output of the outer-loop voltage PI regulator G_{V0}) is the input to the inner current loops, which use the current of the filter inductor as feedback in each inverter. If the output voltages of the DC-DC converters are equal and, meanwhile, the modulated signals of the inverters are the same, then OVS can be achieved by just using the outer voltage loop and inner current loops. But, in the actual conditions, the circuit parameters of the modules are not exactly equal. Therefore, the feedback currents of the filter inductors are not the same, so that the output voltages of the DC-DC converters are also not the same. Although the modulated signals of the inverters are the same, OVS cannot be achieved by just using the outer voltage loop and inner current loops. The voltage sharing loop is added to adjust the reference value of the current in each inverter. I_{REFx}, which is the reference value of the current for Module x (x=1,2,…, N), is expressed as

$$I_{REFx} = i_{ref0} + i_{refx} \quad (x = 1, 2, \cdots, N) \tag{15}$$

where i_{refx} is the output of G_{Vx}.

The voltage u_0/N is the reference value of each voltage sharing loop. When $u_0/N > u_{0x}$ (u_{0x} is the output voltage of Module x), i_{refx} will increase. Then, I_{REFx} increases according to (15). The relationship between the current i_{Lx} of filter inductor L_{fx} and u_{0x} is

$$i_{Lx} - i_0 = C_{fx} \frac{du_{0x}}{dt} \quad (x = 1, 2, \cdots, N) \tag{16}$$

From (16), we have

$$u_{0x}(t) = \int_0^t (i_{Lx} - i_0) / C_{fx} dt \quad (x = 1, 2, \cdots, N) \tag{17}$$

Based on (17), with an increase of i_{Lx}, u_{0x} will increase until $u_0/N = u_{0x}$. Conversely, when $u_0/N < u_{0x}$, i_{refx} will decrease. Then, I_{REFx} decreases according to (15). Based on (17), with a decrease of i_{Lx}, u_{0x} will decrease until $u_0/N = u_{0x}$. Thus, OVS can be achieved. Then, ICS is automatically achieved according to Section 3.

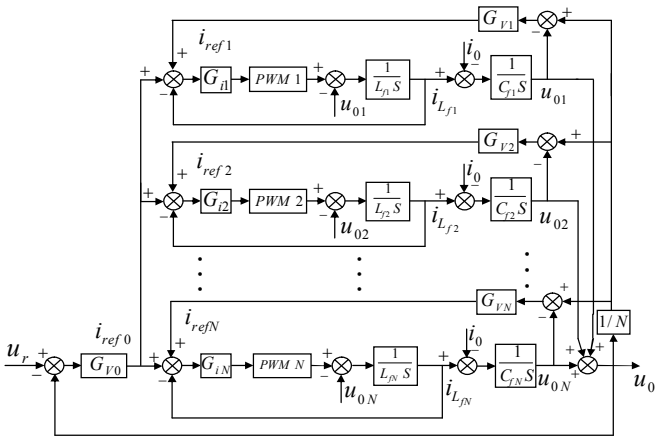

Fig. 3. Block diagram of the control strategy

5. Simulation Results

The simulation model consists of two standard modules. Simulation parameters are set for two cases. The following parameters are common for both cases. The capability of this IPOS inverter system is about 10 kW. The desired output voltage is 380 *sin(*100*πt)* V. The input voltage is 250 V. Load resistance R_L is 15 Ω. The carrier frequency of the SPWM modulation is 10 kHz. In order to avoid a huge impulse current in the input port of each module, the initial voltage of the filter capacitor in each DC-DC converter is set at 200 V.

In the first case, all corresponding parameters are the same in the two modules. There is no voltage sharing loop in the control method of the cascaded inverters. L_1 = 0.6 mH, C_1 = 500 μF, L_2 = 0.6 mH, C_2 = 500 μF in the two DC-DC converters. L_{f1} = 1 mH, C_{f1} = 20 μF, L_{f2} = 1 mH, C_{f2} = 20 μF in the two inverters.

The output voltages of the two modules completely overlap, as is shown in Fig.4. Fig. 4 demonstrates that when corresponding circuit parameters, switch signals of DC-DC converters, and the carrier phases of SPWM modulation of cascaded inverters are the same in the two modules, OVS can be achieved without voltage sharing loops in the control strategy.

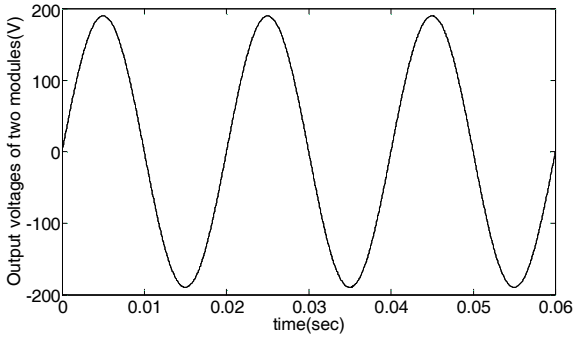

Fig. 4. Output voltages of the two modules without voltage sharing loops in the first case

The input currents of the two modules also completely overlap, as is shown in Fig.5. Therefore, when the two modules are fully symmetrical, if the output voltage is shared evenly among the modules, then so is the input instantaneous current.

In the second case, some circuit parameters are different. L_1 = 0.6 mH, C_1 = 450 μF, L_2 = 0.5 mH, C_2 = 500 μF in the two DC-DC converters. L_{f1} = 1.2 mH, C_{f1} = 20 μF, L_{f2} = 1 mH, C_{f2} = 25 μF in the two inverters. If the control strategy that is used is the same as in the first case, the output voltages of the two modules are as shown in Fig.6. We can easily see that OVS is not achieved.

So, ICS also cannot be achieved, as indicated in Fig.7(a) and Fig.7(b), when OVS cannot be achieved, which is the case when the control strategy without voltage sharing loops is used.

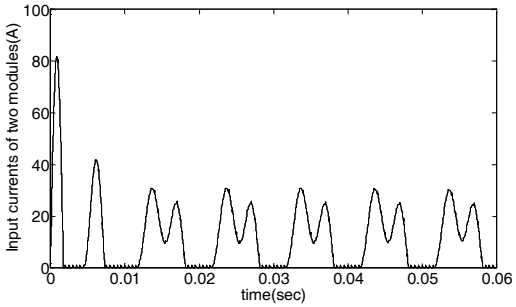

Fig. 5. Input currents of the two modules without voltage sharing loops in the first case

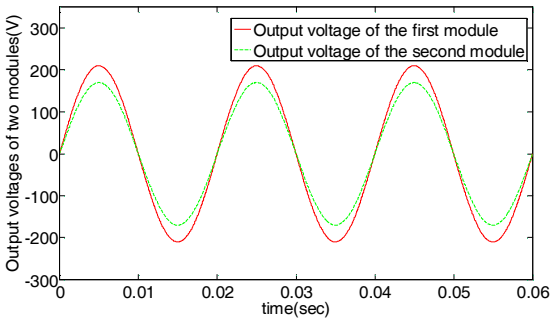

Fig. 6. Output voltages of two modules without voltage sharing loops in the second case

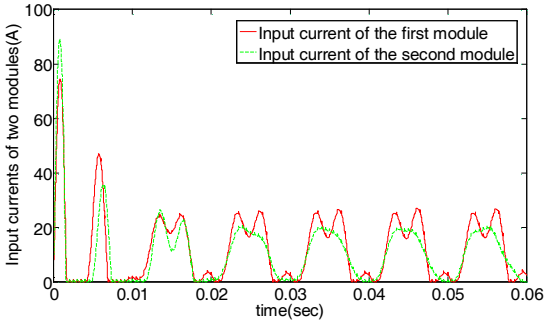

Fig. 7. (a) Input currents of two modules without voltage sharing loops in the second case

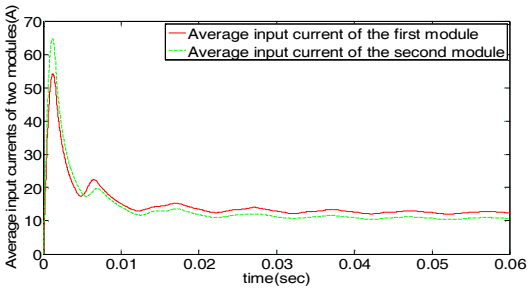

Fig.7. (b) Average input currents of two modules without voltage sharing loops in the second case

In order to improve the OVS effect, the cascaded inverters are controlled by three-loop control, which is described in Section 4. The waveform of the output voltage that has been filtered is shown in Fig.8. The output voltage, whose THD is only 0.01%, can quickly reach a stable state.

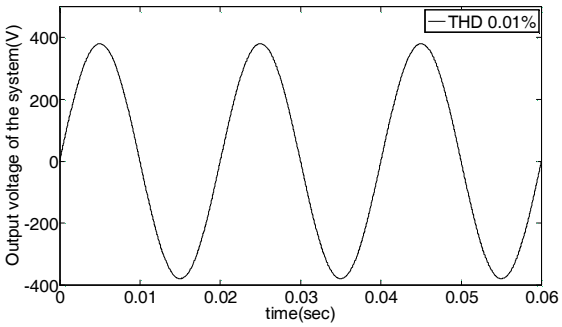

Fig. 8. The output voltage in the second case

The output voltages of the two modules almost overlap, as is shown in Fig.9. The OVS effect is good because of the addition of the voltage sharing loops.

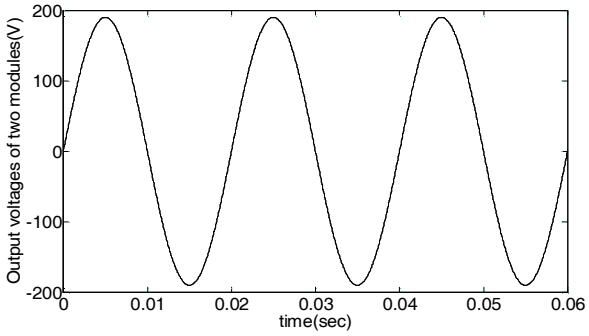

Fig. 9. Output voltages of two modules with voltage sharing loops in the second case

Because the parameters of corresponding elements are different in the two modules, the input instantaneous currents, which are shown in Fig.10(a), are not always equal even though there is good OVS effect.

However, Fig.10(b) shows that the average input current is shared evenly among the modules when OVS has been achieved.

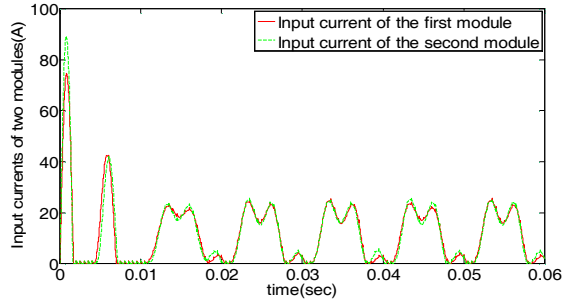

Fig.10(a). Average input currents of two modules with voltage sharing loops in the second case

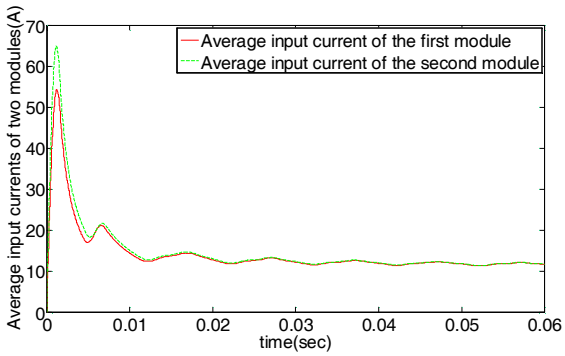

Fig.10(b). Average input currents of two modules with voltage sharing loops in the second case

6. Conclusions

Through the analysis in this paper, input current sharing is automatically achieved as long as output voltage sharing is achieved. The IPOS inverter system is controlled by three-loop control, which is composed of an outer common output voltage loop, inner current loops and voltage sharing loops. Simulation results show that this control strategy can achieve low total harmonic distortion in the system output voltage, fast dynamic response and good output voltage sharing performance whether corresponding parameters among modules are equal or not.

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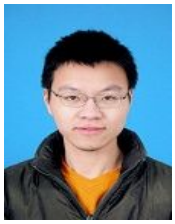

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