A Novel Topology Structure and Control Method of High-Voltage Converter for High-Input-Voltage Applications

Chun-Wei Song*, Rong-Xiang Zhao*, and Hao Zhang**

Abstract – In this paper, a three-phase high-voltage converter (HVC), in which the main structure of each phase is composed of a cascaded PWM rectifier (CPR) and cascaded inverter (CI), is studied. A high-voltage grid is the input of the HVC. In order to ensure proper operation of the HVC, the control method should achieve output voltage sharing (OVS) among the rectifiers in the CPR, OVS among the inverters in the CI, and high power factor. Master-slave direct-current control (MDCC) is used to control the CPR. The ability of the control system to prevent interference is strong when using MDCC. The CI is controlled by three-loop control, which is composed of an outer common-output-voltage loop, inner current loops and voltage sharing loops. Simulation results show low total harmonic distortion (THD) in the HVC input currents and good OVS in both the CPR and CI.

Keywords: High-voltage converter, Cascaded PWM rectifier, Cascaded inverter, Output voltage sharing

1. Introduction

HVC has been widely used in various industries. HVC structures have not yet formed a unified topology because there are advantages and disadvantages in the switching devices that are used, such as thyristors, GTO, IGBT, IECT, IGCT and SGCT. In order to avoid the difficulties caused by the devices, there are two common types of solutions. One solution is the device series-parallel technology, such as in [1-4]. The other solution is the low-power unit series-parallel technology, for example in [5-6]. According to the voltage conversion process, HVC can be divided into high-high style and high-low-high style.

A high-high style HVC exports high voltage directly using the grid as the input source. It can reduce losses and improve efficiency by not using a step-down transformer or a step-up transformer. Three-level inverter and ac-ac frequency converter are the common topologies of this HVC. The thyristor, which is used by the ac-ac frequency converter, has many advantages, such as high voltage tolerance, high current capability, and strong overload protection ability [7]. The simple structure can be designed for an ac-ac frequency converter whose conversion efficiency is high. It is easily integrated in the system without using an electrolytic capacitor in the dc link. However, not only is THD high in both its input current and output voltage but, also, the power factor is low. In addition, the output frequency range is narrow. Compared with a two-level voltage source inverter at the same switching frequency, both the voltage stress of the single switching device and the derivative of the output voltage in the three-level voltage source inverter can be reduced by half [8]. And the THD in the output voltage can also be reduced. Because of these advantages, the three-level inverter is suitable for high-voltage frequency-control systems.

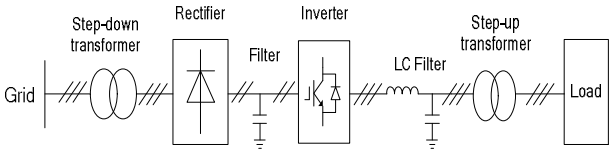

Fig. 1. Structure of traditional high-low-high style HVC

The structure of the traditional high-low-high style HVC is shown in Fig.1 [7]. First, a high ac voltage is converted into a low ac voltage by the step-down transformer; then a low ac voltage is rectified into a low dc voltage; then a low ac voltage is obtained from the inverter; and, finally, the output of the step-up transformer is a high ac voltage, which is used as the source for the load. Although such a structure can solve the problem of breakdown voltage, the current flowing through the switching device becomes large when the load is very large [7]. Both the losses and the volume of the system are large because of the step-up and step-down transformers. In addition, this HVC has great influence on the grid, as the THD in its input current is

* Dept. of Electrical Engineering, Zhejiang University, China. (scw0220@yahoo.com.cn)

** Department of Electrical and Mechanical Products Inspection, Shanghai Entry-Exit Inspection and Quarantine Bureau, China. (zariesh@hotmail.com)

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large.

The cell-series multi-level technology has been very popular as a solution for the high-low-high style HVC in recent years. Its structure is shown in Fig.2. First, the high input ac voltage is converted into a series of low ac voltages through a phase-shifting transformer. Then, taking phase A for example, the low ac voltages go through A_1, A_2, ..., A_n, which are ac-dc-ac inverters. Finally, the high output ac voltage is obtained by overlaying the output voltages of A_i $(i=1,2,...,n)$. This HVC can use low-power-level switching devices without being subjected to the problems caused by device series-parallel technology. What's more, this structure can adopt the technologies of phase-shifting and multiple rectification [9]. Also, it has little influence on the grid, as the THD in its input current is very small.

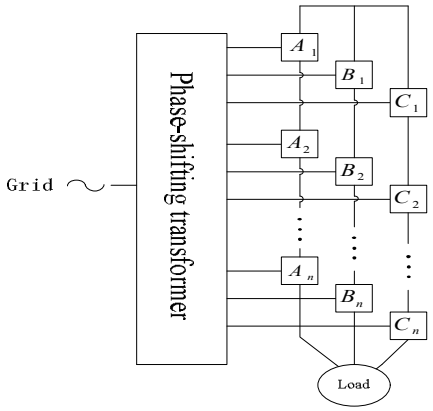

Fig. 2. The structure of cell-series multi-level HVC

The novel topology structure of HVC in this paper draws on the design of cell-series multi-level technology. The structure of each phase is independent. The structure does not contain a large phase-shifting transformer. Low dc voltages are obtained after power network voltages are rectified by CPR. One of the CPR's functions is the same as that of a multi-pulse rectifier: to reduce THD in the input current so that the structure has little influence on the grid. The high-voltage output is obtained from CI. In Section 2, the description of the topology is discussed in detail. In Section 3, the control method for CPR is discussed. In Section 4, the control method for CI is discussed. In Section 5, relationship between IVS and OVS is discussed. Simulation results, given in Section 6, show that the control method can ensure proper operation of the HVC and that it leads to low THD in both the input currents and the output voltages.

2. Novel Topology Structure of HVC

The simplified diagram of the HVC is shown in Fig.3. The circuit of each phase, which are identical, is suitable for modular assembly and production. The presented topology can lower the voltage class of the required power devices. The circuit of each phase is composed of CPR and CI. The dc voltage V_{xi} $(x=a,b,c;\ i=1,2,...,n)$, where x is the phase, is obtained after u_x $(x=a,b,c)$ is rectified by the CPR. The output of each rectifier is the dc side of a corresponding inverter. The high-voltage output u_{xo} $(x=a,b,c)$ is obtained from the CI. If *Rectifier xi* or *Inverter xi* $(x=a,b,c;\ i=1,2,...,n)$ fails, then both should be bypassed.

The specific circuit structure of phase A is shown in Fig.4. *Rectifier ai* is a single-phase full-bridge PWM rectifier. *Inverter ai* is a single-phase full-bridge inverter with *LC* filter and isolation transformer. The isolation transformers can isolate both the low-voltage output winding of each module from the high-voltage input side and the low-voltage input winding of each module from the total output voltage. There are no short circuits or loop currents between the modules.

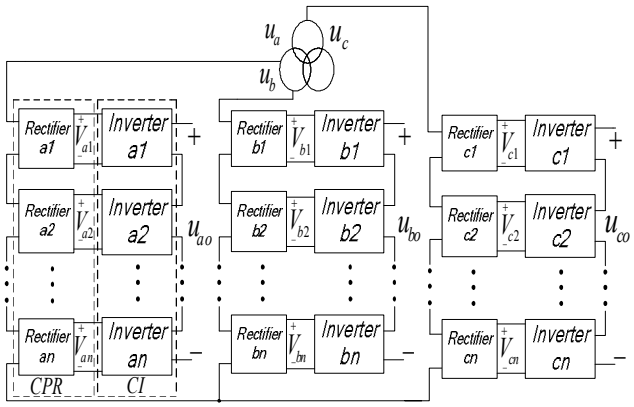

Fig. 3. The simplified diagram of the HVC

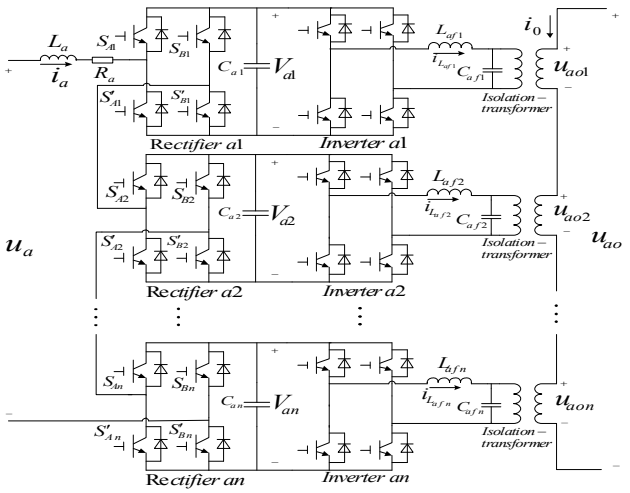

Fig. 4. Power circuit of phase A

3. Control Method for CPR

There are two functions of the CPR. One is to achieve low THD in the input currents and unity power factor operation. The other is to obtain the dc voltages provided for the inverters. The control strategy used for the CPR not only ensures that the input current phases follow the input voltage phases, but it also achieves OVS among the rectifiers in the CPR. Although the control strategy for the CPR does not consider input voltage sharing (IVS) among the rectifiers, IVS is automatically achieved as long as OVS among the inverters in the CI is controlled, based on the analysis in Section 5.

MDCC is used to control the CPR. The anti-interference ability of the control system is strong when MDCC is used. Taking phase A for example, the control diagram is shown in Fig.5. The control system is composed of an outer voltage loop, inner current loops and voltage sharing loops. G_{av0} is the voltage PI regulator. G_{avx} $(x=1,2,...,n)$ are the voltage-sharing PI regulators. G_{aix} $(x=1,2,...,n)$ are the current PI regulators. V_{aref} is the given reference total voltage of the CPR. The total output voltage of the CPR is used as feedback in the outer control loop. The product of the output of G_{av0} and $u_a/|u_a|$ is the given reference current of the inductor L_a. If the output value of G_{av0} is positive, the CPR is in the rectification state. Conversely, if the output value of G_{av0} is negative, the CPR is in the inversion state. The mean of the output voltages of the CPR is used as the reference value for the voltage-sharing loops. The voltages V_{ai} $(i=1,2,...,n)$ are used as feedback for the n voltage-sharing loops, one voltage for each loop, respectively. The difference between i_{aref} (the reference value of the input current of phase A) and i_s (the actual value of the phase A current) is the reference value for the current loop in each rectifier. PWM pulses for each rectifier are obtained after the output of the current regulator is compared with the triangular wave.

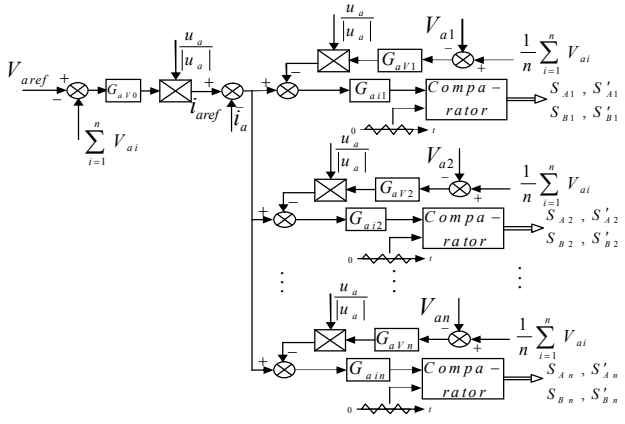

Fig. 5. Block diagram of the control strategy for CPR

The steady-state output voltage of the CPR can be maintained at V_{aref}, even when several damaged rectifiers need to be bypassed, by using this control method.

4. Control Method for CI

The high-voltage output is obtained from the CI in each phase. In order to ensure proper operation of the CI, the control method should achieve OVS among the inverters. Taking phase A for example, the CI is controlled by three-loop control, as is shown in Fig.6 [10]. The voltage u_{aoref} is the given reference voltage. G_{AV0} is the voltage PI regulator in the outer loop. G_{Ai1}, G_{Ai2}, …, G_{Ain} are current PI regulators in the inner current loops. G_{AV1}, G_{AV2}, …, G_{AVn} are voltage-sharing PI regulators in the voltage-sharing loops.

The sum of the output of G_{AV0} and the output of G_{Aix} ($x=1,2,\ldots,n$) is the reference value for inner current loop x (for $x=1,2,\ldots,n$), which uses the output current of the filter inductor as feedback in each inverter. The voltage u_{ao}/n is the reference value for each voltage-sharing loop. The steady-state output voltage of the CI can be maintained at u_{aoref}, even when several damaged inverters need to be bypassed, by using this control method.

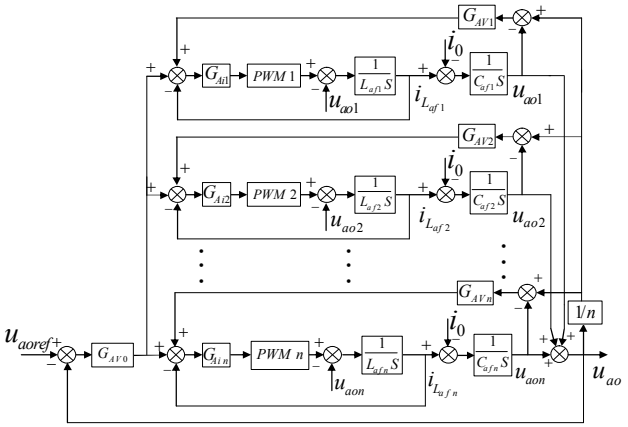

Fig. 6. Block diagram of the control strategy for the CI

5. Relationship between IVS and OVS

Through the analysis in this section, it is shown that input voltage sharing is automatically achieved as long as output voltage sharing is controlled. Taking phase A for example, the steady-state simplified diagram of this system, which is made up of n modules, is shown in Fig.7. The current i_a is the input current of phase A, i_{ao} is output current, u_{aox} $(x=1,2,...,n)$ is the output voltage of each module, and u_{aIx} $(x=1,2,...,n)$ is the input voltage of each module.

If the OVS condition among the inverters in the CI is met (including voltage amplitude and phase angle), we have

$$u_{ao1} = u_{ao2} = \cdots = u_{aon} = u_{ao} / n \quad (1)$$

The output active power of each module is expressed as

$$P_{aoi} = \int_0^{t_0} i_{ao} \cdot u_{aoi} d(t) \quad (i = 1, 2, \cdots n) \quad (2)$$

According to (1), (2):

$$p_{ao1} = p_{ao2} = \cdots = p_{aon} \quad (3)$$

The output reactive power of each module is expressed as

$$Q_{aoi} = \sqrt{(U_{aoi} I_{ao})^2 - (P_{aoi})^2} \quad (i = 1, 2, \cdots n) \quad (4)$$

In (4), U_{aoi} is the RMS value of u_{aoi} and I_{ao} is the rms value of i_{ao}. According to (1), (3), and (4):

$$Q_{ao1} = Q_{ao2} = \cdots = Q_{aon} \quad (5)$$

Suppose the efficiency of each module is 100%. Then, by power conversion, the input active power of each module equals its output active power. Similarly, the input reactive power of each module equals its output reactive power. Thus, we have

$$\begin{cases} P_{aIi} = P_{aoi} \\ Q_{aIi} = Q_{aoi} \end{cases} \quad (i = 1, 2, \cdots, n) \quad (6)$$

In (6), P_{aIi} is the input active power of module i, and Q_{aIi} is the input reactive power of module i. According to (4), (5), and (6):

$$\begin{cases} P_{aI1} = P_{aI2} = \cdots = P_{aIn} \\ Q_{aI1} = Q_{aI2} = \cdots = Q_{aIn} \end{cases} \quad (7)$$

Using the input impedance of each module, the equivalent circuit of the input side of phase A is shown in Fig. 8. The input current i_a is shown as a current source, $Z_0 = R_a + j\omega L_a$ (ω is the grid angular frequency), and the input impedance of each module is $Z_i = R_i + jX_i$ *(i=1,2,...,n)*. The input power of each module is expressed as

$$\begin{cases} P_{aIi} = {I_a}^2 R_i \\ Q_{aIi} = {I_a}^2 X_i \end{cases} \quad (i = 1, 2, \cdots, n) \quad (8)$$

According to (7), (8):

$$\begin{cases} R_1 = R_2 = \cdots = R_n \\ X_1 = X_2 = \cdots = X_n \\ Z_1 = Z_2 = \cdots = Z_n \end{cases} \quad (9)$$

The relationship between the input voltage and input current in each module is

$$\dot{U}_{aIi} = \dot{I}_a Z_i \quad (i = 1, 2, \cdots n) \quad (10)$$

According to (9), (10)

$$\dot{U}_{aI1} = \dot{U}_{aI2} = \cdots = \dot{U}_{aIn} \quad (11)$$

Thus, IVS is automatically achieved as long as OVS is controlled in the steady state.

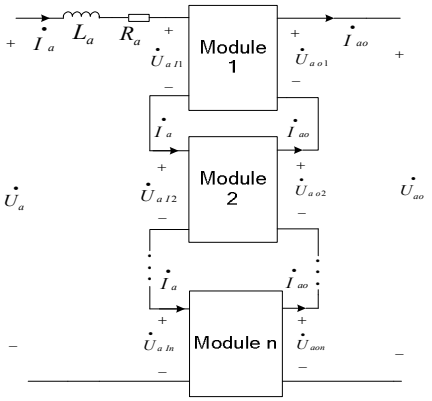

Fig. 7. The steady-state simplified diagram of phase A

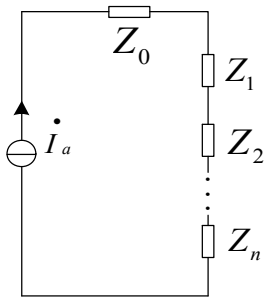

Fig. 8. Phase A equivalent circuit

6. Simulation Results

In the simulation model, the circuit structure of each phase includes a CPR consisting of two PWM rectifiers and a CI consisting of two inverters. The specific parameters are set as follows. The capacity of the HVC is about 10 kW. The frequency of the network voltage is 50 Hz. The amplitude of the network phase voltage is 1000 V. $R_a = R_b = R_c = 0.2\ \Omega$ and $L_a = L_b = L_c = 1.5$ mH on the line side. $R_{La} = R_{Lb} = R_{Lc} = 150\ \Omega$ is the star-connected load resistance. $C_{a1} = C_{b1} = C_{c1} = 300\ \mu$F and $C_{a2} = C_{b2} = C_{c2} = 320\ \mu$F in the CPR. $L_{af1} = L_{bf1} = L_{cf1} = 1.2$ mH; $C_{af1} = C_{bf1} = C_{cf1} = 20\ \mu$F; $L_{af2} = L_{bf2} = L_{cf2} = 1$ mH; and $C_{af2} = C_{bf2} = C_{cf2} = 25\ \mu$F in the CI. The given reference total voltage of the CPR is 1500 V. The given three-phase output voltages are symmetrical to each other. Taking phase A for example, the given output voltage is 1100 *sin(*100πt*)* V. The carrier frequency of the PWM signals is 10 kHz.

The output voltages, which have been filtered, are shown in Fig.9. After about one period, they are all in steady state.

This indicates that the dynamic response of the control method for the CI is fast. Through harmonic analysis, the THD of each output voltage is seen to be very low.

In order to avoid very large impulse currents in the input ports of the HVC, the initial voltages of the capacitors in the CPR are set at 500 V. The maximum absolute value of the initial impulse input current is less then 60 A, as is shown in Fig.10. The current i_b reaches steady state the fastest, using about 0.12s, compared to 0.27s for i_a and 0.23s for i_c. Through harmonic analysis, the THD of the three-phase input steady-state currents is seen to be about 7.5%, much less than that of an uncontrolled rectifier.

Through the following analysis and simulation results of phase A, we can observe that both the CPR and CI work properly. Fig.11 shows the relationship between the output voltages and the input current in the CPR. Before t = 0.24s, the input current i_a charges the capacitors in the CPR. In this process, V_{a1} and V_{a2} rise to about 890 V, which is bigger than the given referrence voltage of 750 V. From t = 0.24s to t = 0.27s, i_a becomes small. V_{a1} and V_{a2} decrease to the steady-state value of 750 V with the discharge of the capacitors C_{a1} and C_{a2}. Finally, V_{a1} and V_{a2} remain around 750 V, with small fluctuations. The phase current i_a can follow $u_a/|u_a|$, as is shown in Fig.11, so unity power factor operation of the HVC is achieved. In addition, it can be seen that the OVS effect is good in the CPR because V_{a1} and V_{a2} almost overlap.

After about one period, the output voltages of the CI, u_{ao1} and u_{ao2}, almost overlap, as is shown in Fig.12. Therefore, the output voltage is shared evenly among the two inverters in the CI.

When the HVC is in steady state, the input voltages of the two modules, u_{al1} and u_{al2}, consist mainly of the fundamental components, which are shown in Fig.13. The absolute error between the amplitudes of the fundamental components is less than 3 V, which can be ignored relative to the actual amplitudes (about 500 V). And the absolute error between the initial phase angles is less than 4°. So, IVS is automatically achieved as long as OVS is controlled in the steady state.

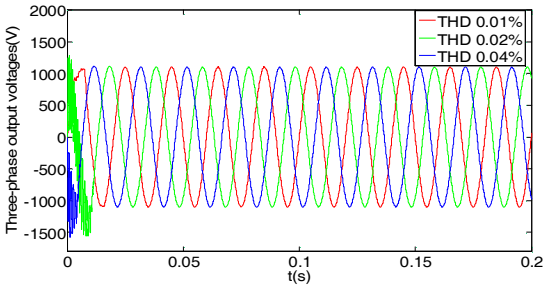

Fig. 9. Three-phase output voltages

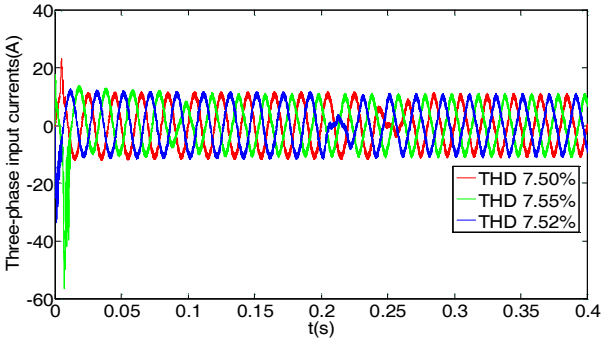

Fig. 10. Three-phase input currents

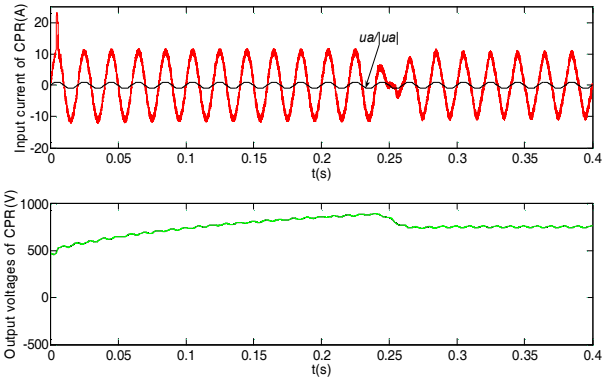

Fig. 11. Input current i_a and output voltages V_{a1} , V_{a2} in CPR

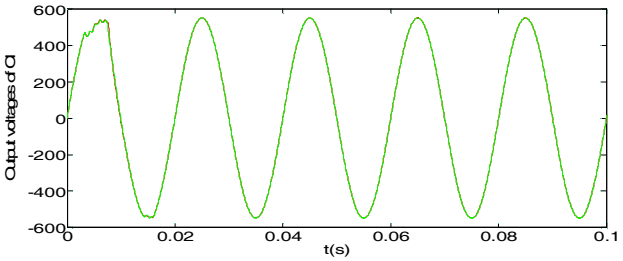

Fig. 12. Output voltages of the CI: u_{ao1}, u_{ao2}

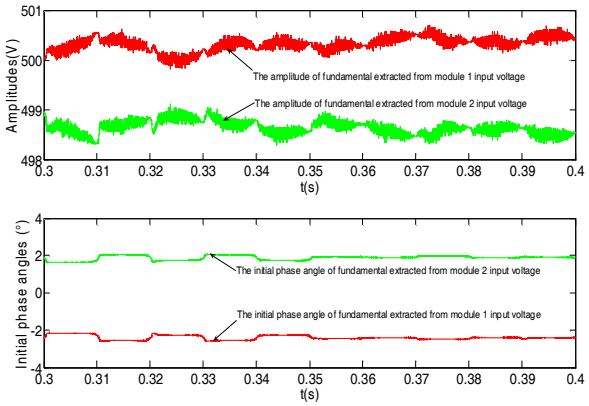

Fig. 13. Amplitudes and initial phase angles of the fundamentals extracted from u_{al1}, u_{al2}

7. Conclusions

The control method used in this paper can achieve OVS among the rectifiers in the CPR, OVS among the inverters in the CI, and unity power factor operation of the HVC. Through the analysis in this paper, it is seen that IVS of the HVC is automatically achieved as long as OVS of the HVC is controlled in the steady state. In addition, THD in both the input currents and output voltages of the HVC is low.

Acknowledgements

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Chun-Wei Song was born in Zhejiang, China, in 1987. He received his B.S. degree in electrical engineering in 2009 from China Jiliang University, Hangzhou, China. He is currently working toward the Ph.D. degree at the College of Electrical Engineering, in Zhejiang University, Hangzhou, China. His current research interests include motor control and power converter systems.

Rong-Xiang Zhao was born in Zhejiang, China, in 1962. He received his B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 1984, 1987, and 1991, respectively. He is currently a Professor in the Department of Electrical Engineering, Zhejiang University, where he is also the Director of the National Engineering Research Center for Applied Power Electronics. His current research interests include motors, motor control, and power converter systems.

Hao Zhang received his B.Sc. and M.Sc. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 2006, 2008, respectively. His current research interests include motor control and power converter systems.