

A Cascaded Multilevel Inverter Using Bidirectional H-bridge Modules

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Abstract – This paper presents a multilevel inverter configuration which is designed by insertion of a bidirectional switch between capacitive voltage sources and a conventional H-bridge module. The modified inverter can produce a better sinusoidal waveform by increasing the number of output voltage levels. By serial connection of two modified H-bridge modules, it is possible to produce 9 output voltage levels including zero. There are 24 basic switching patterns with the 9 output voltage levels. Among the patterns, we select the 2 most efficient switching patterns to get a lower switching loss and minimum dv/dt stress. We then analyze characteristics of Total Harmonic Distortion (THD) of the output voltage with variation of input voltage by computer-aided simulations and experiments.

Keywords: Bidirectional switch, Inverters, Multilevel systems, Total harmonic distortion (THD), H-bridge module

1. Introduction

The cascaded H-bridge multilevel inverter has been researched for high voltage applications since it has advantages in number of components, high reliability, and modularity [1]-[6]. The main purpose of a multilevel inverter is the generation of a high voltage using lower voltage rating devices connected in series. Also it has the potential to get a high quality output voltage by producing multi output voltage levels. However, it increases the number of switching devices and other components, which results in an increase of complexity problems and system cost.

Many multilevel inverter configurations have been researched to get a sinusoidal-like output voltage wave with minimum circuit components [7]-[11]. In reference [7], authors have tried to increase the number of output levels by switched series/parallel DC voltage sources. However, the configuration has brought a weakness in usage of high voltage applications due to its complexity in switch control and voltage stress (same as its input voltage source).

To alleviate these problems, multilevel inverters using a cascaded transformer have been studied in [8]. In the paper, the cascaded transformers produce trinary output voltage and it improves the shape of the output voltage waveform.

Reference [9] has a very similar concept with reference [8] but the configuration is suitable for high capacity applications. The multilevel inverter approach has merits in reduction of the number of switching devices and in a galvanic isolation between the source and loads by employing a cascaded transformer. However, it may decrease the power conversion efficiency, and increases volume and cost of the system due to the transformer. To decrease the number of transformers, a modified version of the cascaded-transformer based multilevel inverter has been reported in [10]. Authors in the paper have proposed two kinds of inverters according to the role. One is a level inverter, and the other is a Pulse Width Modulation (PWM) inverter. Pulse width modulated wave is added on a fundamental voltage level, which is generated by the Level inverter. The chopped wave is changed into a sinusoidal wave when load current is increased due to the filtering effect by the leakage inductance of the transformer. The presentable advantage of the method is to produce a high quality output voltage wave with a reduced number of transformers. However, it still has a drawback in power conversion loss generated by usage of the transformers. Moreover, those approaches in [8]-[10] employing low frequency transformers are inappropriate to the motor driver, which is operated by Variable Frequency (VF) control scheme due to saturation problem of the transformer.

The multilevel inverters in the references [7]-[11] have been designed with a cascaded H-bridge configuration. In general, the H-bridge configuration has an advantage in

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modularity and is a very efficient configuration to get multi output voltage level with minimum electric components. Therefore the cascaded H-bridge integrated multilevel inverter has been utilized for the decentralized power supply system of large capacity STATCOM [11] and solar power generation [12]. However, the cascaded H-bridge multilevel inverter requires multi input voltage sources to achieve multilevel output voltage [13] and insertion of input capacitors to get multi input voltage sources induces an imbalance of the input voltages [14]-[16].

We propose a modified multilevel inverter configuration to reduce the number of independent input voltage sources with minimum electric components and a maximum output voltage level. The proposed cascaded H-bridge multilevel inverter is configured by two independent DC input voltage sources, two H-bridge modules, and two bidirectional switches and it produces nine output voltage levels. There are 24 basic switching patterns with the 9 output voltage levels. Among the patterns, we select the 2 most efficient switching patterns to get lower switching loss and minimum dv/dt stress. Then we analyze characteristics of Total Harmonic Distortion (THD) of the output voltage with variation of input voltage. To verify the validity of the proposed multilevel inverter, we carried out a simulation and experiments based on a prototype.

2. Proposed Multilevel Inverter

2.1 General Cascaded H-bridge Multilevel Inverter

Fig. 1 shows a circuit configuration of a general cascaded H-bridge multilevel inverter. Each H-bridge module has an independent DC voltage source of E . Every output terminal of H-bridge cells is connected in series. So the output voltage can be obtained by Eq. (1). And the number of output voltage levels is obtained by Eq. (2).

$$v_{out} = \sum_{n=1}^k v_n = v_1 + v_2 + v_3 + v_4 \quad (1)$$

$$N = 2k + 1 \quad (2)$$

where k is the number of H-bridge cells.

In Eq. (1), v_n can be E , 0 , or $-E$; therefore, v_{out} can produce $-4E$, $-3E$, $-2E$, $-E$, 0 , E , $2E$, $3E$, $4E$ by mixing of each output voltage. We can notice that this kind of multilevel inverter is advantageous in terms of modularity and simplicity. However, it needs 16 switches and 4 independent DC input sources to produce nine output

voltage levels.

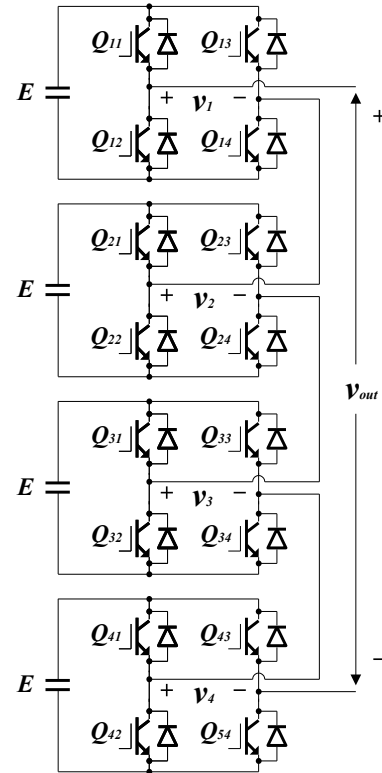


Fig. 1. Circuit configuration of a conventional cascaded H-bridge multilevel inverter to produce nine output voltage levels

2.2 Cascaded Transformer based Multilevel Inverter

To reduce the number of switches, a multilevel inverter using a cascaded transformer has been introduced in [8]. Fig. 2 shows a multilevel inverter employing a cascaded transformer. It has a single DC voltage source, two H-bridge cells, and two transformers. Since each secondary of the transformer is connected in series, the output voltage becomes the instantaneous sum of every secondary voltage of both transformers as given in Eq. (3). As well, the number of output voltage levels is determined by Eq. (4).

$$v_{out} = \sum_{n=0}^{k-1} 3^n \cdot v_{n+1} = v_1 + 3 \cdot v_2 \quad (3)$$

$$N = 3^k \quad (4)$$

where k is the number of transformers.

In Eq. (3), v_n can be E , 0 , or $-E$; therefore, v_{out} can produce $-4E$, $-3E$, $-2E$, $-E$, 0 , E , $2E$, $3E$, $4E$ by mixing of each secondary voltage of the transformers.

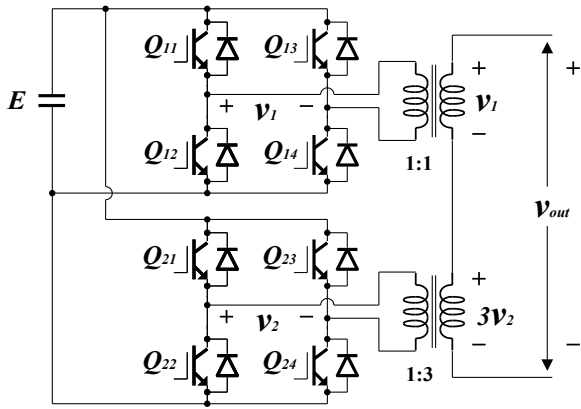


Fig. 2. Circuit configuration of a multilevel inverter having a cascaded transformer to produce nine output voltage levels

From Fig. 2, we can find that this multilevel inverter saves 8 switches and 3 DC voltage sources compared with the prior approach given in Fig. 1. It automatically achieves galvanic isolation between a source and loads by the cascaded transformer; however, it decreases the power conversion efficiency due to transformer loss, and increases total volume and cost of the system.

2.3 Multilevel Inverter Using Bidirectional Switches

To solve the problem of the above mentioned approaches, we present a modified multilevel inverter which has couple of bidirectional switches. One side of the switch is connected at neutral points of input voltage sources and the other is connected at neutral points of the H-bridge module as shown in Fig. 3. To generate nine output voltage levels, it needs two independent dc input voltage sources, two H-bridge modules, and two bidirectional switches. The circuit configuration of the proposed inverter is very similar to the configuration of a serial connection of conventional 5-level inverters [17-18]. It can prevent the efficiency drop induced by transformers in the multilevel configuration of Fig. 2. It can reduce the number of switches compared with the conventional cascaded H-bridge multilevel inverter shown in Fig. 1.

To synthesize nine output voltage levels, it employs two independent dc voltage sources of $2E$ which are divided into two input sources E in order to secure an additional dc voltage source of E . The inverter module having a bidirectional switch produces 5-levels of output voltage ($-2E, -E, 0, E, 2E$) by controlling of the switches. Since every output terminal of the inverter module is connected in series, the output voltage becomes the sum of the terminal voltages of each inverter.

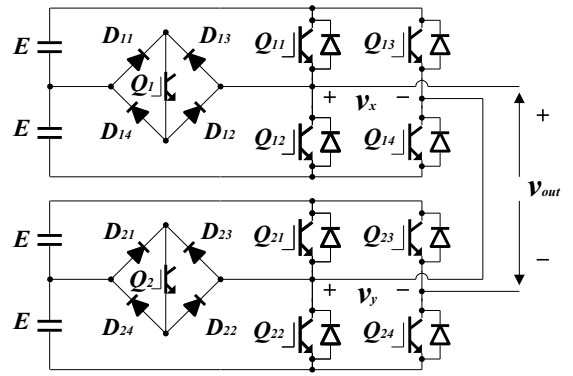


Fig. 3. Circuit configuration of the proposed multilevel inverter having bidirectional switches to produce nine output voltage levels

The switching function of an inverter can be summarized as

$$\begin{aligned}
 & \text{if } (Q_{n1}, Q_{n4}) = \text{on then } SF_n = 2 \\
 & \text{if } (Q_n, Q_{n4}) = \text{on then } SF_n = 1 \\
 & \text{if } (Q_{n1}, Q_{n3}) \text{ or } (Q_{n2}, Q_{n4}) = \text{on then } SF_n = 0 \\
 & \text{if } (Q_n, Q_{n3}) = \text{on then } SF_n = -1 \\
 & \text{if } (Q_{n2}, Q_{n3}) = \text{on then } SF_n = -2
 \end{aligned}
 \tag{5}$$

For generation of nine levels in an output voltage wave, we consider 24 switching patterns which are obtained by mixing the switching functions (SF_n) as listed in Table 1. It shows switching functions for generating positive output levels. By multiplying -1 to Table 1, we can obtain switching functions for a negative case.

Table 1. Switching function for generating 9-level output voltage

No. of output levels	Switching Function		Output Voltage of each inverter		Output Voltage
	SF_1	SF_2	v_x	v_y	v_{out}
4	2	2	$2E$	$2E$	$4E$
3	2	1	$2E$	E	$3E$
	1	2	E	$2E$	
2	1	1	E	E	$2E$
	0	2	0	$2E$	
1	2	0	$2E$	0	E
	0	1	0	E	
	1	0	E	0	
0	2	-1	$2E$	$-E$	0
	-1	2	$-E$	$2E$	
0	0	0	0	0	0

With the switching function, the output voltage of the proposed inverter is expressed in Eq. (6). The number of output voltage levels is given by Eq. (7).

$$v_{out} = \sum_{n=1}^{\infty} SF_n \cdot E \quad (6)$$

$$N = 4k + 1 \quad (7)$$

where k is the number of inverter modules.

If we apply Eq. (6) for two inverter modules, v_{out} can be $-4E, -3E, -2E, -E, 0, E, 2E, 3E, 4E$ by the selecting of a proper switching pattern.

From Table 1, we can consider 24 switching patterns to generate a 9-level output voltage. Among them, 12 switching patterns are shown in Fig. 4. The remainder is in symmetry. The symmetry can be obtained by multiplying -1 to the voltages. For example, in pattern 1, $v_x - v_y$ becomes v_{out} at positive polarity. On the other hand, $v_y - v_x$ becomes v_{out} for a negative.

Fig.4 shows output patterns of the upper and lower module. During the pattern selection, cross switching was avoided. That is, if the v_x indicates upper module output voltage levels with a positive polarity, then v_y should be a lower module output voltage level with a negative polarity. In the Fig. 4, switching pattern 1, 2, 10 has low switching times in a period. Other patterns have more switching times or have relatively higher dv/dt variation. We exclude the patterns in analyses and experiments. In the case of pattern 10, the power capacity on the upper module is much higher than on the lower module. This difference of power capacity on the modules can induce a gap in power capacity and lifetime in the switches. Therefore we study the switching pattern for the pattern 1 and 2 with simulation and experiment in this paper.

3. Simulations and Experiments

We performed computer-aided simulations for pattern 1 and 2 with the modified H-bridge multilevel inverter. The simulation was implemented by PSpice with consideration for pure resistive load. Fig. 5 shows simulation waveforms of pattern 1 and 2. It shows output voltage (v_{out}), terminal voltages of the upper (v_x) and the lower (v_y) inverter in sequence.

We can notice that one inverter generates a fundamental output voltage, and then another inverter adds voltages on the fundamental voltage to produce stepped waves. Consequently, the final output voltage becomes the sum of the terminal voltage of H-bridge modules. A patterning

difference of patterns 1 and 2 comes from the output voltage's switching angle difference of the upper and lower module.

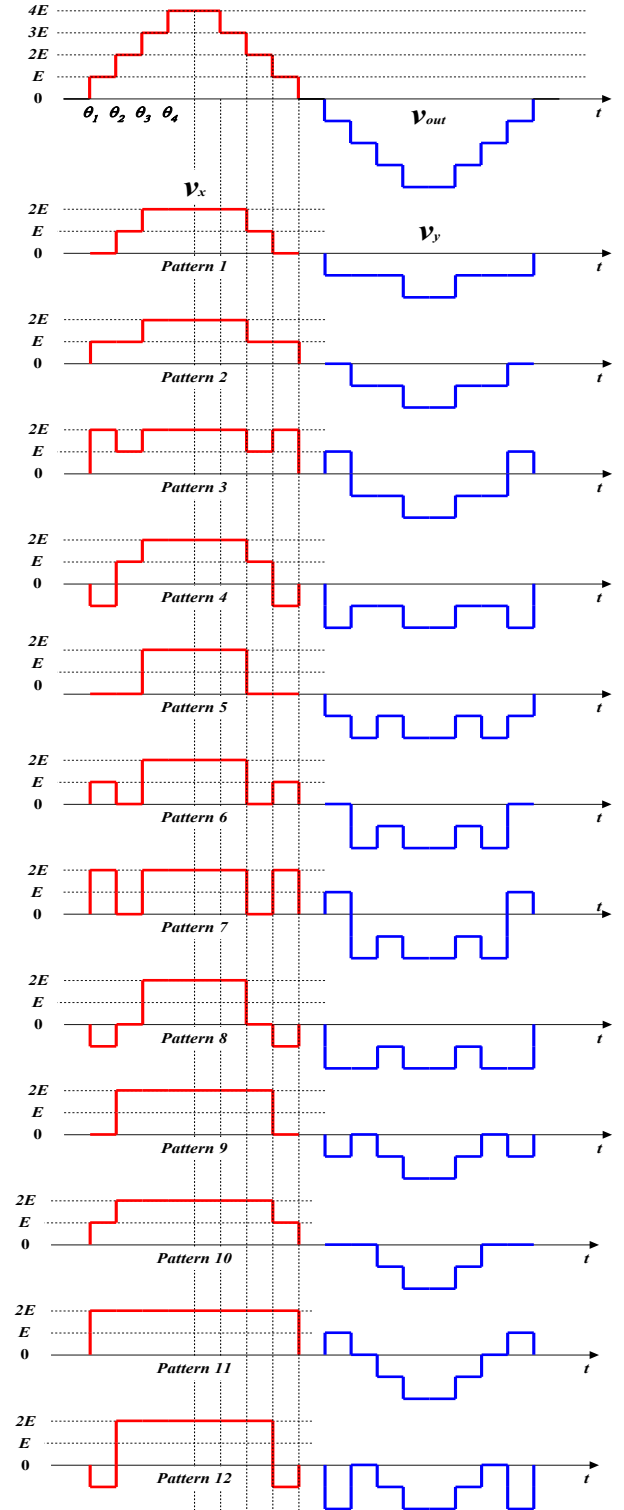


Fig. 4. Switching patterns for generating a 9-level output voltage

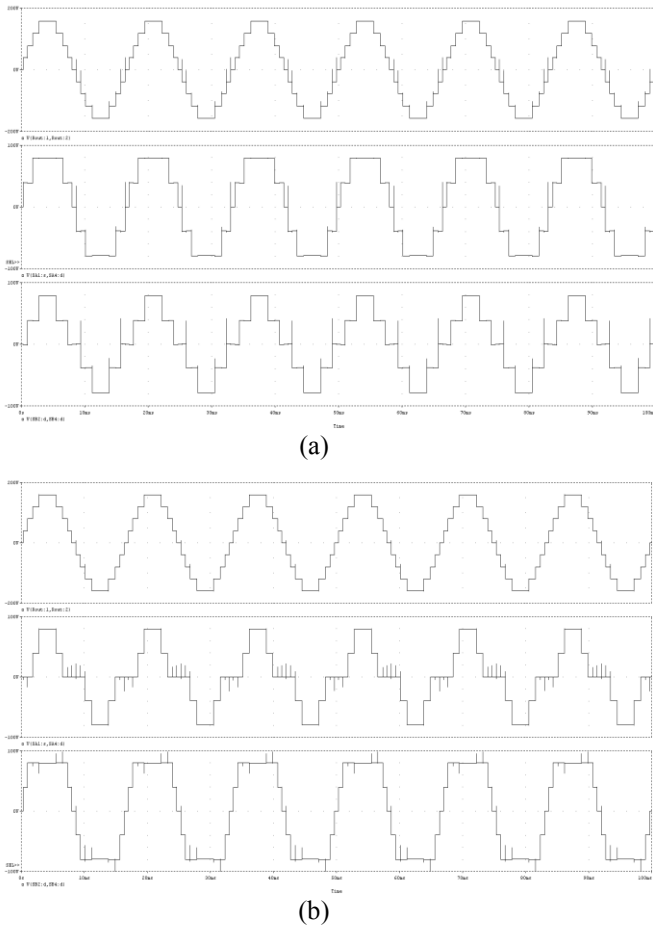


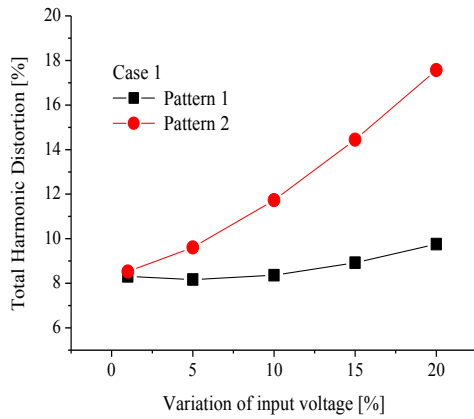
Fig. 5. Simulation waveforms of output voltage (v_{out}), output voltages of the upper inverter (v_x) and the lower inverter (v_y), (a) Pattern 1, (b) Pattern 2

If we explain the result with energy transfer, the difference of the output voltage’s area in the upper and lower modules in pattern 1 is much smaller than pattern 2’s. From Fig.5, the area of the waveform can be translated as the energy transfer from each module to the load. By simple visual comparison, we can see the area difference between upper and lower modules in pattern 1 is smaller than pattern 2. The proposed multilevel inverter requires two independent input voltage sources for the upper and lower inverter module and each input voltage source is connected with two capacitors which are in series. Therefore, there is a possibility that voltages difference on the capacitors influences the THD of the output voltages. To analyze the effect, we chose 6 cases summarized in Table 2 and executed simulations. Fig. 6 shows variations of the output voltage’s THD when voltage on the upper or lower module is increased with a constant dc 160 V total input voltage. When the upper module voltage is higher (case1), the simulation result is shown in Fig. 6(a). With the switching

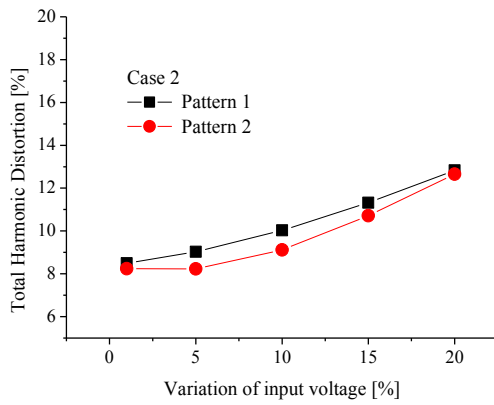
pattern 1, the THD variation of output voltage is less than 1 % as input voltage is changed. But, with switching pattern 2, the THD variation of output voltage is drastically increased by as much as 18% when input voltage is changed. If we explain the result with Fig. 5, the fundamental voltage (upper module voltage in pattern 1 and lower module voltage in pattern 2) waveform is added with the counterpart modules’ voltage (lower module voltage in pattern 1 and upper module voltage in pattern 2) waveform to produce output voltage waveform. In pattern 1, the fundamental and the added voltage have very similar waveforms. Therefore, the THD of the output voltage was little effected by the added voltage. However, in pattern 2, the fundamental voltage (lower module voltage) is a more similar waveform to the final waveform than the added voltage (upper module voltage). If we increase the voltage of the upper module voltage in pattern 2, the steps between each angle on the upper level is increased. Therefore the final waveform of the output voltage in pattern 2 has a bigger distortion than pattern 1. Fig. 6(b) shows case 2 that is higher voltage on the lower module with constant total input voltage (dc 160V). The result shows that the THD variation of output voltage is almost same in case of pattern 1 and pattern 2. Even though voltage of the lower module in the pattern is increased, the final output voltage waveform is followed by the increased lower module waveform.

Table 2. Case SUMMARY: The variation of output voltage by capacitive input voltage difference

Case	Condition
1	Higher voltage on the upper module, Total input voltage: DC 160 V
2	Higher voltage on the lower module, Total input voltage: DC 160 V
3	Higher capacitive voltage cross the upper capacitor on the upper module, Input voltage on lower module: DC 80 V
4	Higher capacitive voltage cross the lower capacitor on the upper module, Input voltage on lower module: DC 80 V
5	Higher capacitive voltage cross the upper capacitor on the lower module, Input voltage on upper module: DC 80 V
6	Higher capacitive voltage cross the lower capacitor on the lower module, Input voltage on upper module: DC 80 V



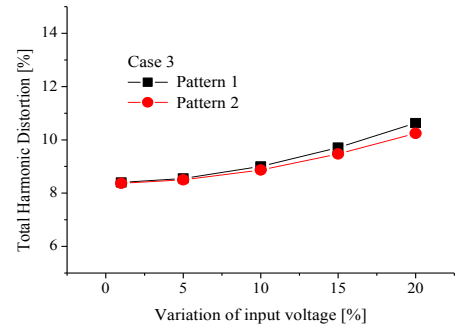
(a)



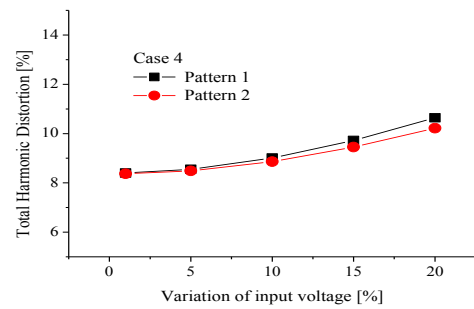
(b)

Fig. 6. Output voltage's THD variation as capacitive input voltage is varied. (a) Case 1, (b) Case 2

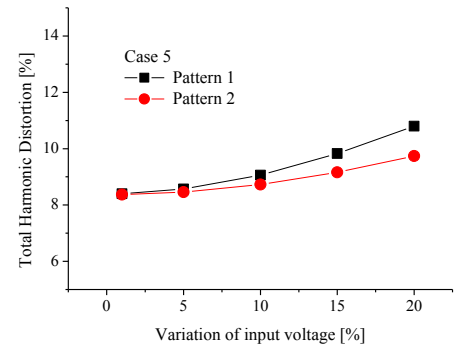
Fig. 7 describes simulation results of case 3 to case 6 in Table 2. As described in the previous result, when variation of the total input voltage is relatively big, pattern 1 has better performance in the THD variation of output voltage. However, with relatively less variation of input voltage in case 3~6, the pattern 2 has better performance in the THD variation of output voltage. From Fig. 5, lower module of pattern 2 is the dominant waveform in production of the final output voltage waveform. With the condition of case 3~6, the input voltage variation is relatively smaller than case 1 and 2. That is, the input voltage variation has little influence on the final output voltage waveform. Therefore, the output voltage waveform in pattern 2 has a similarity to the voltage waveform in the lower module which is dominant. But in pattern 1, the waveforms of the lower and upper have very similar shape.



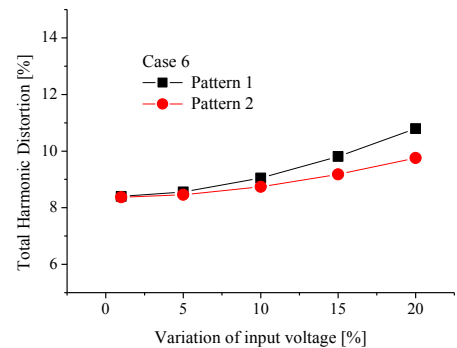
(a)



(b)



(c)



(d)

Fig. 7. Output voltage's THD variation as capacitive input voltage is varied, (a) Case 3, (b) Case 4, (c) Case 5, (d) Case 6

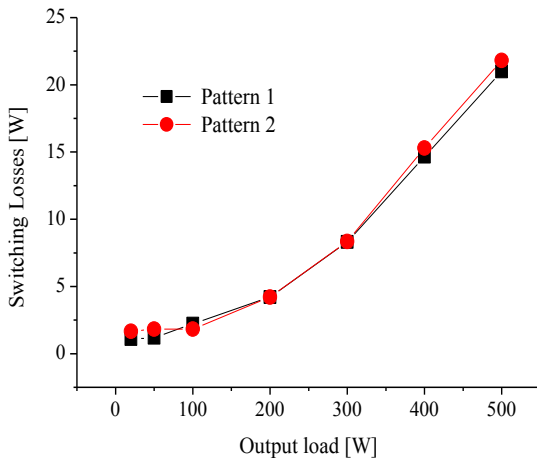
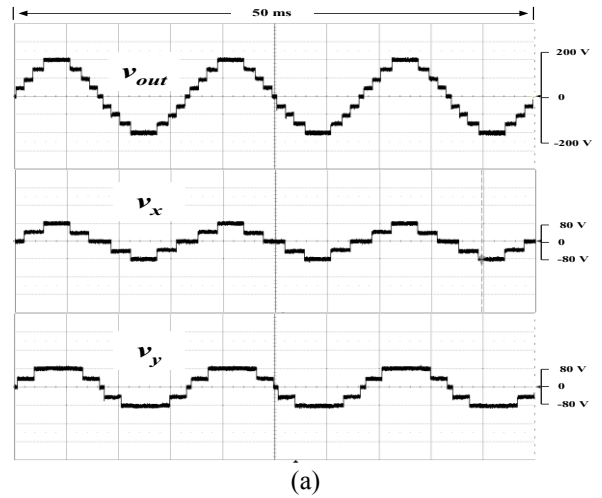


Fig. 8. Switching loss comparison of pattern 1 and 2 with output load variation

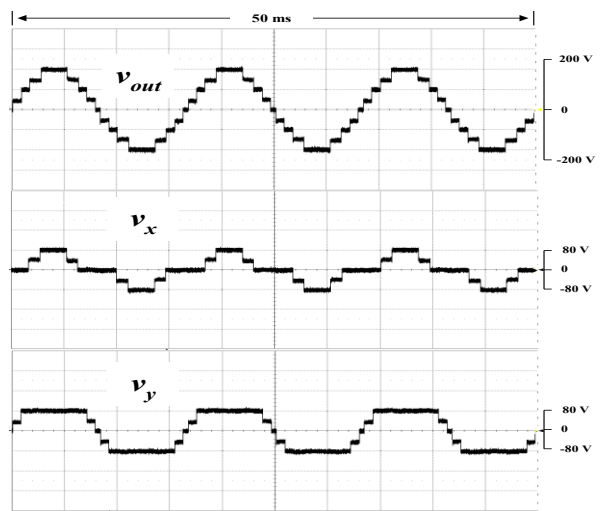
Fig. 8 describes the switching loss of pattern 1 and 2 with output load variation. The result shows that there is very similar switching loss, but it seems that the pattern 1 has a little better performance than pattern 2. This tiny difference seems to be generated by a difference of switching angle which can produce changing of the current value. From the above simulation results, switching pattern 1 is appropriate to the proposed circuit configuration because of its better performance in switching loss, and in THD characteristics of output voltage. Also the switches in pattern 1 can have longer life times since the applied power capacity on the switches has little difference. That is, the difference in pattern 1 is smaller than the one of the pattern 2.

Based on the simulation results, the proposed multilevel inverter was tested by a prototype. As a controller, AVR MEGA 128 was used. Fig. 9 shows experimental waveforms of pattern 1 and 2. It includes a reference voltage, output voltage (v_{out}), terminal voltages of the upper (v_x) and the lower (v_y) inverter in sequence. The output voltage has nine levels including a zero level. Although it is close to a sinusoidal wave, it has some lower order harmonics. So it should be improved by more H-bridge modules or output filter to obtain high quality output voltages.

Fig. 10 is an efficiency comparison of two switching patterns when it is applied for the proposed inverter with variation of output load from 0 to 500 W. The simulation and experimental results show that the switching pattern 1 has a little better performance in the efficiency.



(a)



(b)

Fig. 9. Experimental waveforms of output voltage (v_{out}), terminal voltages of the upper inverter (v_x) and the lower inverter (v_y), (a) pattern 1, (b) pattern 2

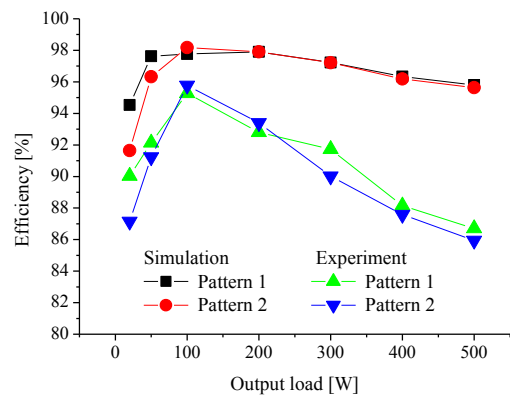


Fig. 10. Efficiency comparison with the switching patterns

With the simulation and experiment result, we can have short time to look back on complexity of the conventional multilevel inverters, i.e., diode-clamped, flying capacitor, cascaded H-bridge, and cascaded transformer based multilevel inverters. In the case of diode-clamped, a large number of clamping diodes are a severe drawback. And a lot of balancing capacitors is a disadvantage of the flying capacitor method. Among them, the isolated cascaded H-bridge multilevel inverter looks very effective to synthesize output voltage levels. It only needs a single dc input source. However, it shows low efficiency because of adopting a cascaded transformer. And it will be suffered from large size and heavy weight. Moreover, this method is not desirable for the motor drives employing VF control scheme because of the saturation of the transformer.

From the comparison, it is clear that the most outstanding advantage of the proposed multilevel inverter scheme is the elimination of the transformer in the main power stage. However, each cell of the proposed multilevel inverter requires its own isolated power supply. The provision of these isolated supplies is the main limitation in the power electronic circuit design. So the proposed multilevel inverter is suitable for photovoltaic power generating systems equipped with distributed power sources.

4. Conclusion

We proposed a cascaded H-bridge multilevel inverter using bidirectional switches to increase the number of output voltage levels with minimum devices. The circuit configuration is simple and easy to control. The operational principle and key waveforms are illustrated and analyzed. Also, we have selected two kinds of switching patterns among 24 patterns, which can produce a 9-level output voltage.

From simulations and experiments, we claim that the proposed multilevel inverter is

- (1) Economically sound for producing multilevel outputs by using bidirectional switches,
- (2) Easy for increasing the output voltage levels and output power owing to its modularity characteristic
- (3) Efficient in the power management with switching pattern 1 due to its lower THD variation, longer switch lifetime and lower switching loss.

The proposed multilevel inverters can be utilized in solar power generation, which has merits as an independent voltage source.

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