# **A Design of a PI Compensator for a Bidirectional DC-DC Converter in a DC Distributed Power System**

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**Abstract –The Voltage Bus Conditioner(VBC) is a bidirectional DC-DC converter for damping the instability and any transients of the bus voltage in a DC Distributed Power System(DPS). In this paper, a PI controller for the VBC has been designed for the frequency domain. The proposed PI controller not only dampens the bus transients, but also keeps the storage voltage level. Simulation by Matlab/Simulink and experimental results are presented for the validity of the proposed control technique.**

**Keywords**: **VBC, DPS, Voltage bus conditioner, Bidirectional converter, PI compensator, Distributed power system.**

## **1. Introduction**

DC Distributed Power System(DPS)s have been widely used for communication systems, military VHSIC systems, bulky power supply systems, aircraft/aerospace, electric/hybrid car, regenerative energy systems, etc [1]-[5]. The general structures of the DC DPS are shown in Fig. 1. Most DC DPS architectures include an intermediate distribution bus, and are configured using various combination of cascading, load splitting, and so on.



**Fig. 1.** General architecture of the DC distributed power system

In the DC DPS, the converter is required by the suitable filter due to the switching noise. Also, the converters have

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Constant Power Load (CPL) characteristics which lead to negative impedance [6]. In part, a DC DPS has a source converter and a load converter (Fig. 2).



**Fig. 2.** Typical structure of a DC DPS

In Fig. 2, instead of the load converter, the load can be connected to the motor which consists of the Permanent Magnet Synchronous Motor (PMSM) and an Induction Motor (IM). The load with Constant Power Load (CPL) characteristics causes the negative impedance characteristics which might lead to the instability of the DC DPS due to interaction of the input filter [6]-[7].

The Voltage Bus Conditioner (VBC) is a bidirectional DC-DC converter for damping bus transient [8]-[10]. VBCs can be divided as storage types that are either the inductor type or the capacitor type. A VBC with the storage inductor type has the advantage of effectively using energy. However, under steady-state, the VBC causes a high level of power loss in the inductor. Also, if the load current level is higher than the inductor current level, the VBC could not been effectively regulated [8].

A VBC with the storage capacitor type avoids the above disadvantage. However, the bus voltage is always smaller than the storage voltage level [9]. Thus, the VBC is required by the larger capacitance. To avoid the above disadvantage, a VBC with a reduced capacitor has been proposed [10].

In this paper, the VBC with a reduced capacitor confirms the effectiveness that is necessary for the PI compensator. PI control can improve the steady-state error [11]. The locations of the zero and pole have to be selected properly so that the transient response is satisfactory.

#### **2. Bidirectional DC-DC Converter**



**Fig. 3.** Topology of the Voltage Bus Conditioner

The topology of the VBC is shown in Fig 3. In Fig 3,  $V_c$ is the bus voltage, and *VST* is the storage voltage. The filter capacitor  $C_F$  is used for damping the switching ripple while both the switches are turned on or turned off. The inductor  $L_F$  limits the current between the switches.  $C_{ST}$  is the storage capacitor with the restored the energy during steady-state, D of the switching duty ratio can be defined as:

$$
D = \frac{V_{ST}}{V_{ST} + V_C} \tag{1}
$$

where, the value of the duty ratio D is determined by the switch  $Q_2$ .

#### **3. Averaged small-signal model**

The converters with switches can predict the converter characteristics from the state-space averaged model [12]. In Fig. 3,  $I_C$  has the approximately value of zero. Thus, if  $I_C = 0$ ,  $I_S$  is the same as  $I_L$ . When  $I_C$  is zero, the state-space averaged model for a VBC is shown below,

$$
\begin{bmatrix} \dot{\overline{V}}_{ST} \\ \dot{\overline{I}}_L \end{bmatrix} = \begin{bmatrix} 0 & \frac{1-D}{C_{ST}} \\ \frac{1-D}{L_F} & 0 \end{bmatrix} \begin{bmatrix} \overline{V}_{ST} \\ \overline{I}_L \end{bmatrix} + \begin{bmatrix} 0 \\ D \\ \overline{L}_F \end{bmatrix} \overline{V}_C
$$
 (2)

where the bars indicate the averaged value and D is the duty ratio of the bottom switch  $Q_2$ . The resulting linearized small signal model is:

$$
\begin{bmatrix}\n\widetilde{V}_{ST} \\
\widetilde{I}_L\n\end{bmatrix} = \frac{\begin{bmatrix}\n(1-D)D \\
L_F C_{ST} \\
D \\
E_F\n\end{bmatrix}\n\begin{bmatrix}\n\widetilde{V}_{ST} \\
\widetilde{I}_L\n\end{bmatrix} + \begin{bmatrix}\n\frac{I_L}{C_{ST}} - \frac{(1-D)V_T}{L_F C_{ST}} \\
\frac{V_T}{L_F} s + \frac{(1-D)I_L}{L_F C_{ST}}\n\end{bmatrix}\n\widetilde{D}
$$
\n
$$
s^2 + \frac{(1-D)^2}{L_F C_{ST}}\n\tag{3}
$$

where the tildes indicate small-signal quantities and s is the Laplace operator. The transfer function  $G(s)$  of  $\widetilde{I}_L$  over  $\widetilde{D}$ can be extracted from (3) as:

$$
G(s) = \frac{\widetilde{I}_L}{\widetilde{D}} = \frac{\frac{V_T}{L_F} s + \frac{(1 - D)I_L}{L_F C_{ST}}}{s^2 + \frac{(1 - D)^2}{L_F C_{ST}}}
$$
(4)

where  $\overline{V}_T$  is  $\overline{V}_C + \overline{V}_{ST}$ . Under the steady-state switching, while both of the switches are operated, the value of  $I_L$ has a negative or positive value. Thus, Right Half Plane (RHP) zero may occur. A system with a RHP zero is referred to as a non-minimum phase system [11]. Therefore, a VBC is required by the proper compensator.

#### **4. The proposed pi compensator**

#### **4.1 Transfer function of the Proportional Integration**

The Proportional Integration(PI) controller has the essentially characteristic of a Low Pass Filter(LPF), and the steady-state error of the original system improved by one order [11]. Generally, the transfer function of the PI controller is shown below,

$$
G(p) = \frac{K_p(s+P)}{s} \tag{5}
$$

where, P is P I K  $\frac{K_f}{K}$ . The phase of the PI compensator is always negative, which is not desirable to the system stability. Thus, the corner frequency P I K  $\omega = \frac{K_I}{K}$  of the PI controller should be placed as far to the left side.

## **4.2 P Gain and I Gain Calculation**

The transfer function of the uncompensated VBC is shown in Fig. 4. The initial phase is zero and the phase margin is 90 degree.



If the VBC is connected to the PI compensator, the new gain-crossover frequency  $\omega_g$  corresponding to this phase margin is found on the bode plot. The magnitude plot of the compensated transfer function must pass through the 0-dB axis. In order to obtain the desired phase, gains  $(K_P, K_I)$ of the PI controller have to be chosen properly. Thus, *K<sup>P</sup>* has to be satisfied with the equation (6),

$$
K_P = 10^{-|G_P(j\omega_g)|_{dB}/20} \t K_P < 1 \t (6)
$$

After the value of  $K_p$  is determined, it is necessary only to choose the proper value of  $K_I$  to complete the design. In this paper, the new gain-crossover frequency is chosen as 5 kHz which is fourth times smaller than the switching frequency of the system. Thus, the value of  $K_p$  that is used in the equation (6) is calculated as 0.04. For the attenuation property of PI controller, generally, the range of  $\frac{K_I}{K_P}$ *I K*  $\frac{K_I}{K_I}$  must satisfy following the requirement [11].

$$
\frac{K_I}{K_P} = \frac{\omega_g}{10 \sim 20} \qquad rad/sec \tag{7}
$$

Where,  $K_I < 70$ . Thus, the value of  $K_I$  is chosen as 40.

## **4.3 System control block**

The control block diagram of system is shown in Fig. 5. The control system consists of two control loops. The main control loop is to damp the transients or instability of the DC bus. Also, the auxiliary control loop is to maintain the storage voltage at the desired level. Due to  $K_1 \gg K_2$ , the level of the auxiliary loop can be negligible. Thus, the open-loop transfer function of the system is shown as below,



**Fig. 5.** Control block diagram of the VBC system

$$
G(s) = \frac{V_T K_1 K_P C_{ST} \cdot s^2 + (V_T P C_{ST} + (1 - D)I_L) \cdot K_P K_1 \cdot s + (1 - D)P K_P K_1 I_L}{L_F C_F \cdot s^3 + (1 - D)^2 \cdot s}
$$
\n(8)

The bode plot of equation (8) is shown in Fig. 5.



PI compensator

The VBC with PI compensator has bandwidth 5 kHz, the phase margin is 88.2 degree. The bode plot of the closedloop transfer function is shown in Fig. 5. In Fig. 5, the damping ratio  $\zeta$  is approximately 0.7 [13]. The system response has the slightly overshoot and a proper steadystate error. Thus,  $K_p$  and  $K_l$  of the PI compensator are chosen properly. The control block diagram of the overall system can be expressed in Fig. 8.



**Fig.** 7**.** Closed-loop Bode plot of the VBC with PI compensator



**Fig. 8.** Overall control blocks of the VBC system

The reference current  $I_L^*$  is estimated from DC voltage by the High-Pass Filter (HPF). In the HPF, the cut-off frequency of the HPF was chosen as 1 kHz by trial and error through simulations. The gain  $K_1$  of the main control loop was chosen as 1 and the gain  $K_2$  of the auxiliary control loop was chosen as 0.06.

# **5. Simulation and Experimental results**

The VBC with the reduced storage capacitor is connected to the DC bus in the distributed power system. The overall system has been simulated by MATLAB/Simulink. The block diagram of the system is shown in Fig 9.



**Fig. 9.** Block diagram of system using Matlab Simulink

The system parameters are shown in the Table I. The pulsed load is a resistive load which bring 10 A from the bus voltage in the steady-state.

**Table 1**. Circuit parameters of the simulation

Parameter	Symbol	Value & Unit
Bus Voltage	$\sqrt{2}$	200 V
Inductance of LC Filter		$400 \mu H$



The simulation results when the resistive load is connected are shown in Fig. 10. In Fig. 10(a), without the VBC (dotted line), the bus voltage variations are between 174 V and 224.5 V. Then the oscillation frequency occurs at approximately 1.1 kHz by the input filter  $L_S$  and  $C_S$ . With VBC (a solid line), the bus voltage variations are between 180 V and 222.5 V. Also, the oscillations are damped within around 1.5 msec. The storage voltage level is averagely maintained at 360 V (Fig. 10(c)).



**Fig. 10.** Simulation results for the resistive load

The experimental parameters are shown in the Table II.The pulsed load is a resistive load which brings around 10 A from the bus voltage in the steady-state.

Parameter	Symbol	Value & Unit
<b>Bus Voltage</b>	$V_C$	200V
Inductance of LC Filter	$L_S$	$401 \mu H$
Capacitance of LC Filter	$C_{S}$	$49.2 \mu F$
Storage capacitor of the VBC	$C_{ST}$	94.7 µF
Inductance Of the VBC	$L_F$	901 µH
Capacitance of the VBC	$C_F$	$1 \mu F$
Rated Pulsed Load		$2$ kW
Switching frequency		$20$ kHz

**Table 2.** Circuit parameters of the experiment

The experiment results when the resistive load is connected are shown in Fig. 11 (without VBC). The bus voltage variations are between 176 V and 226 V. In addition, the 1.14 kHz oscillation frequency by the input

filter components ( $L_S$  and  $C_S$ ) can be seen. In Fig. 12 (with VBC), the bus voltage variations are between 180 V and 222.5 V. The oscillations are damping within 1.5 msec. In Fig. 13, the average storage voltage is just below 360 V.



**Fig. 11. Experimental results for the resistive load without VBC**



**Fig. 12.** Experimental results for the resistive load with VBC



# **6. Conclusion**

This paper has presented the VBC system with the proposed PI compensator with constant switching frequency. The simulation by Matlab Simulink and experiment result show that the proposed approach not only effectively mitigates the bus voltage transients caused by pulsed power loads, but also contributes to the improvement of the power quality and stability of the power distribution system.

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