# New Switch-Control Technique for Multiphase Interleaved Converters with Current Sharing and Voltage Regulation

**Ponlawat Thongbuaban \*, Niphat Jantharamin \*\***

**Abstract – This paper presents a new switch-control approach for multiphase interleaved converters. Development of the proposed technique is based on control-signal generation for multi-unit synchronization. Current sharing among the switching cells and voltage regulation are achieved by means of a multi-loop control scheme regardless of changes in input voltage and load. System stability is ensured by single-pole compensation. This proposed technique is straightforward, reliable and inexpensive, and can be applied to any higher number of cells without difficulty.**

## 1. Introduction

Rapid changes in voltages and currents within a switching converter cause electromagnetic interference (EMI). The converter becomes a source of interference for other equipment in its system, and its EMI also hinders its own proper operation. The most cost-effective way of dealing with EMI is to prevent the EMI from being generated at its source [1]. EMI production can be attenuated by using an interleaving technique which cancels unwanted harmonics [2]. Another advantage of using this approach is that the converter becomes more reliable and less susceptible to its own noise [1]. The circuit diagram of an $N$-phase interleaved step-up converter is shown in Fig. 1. According to the interleaving technique, the identical parallel switching cells are operated
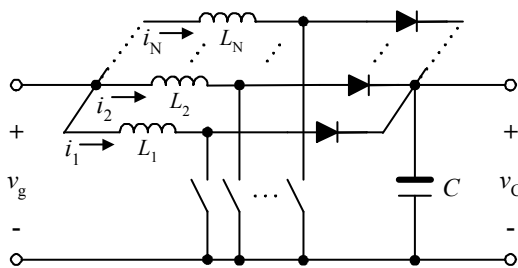


**Fig. 1.** An $N$-phase interleaved step-up converter

at the same switching frequency with a phase shift in their switching waveforms over equal fractions of a switching

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period. Interleaving $N$ cells therefore requires the cells to operate at a phase displacement of $2\pi/N$ radians with respect to one another [3]. However, as the number of switching cells of an interleaved converter is increased, the aforesaid switch control and achieving equal current sharing among the cells become more complicated [4].

## 2. Interleaved Switch-Control Techniques

Different techniques for driving power switches in interleaved converters have been discussed in the literature. Though microcontrollers have been used to generate desired switching signals, their use has several drawbacks: programming expertise of the user is required in the implementation, and cost, circuitry complexity, and difficulty of implementation increase as the number of cells increases [5].

A new integrated circuit (IC), namely UCC28220 from Texas Instruments, is used in [6] to control the switches in a two-phase step-up converter for low-voltage applications. The IC includes fast current mode controllers and gate drivers for both switching cells. It supports switching frequencies of up to 2 MHz. Slope compensation for internal current mode is also available. However, switch control with this IC becomes impossible for interleaving more than two cells. In addition, the UCC28220 is still not readily available.

A challenging application is to use an IC controller in a two-phase interleaved converter for power factor correction (PFC) [7]. However, driving a higher number of interleaved cells with this approach is troublesome due to being constrained to one IC. Moreover, the system performance

depends on this IC controller. So, fault of this IC may cause system failure.

A synchronizing circuit for paralleled converter systems, suitable for voltage regulator modules (VRM) that are designed for modern microprocessors, is proposed in [8]. Interleaved operation between the cells with automatic phase-shift operation without pre-adjustment is achieved. Use of simple analog circuits, which are easily implemented, results into the switching cells being implemented as conventional pulse-width-modulation (PWM) controllers. However, errors in the threshold voltages of the cells easily arises and cause time delays among the cells. The aforesaid errors accumulateand result in phase-shift differences between the cells.

## 3. New Switch-Control Technique

Hereby, a straightforward, reliable, and low-cost approach of switch control for multiphase interleaved converters is proposed. This technique is devised from the concept of control-signal generation for multi-unit synchronization by which all devices are operated at the same frequency. A desired switching frequency and phase shift among the parallel cells are dictated by a properly designed resistance-capacitance time constant for the PWM controllers, where trigger signals are generated by a sync pulse generator as shown in Fig. 2.
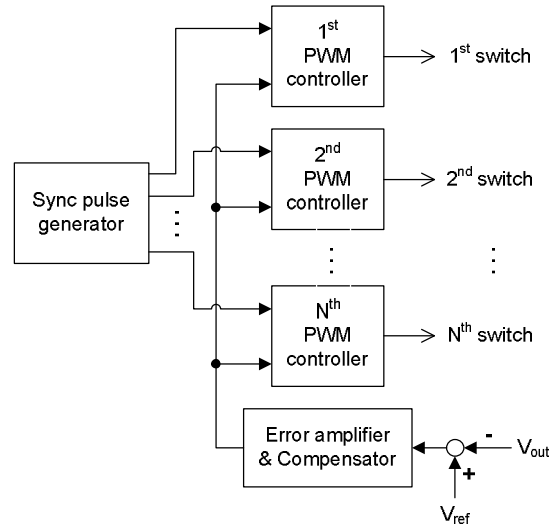


**Fig. 2.** Synchronization of switch-control signals

As an example, the proposed switch-drive circuit for a two-phase interleaved step-up converter is shown in Fig. 3. Each PWM controller of the proposed technique consists of a UC3843, which is a fixed frequency current-mode PWM controller. It is designed especially for off-line and DC-to-DC converter applications, and is designed to be used with a minimal amount of external components. This IC includes a trimmed oscillator for exact duty-cycle control, a temperature-compensated reference, a high gain error amplifier, a current sensing comparator, and a high current totem pole output for driving a power MOSFET [9].
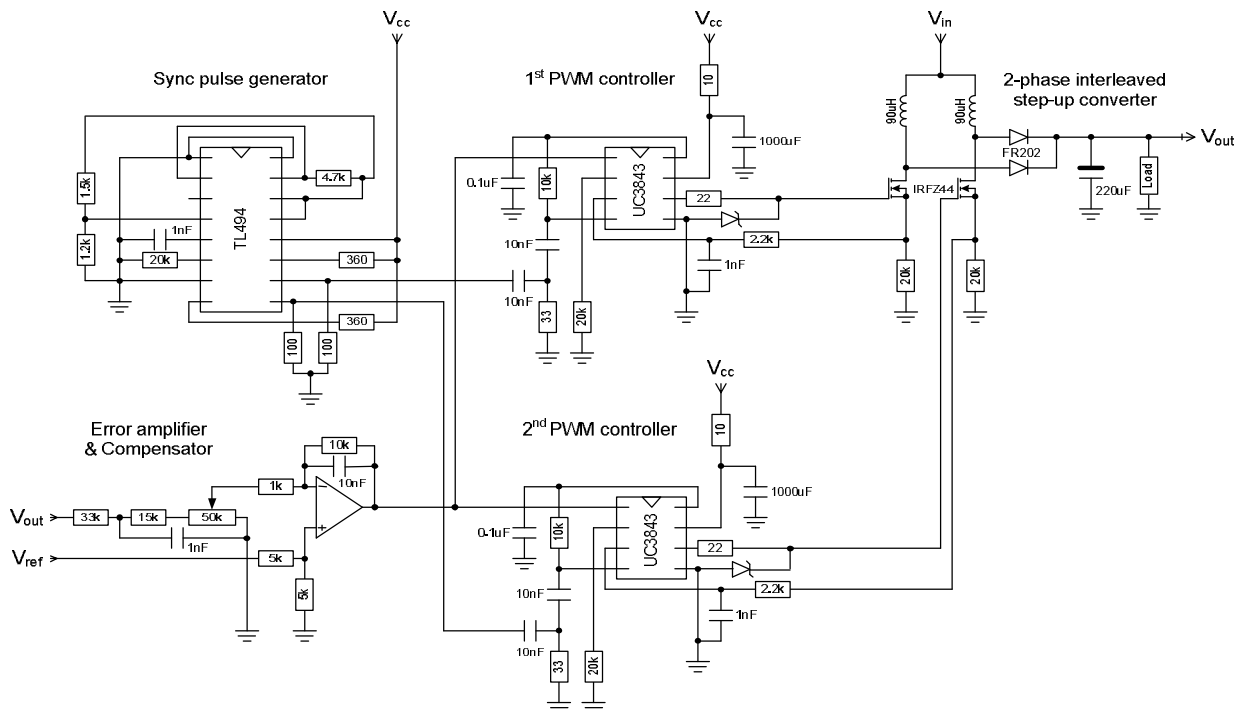


**Fig. 3.** Proposed switch-drive circuit for a two-phase interleaved step-up converter

Normally, the timing capacitor ($C_T$) is charged between two thresholds, namely the upper and lower voltage limits. When the $C_T$ initiates its charge cycle, the output of the PWM is enabled. The timing capacitor is charged until it reaches the upper voltage limit of the internal comparator. Consequently, the discharge circuitry activates and discharges $C_T$ until the lower voltage limit is met. During this discharge period, the PWM output is disabled, thus ensuring an off time for the output [9].

Even a slight difference in the resistance and capacitance values in PWM controllers results in non-identical waveforms as shown in Fig. 4. However, the aforementioned difference has no detrimental effect on the proposed switch control.

Hereby, synchronization is imposed in the following way. $C_T$ is connected to ground via a small timing resistor $R_T$. ($R_T$ and $C_T$ are connected in series). *This timing resistor $R_T$ performs as the input for the sync pulse (Fig. 5) which increases the timing-capacitor voltage above the upper voltage limit of the internal oscillator
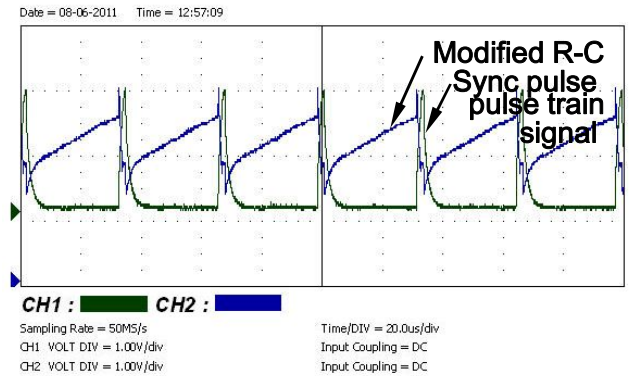
The PWM therefore operates at the frequency dictated by the combination of $R_T$ and $C_T$ until the sync pulses appear, as shown in Fig. 6.
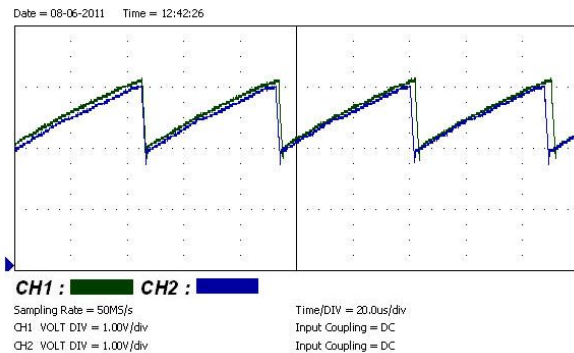


**Fig. 4.** Two R-C pulse trains generated for two PWM controllers
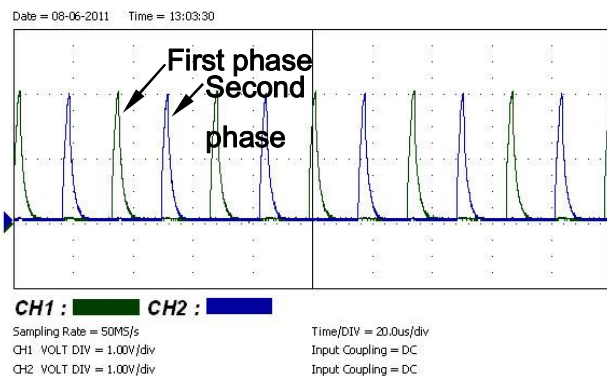


**Fig. 5.** Sync pulse trains for the two-phase interleaved converter



**Fig. 6.** Determination of switching frequency

The UC3843 oscillator is set to a lower frequency than that of the sync pulse train [9]. The modified R-C oscillator pulse trains for both phases are shown in Fig. 7 and become inputs of their corresponding PWM controllers. Following the R-C oscillator pulse inputs, the PWM controllers generate switch control signals for both switching cells with a phase shift of 180° between them, as shown in Fig. 8.
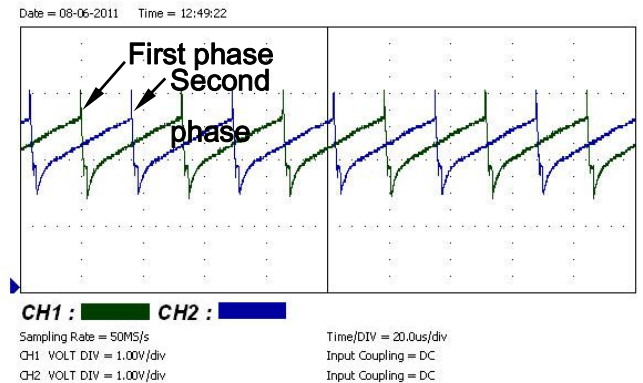


**Fig. 7.** Modified R-C pulse inputs of the PWM controllers
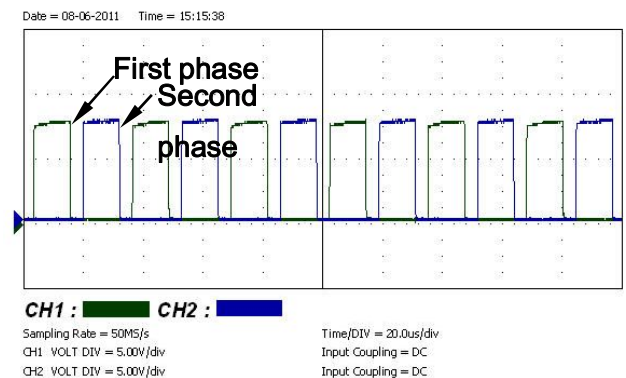


**Fig. 8.** Switch control signals for the two-phase interleaved converter

## 4. Experimental Results

The proposed control method was implemented with the two-phase interleaved step-up converter shown in Fig. 3. The inductor current waveforms of this converter are shown in Fig. 9. The experimental results show that this control scheme is viable in the continuous conduction mode (CCM) as well as the discontinuous conduction mode (DCM) of the converter.

For an interleaved converter it is necessary to ensure that each cell shares the load current equally in order to reduce the current stress of the switching devices and to improve the reliability of the converter. Hereby, current sharing and voltage regulation are achieved by means of a multi-loop control scheme in which the outer voltage loop regulates the output voltage to a desired value while the inner current loop dictates the peak inductor-current value of each switching cell. Single-pole compensation is introduced to the outer loop to ensure system stability. By means of the proposed switch-control technique, along with the aforesaid multi-loop control scheme, the output voltage of the converter is maintained regardless of the input voltage fluctuation (Fig. 10) and load disturbances (Fig. 11 and Fig. 12). In addition, the inductor currents of the converter are always distributed equally among the cells, regardless of changes in load.
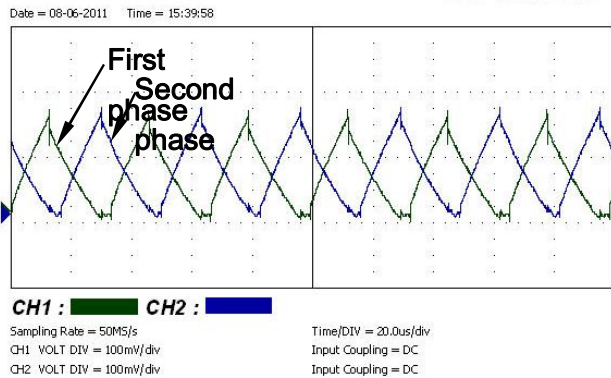


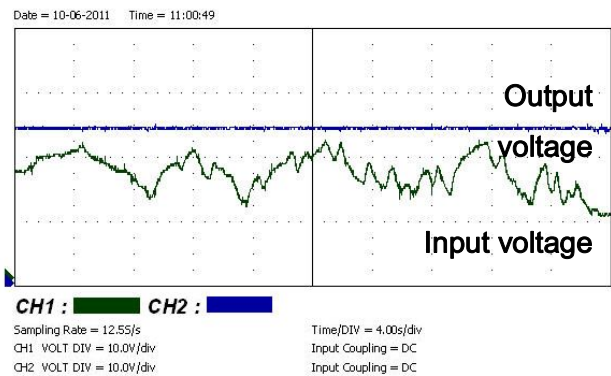**Fig. 9.** Inductor current waveforms of both switching cells in DCM



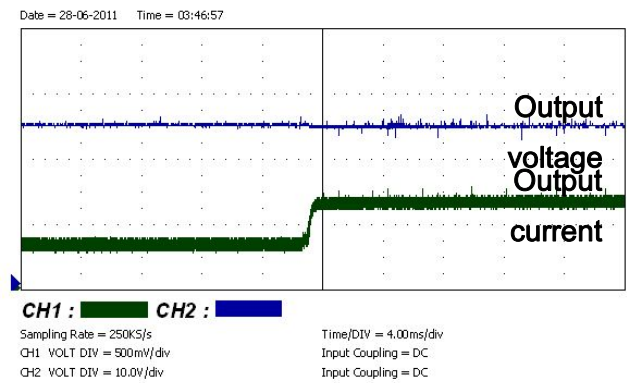**Fig. 10.** Output voltage regulation under input fluctuation



**Fig. 11.** Output voltage regulation as load resistance decreased
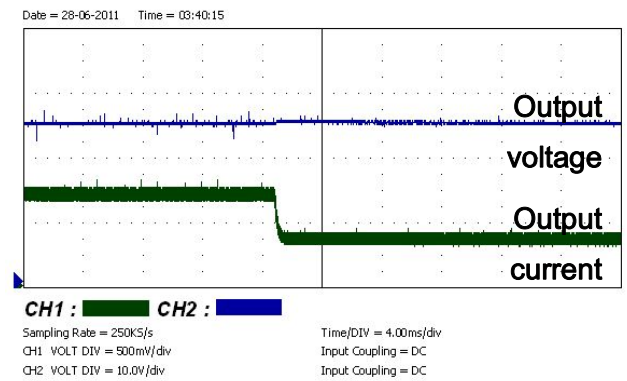


**Fig. 12.** Output voltage regulation as load resistance increased

## 5. Conclusions

In this paper, a new switch driving technique for the interleaved converter is proposed. This approach is based on control-signal generation for multi-unit synchronization. Driving the two-phase interleaved step-up converter is given as an example. Current sharing among the switching cells and voltage regulation are achieved by means of a multi-loop control scheme. They are achieved regardless of changes in input voltage or load. This switch-control approach is not affected by the slight difference between inductance values of the converter inductors. For the interleaved converter with a number of phases above two, critical constraints of frequency, duty cycle, and off time can be accurately controlled by a 555 timer. The proposed technique is straightforward, reliable and inexpensive. In particular, this approach offers switch control that is modular ach switching cell can be implemented individually, independent of the other switching cells. Therefore, this approach can be applied to any higher number of cells without difficulty.

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