JPE 12-3-9

http://dx.doi.org/10.6113/JPE.2012.12.3.458

DC-Link Active Power Filter for High-Power Single-Phase PWM Converters

Hongbo Li†, Kai Zhang*, and Hui Zhao*

†*School of Electrical and Electronic Eng., Huazhong University of Science and Technology, Wuhan, China

Abstract

Single phase converters suffer from ripple power pulsating at twice the line frequency. The ripple power is usually absorbed by a bulky capacitor bank and/or a dedicative LC resonant link, resulting in a low power density and a high cost. An alternative solution is using a dc link active power filter (APF) to direct the pulsating power into another energy-storage component. The main dc link filter capacitor can then be reduced substantially. Based on a mainstream dc APF topology, this paper proposed a new control strategy incorporating both dual-loop control and repetitive control. The circuit parameter design is also re-examined from a control point of view. The proposed APF scheme has better control performance, and is more suited for high power applications since it works in CCM and with a low switching frequency.

Key words: Capacitive energy-storage, DC link active power filter, Power density, Ripple power, single-phase PWM converter

I. INTRODUCTION

Single-phase PWM rectifiers and inverters can be found in many power electronic systems, such as small-volume UPSs, grid-connected photovoltaic (PV) generation systems, multi-level converters based on H-bridge modules, ac-fed railway traction drives, fault-tolerant multi-phase ac drives, etc. A significant disadvantage of single phase converters is the existence of second-order ripple power. If the dc link is connected with a PV panel or a battery, the ripple power will reduce the efficiency of the PV generation or cause over-heating of the battery [1]. A fluctuating dc bus voltage also acts on the ac side through the beat phenomenon [2]. For a grid connected converter, this means a third-order harmonic in the grid current. For an ac-fed railway traction drive, this means beat components in the stator current of the ac machine, the frequencies of which are the sum and difference of the dc-link ripple frequency and the output frequency. The beat currents bring extra power losses, temperature increases, torque pulsations, and audible noise [3], [4].

Usually a large dc capacitor bank and/or an LC resonant circuit are installed in a dc link to absorb the ripple power [5], [6], as shown in Fig. 1(a). If only capacitors are used, they have to be aluminum electrolytic capacitors since the capacitance has to be very large. The short lifetime of aluminum electrolytic capacitors then becomes a bottleneck in terms of the reliability of a whole system. Adding an LC resonant branch can lower the requirements for the main capacitor by providing a short circuit for the ripple power. However, since the resonance frequency is low, the size and weight of the LC branch is considerable. Furthermore, an LC resonant circuit is sensitive to parameter drift and frequency deviation [7], thus necessitating a conservative design for the main capacitor.

To overcome the shortcomings of passive filters, various active power filter (APF) schemes have been proposed. The basic idea is to divert the ripple power into another capacitor or an inductor, which can be much smaller since it permits heavy fluctuating of the voltage and/or current. As a result, film type capacitors can be used, which have a much longer lifetime than the electrolytic ones. Some APF topologies are shown in Fig. 1(b)-(e).

The APF in Fig. 1(b) consists of an energy-storage inductor and a unidirectional bridge circuit [8]. In Fig. 1(c) a third leg is added and an energy storage inductor is connected between the midpoints of the added leg and one of the original H-bridge rectifier [9]. While inductors are superior to capacitors in terms of reliability, they are inferior in terms of energy density and weight. The power loss of inductors is also much higher than that of capacitors when working with switching converters.

In [10] and [11], a pair of capacitors at the grid side is used

Manuscript received Aug. 12, 2011; revised Mar. 15, 2012
Recommended for publication by Associate Editor Yong-Sug Suh.

†Corresponding Author: lihongbo3457@163.com
Tel: +86-027-87553354, Huazhong University of Science and Technology
*School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, China

to store the ripple energy, as shown in Fig. 1(d). A drawback of this method is the increased current stresses on the two rectifier legs due to the added circuitry [12]. Another capacitor-based topology [12]-[14] is shown in Fig. 1(e). The APF part consists of an energy storage capacitor, a smoothing inductor, and a half-bridge power module. The circuit is simple, easy to implement, and it avoids the abovementioned current stress problem. This circuit will be the focus of this research.

Papers [12]-[14] illustrated the basic principles and proposed some control techniques for this APF circuit. However, there is still much room left for improvement. Proportional control is adopted in [12], which is prone to steady-state errors. Also the calculation of the current command is overly simplified, which may bring fourth order harmonics in the dc link. In [13] the calculation of the voltage/current command is made more rigorous, but the current control is basically an open-loop, which is sensitive to disturbances.

Apart from control performance, another problem with present research is that the methods are mainly restricted to low power applications where a high switching frequency is available. In [14] the circuit even works in discontinuous current mode (DCM), which is not an option for high power applications.

This paper deals with the control techniques of dc APF for high power applications (e.g. ac-fed railway traction drives), where the APF operates in continuous current mode (CCM) with a low switching frequency. An advanced closed-loop control scheme is proposed. The circuit design process is also re-examined from a control point of view.

II. BASIC RELATIONS

Assume the grid voltage v_s and ac input current i_s to be purely sinusoidal, that is:

$$v_S = V_S \sin(\omega t) \tag{1}$$

$$i_S = I_S \sin(\omega t - \theta)\ , \tag{2}$$

where V_s and I_s are the peak values of the gird voltage and the input current, and θ is the phase angle between them. In general, the input power factor is controlled high enough, so that θ is close to zero.

From (2), the voltage drop of the input inductor can be expressed as:

$$v_L = L_S \frac{di_S}{dt} = \omega L_S I_S \cos(\omega t - \theta)\ . \tag{3}$$

The input power of the rectifier can be obtained as:

$$p_{in} = v_s i_s - v_L i_s = \frac{V_S I_S}{2}\cos\theta - [\frac{V_S I_S}{2}\cos(2\omega t - \theta) + \frac{\omega L_S {I_s}^2}{2}\sin(2\omega t - 2\theta)]\ . \tag{4}$$

As shown in (4), the constant part and the ripple part of the input power are respectively shown as:

$$P_o = \frac{V_S I_S}{2}\cos\theta \tag{5}$$

$$p_r = -[\frac{V_S I_S}{2}\cos(2\omega t - \theta) + \frac{\omega L_S I_S^2}{2}\sin(2\omega t - 2\theta)]\ . \tag{6}$$

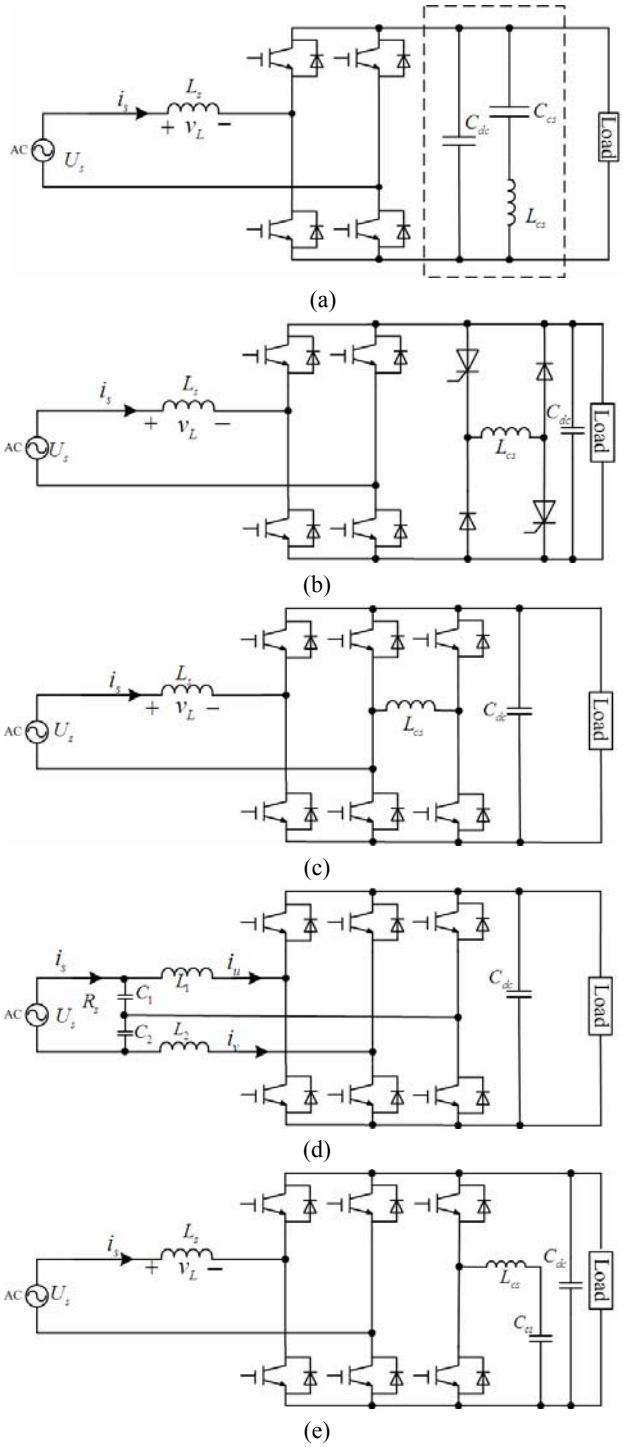


Fig. 1. Different topologies of dc APFs.

Equation (6) clearly shows the contribution of the ripple power from the input inductor. Substituting (5) into (6), the ripple power can be expressed as:

$$\begin{aligned} p_r &= -P_o\sqrt{1+(\frac{2\omega P_o}{V_s^2}L_s\tan^2\theta-\tan\theta+\frac{2\omega P_o}{V_s^2}L_s)^2} \\ &\quad .\sin(2\omega t-2\theta+\psi) \\ &= P_{r\_peak}\cos(2\omega t-2\theta+\psi+\frac{\pi}{2}) \end{aligned} \quad , \quad (7)$$

where:

$\psi=\frac{2V_s^2\cos^2\theta}{4\omega L_s P_o-V_s^2\sin(2\theta)}$, and P_{r_peak} is the magnitude of the ripple power.

A. Traditional passive filters

If all of the ripple power is to be absorbed by the dc link capacitor, the following is obtained:

$$C\frac{dv_{dc}}{dt}v_{dc}=P_{r\_peak}\cos(2\omega t-2\theta+\psi+\frac{\pi}{2}) \quad . \quad (8)$$

The needed capacitance can be calculated as:

$$C=\frac{P_{r\_peak}}{2\omega V_{dc}\Delta V_{dc}}, \quad (9)$$

where V_{dc} is the arithmetic mean value of the dc link voltage and ΔV_{dc} is the allowed magnitude of the dc link voltage ripple. According to (9), a very large capacitance will be needed.

If an LC resonant branch is added, which is tuned at twice the line frequency, the ripple power should be totally bypassed and the main capacitor only has to filter out the switching harmonics. However, there will always be parameter drift and frequency deviation to be considered.

Fig. 2 shows the dc link of the single phase converter considering only the (second-order) ripple frequency. The ripple component of the dc link voltage u_{dc2}, the LC circuit current i_{LC2}, and the dc capacitor current i_{d2} can be calculated as:

$$\begin{aligned} u_{dc2} &= i_{dc2}Z=i_{dc2}\frac{\alpha}{\alpha/Z_L+j\omega_2(\alpha C_{dc}+C_2)} \\ &\overset{(\alpha<<Z_L)}{\approx} i_{dc2}\frac{\alpha}{j\omega_2(\alpha C_{dc}+C_2)} \end{aligned} \quad (10)$$

$$i_{LC2}=\frac{u_{dc2}}{Z_2}=\frac{C_2}{\alpha C_{dc}+C_2}i_{dc2} \quad (11)$$

$$i_{d2}=\frac{u_{dc2}}{Z_{dc}}=\frac{\alpha C_{dc}}{\alpha C_{dc}+C_2}i_{dc2}, \quad (12)$$

where:

$\omega_2=2\omega$, $\alpha=1-\omega_2^2L_2C_2$, $Z_{dc}=\frac{1}{j\omega_2 C_{dc}}$

$Z_2=j\omega_2L_2+\frac{1}{j\omega_2C_2}=\frac{1-\omega_2^2L_2C_2}{j\omega_2C_2}$, $Z=Z_{dc}//Z_2//Z_L$.

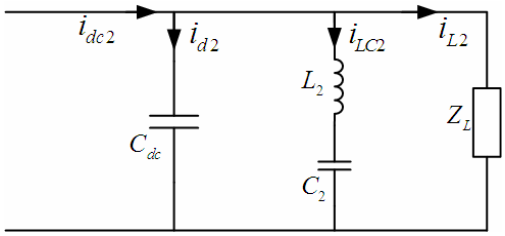


Fig. 2. Equivalent circuit of the dc link.

α depends on the relationship between the LC resonant frequency and the actual ripple frequency. It is a good indication of a mismatch due to LC parameter drift and line frequency deviation. Ideally α and u_{dc2} are zero. When the ripple frequency is lower than the resonance frequency, α is positive and the LC branch becomes capacitive. The input ripple current i_{dc2} will be shared between the main capacitor and the LC branch. When the ripple frequency is higher than the resonance frequency, α is negative and the LC branch acts like an inductor. Then there will be circulating current between the main capacitor and the LC branch.

Taking the above considerations into account, the main capacitor cannot be reduced too much even with an LC branch.

B. Active filters

For the active filter shown in Fig. 1(e), the aim is to divert the ripple power into the energy storage capacitor C_{cs}. In other words, the voltage/current of the capacitor should be controlled such that its reactive power equals the ripple power flowing into the dc link.

The simplest way to do this is to control the capacitor voltage as a dc component superimposed with a second-order component [12]. The capacitor current and voltage can be expressed as:

$$i_{cs}=I_{cs}\sin(2\omega t+\beta) \quad (13)$$

$$u_{cs}=V_b+\frac{1}{C_{cs}}\int i_{cs}dt=V_b-\frac{1}{2\omega C_{cs}}I_{cs}\cos(2\omega t+\beta), \quad (14)$$

where V_b is the dc component.

Then the power of the APF can be calculated as:

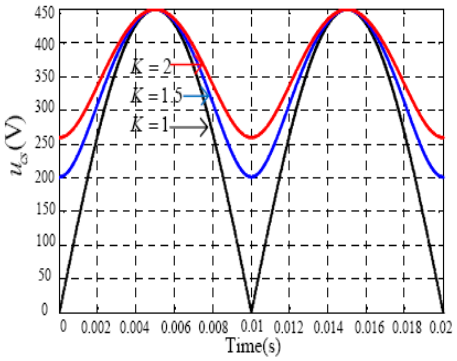
$$\begin{aligned} p_{APF} &= i_{cs}(L_{cs}\frac{di_{cs}}{dt}+u_{cs})=V_bI_{cs}\sin(2\omega t+\beta) \\ &\quad +(\omega L_{cs}-\frac{1}{4\omega C_{cs}})I_{cs}^2\sin(4\omega t+2\beta) \end{aligned} \quad . \quad (15)$$

The second-order component of p_{APF} is used to compensate the ripple power, therefore:

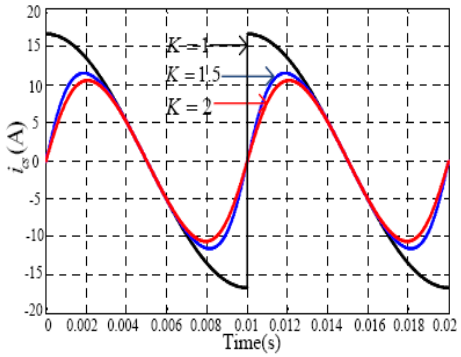
$$V_bI_{cs}=P_{r\_peak} \quad (16)$$

$$\beta=\pi-2\theta+\psi \quad . \quad (17)$$

From (15), it can be seen that p_{APF} also contains a



(a) Capacitor voltage.



(b) Capacitor current.

Fig. 3. Waveforms of capacitor voltage and current as functions of *K*.

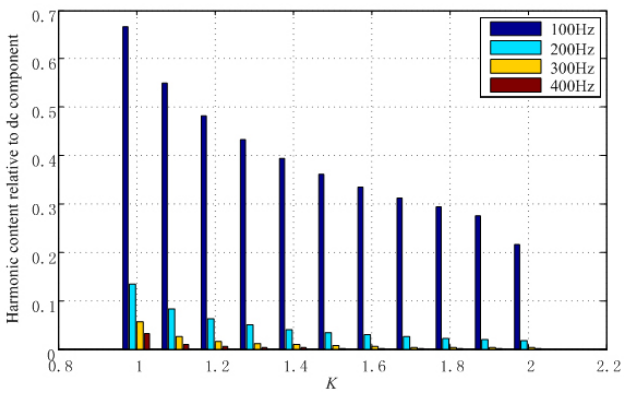


Fig. 4. Harmonic content of u_{cs}^* with different *K* (relative to dc component).

fourth-order component, which means that fourth-order harmonics will be injected into the dc link.

To overcome this problem, the voltage and current commands should be refined. Assuming that all of the ripple power is stored in the capacitor, the instantaneous power can be expressed as:

$$u_{cs}C_{cs}\frac{du_{cs}}{dt} = P_{r\_peak}\cos(2\omega t - 2\theta + \psi + \frac{\pi}{2}). \tag{18}$$

Solving (18) yields the expressions of the capacitor voltage and current as:

$$u_{cs} = \sqrt{\frac{P_{r\_peak}}{C_{cs}\omega}[K - \sin(2\omega t - 2\theta + \psi + \frac{\pi}{2})]} \tag{19}$$

$$i_{cs} = \frac{P_{r\_reak}\cos(2\omega t - 2\theta + \psi + \frac{\pi}{2})}{\sqrt{\frac{P_{r\_peak}}{C_{cs}\omega}[K - \sin(2\omega t - 2\theta + \psi + \frac{\pi}{2})]}}, \tag{20}$$

where $K(K\geq 1)$ is a constant generated during the integration of (18). Physically speaking, *K* relates to the dc component of u_{cs}. Fig. 3 depicts the waveforms of the capacitor voltage and current with different values of *K*. It can be seen that when a higher *K* is selected, the dc component of the capacitor voltage increases while the fluctuating range decreases.

TABLE I

PARAMETERS OF SINGLE PHASE PWM RECTIFIER

Grid voltage	V_s(RMS)	220 V
Grid frequency	f	50 Hz
Input inductor	L	7 mH
Dc bus voltage	V_{dc}	450 V
Dc Capacitor	C_{dc}	220 μF
Output power	P_o	3.5 kW
Switching frequency	f_s	2 kHz

III. PARAMETER DESIGN OF THE ACTIVE FILTER

The design is based on a reduced-scale test setup for an ac-fed traction drive. Table I gives the key parameters of the system. The switching frequency of the APF circuit is 2 kHz, which is the same as the rectifier.

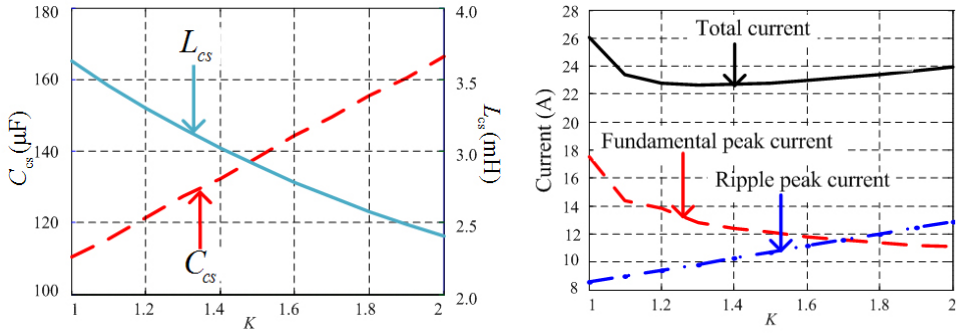
A. Determination of LC parameters

From a control point of view, an important performance index is the bandwidth of the system, which is directly related to the resonance frequency ω_{cs} of the LC circuit. To suppress the switching harmonics, ω_{cs} should be kept low，usually between one-tenth to one-fifth of the switching frequency, or 200-400 Hz in this case. ω_{cs} is finally chosen as 250 Hz. The aim is to achieve the best harmonic suppression while keeping the closed-loop bandwidth no less than 200 Hz, which (as can be seen in Section III-B) is a minimal requirement for good command following. Note that when compared with a passive LC branch tuned at 100 Hz, the LC product is reduced to 16%.

From (19), the capacitance C_{cs} can be determined as:

$$C_{cs} = \frac{(K+1)P_{r\_peak}}{\omega V_{dc}^2}. \tag{21}$$

To get full usage of the dc link voltage, the maximum value of the capacitor voltage u_{cs} can be chosen close to the value of u_{dc}. The selection of *K* will be discussed in Section III-B.



(a) (b)

Fig. 5. LC parameters (a) and current (b) of APF with different K at fixed resonance frequency 250Hz.

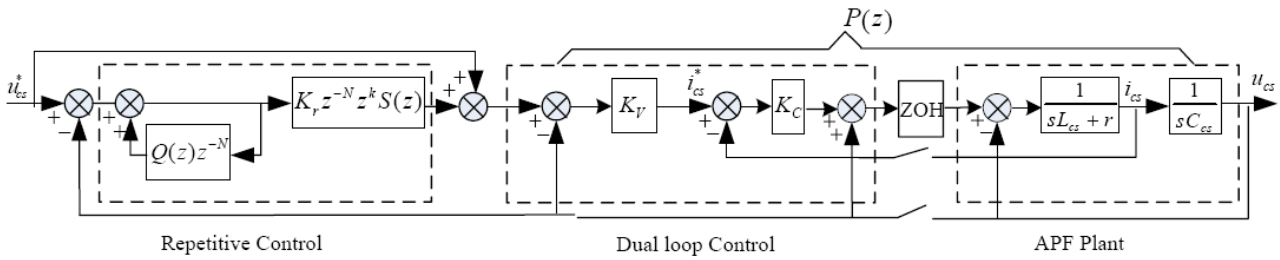


Fig. 6. Control system overview.

By knowing C_{cs} and the resonance frequency ω_{cs}, the inductance L_{cs} can be determined as:

$$L_{cs} = \frac{1}{\omega_{cs}^2 C_{cs}}. \tag{22}$$

In this paper, the APF works in CCM, so the inductor should also satisfy the following:

$$L_{cs} \geq \frac{(V_{dc}u_{cs} - u_{cs}^2)}{2V_{dc}\overline{i_{cs\min}}f_{cs}}, \tag{23}$$

where $\overline{i_{cs\min}}$ is the minimum average value of i_{cs} in a switching period.

B. *Discussion of K*

As demonstrated by (21), K determines C_{cs}. To minimize the requirement on the capacitance, K=1 should be selected. Fig. 3 shows that the capacitor voltage can reach down to zero in this case, which indicates the maximum utilization of the capacitor. However, such a voltage waveform is difficult for the controller to follow since it contains too many high frequency components.

Fig. 4 gives the FFT analysis of the capacitor voltage with different values of K. According to Fig. 4, harmonic components over 200 Hz decrease rapidly with K. Considering the limited bandwidth of the system (200 Hz), K should be made high enough so that the harmonic contents over 200 Hz are negligible. It becomes evident that the selection of K will be a compromise between a high power density and good command following.

Another significant impact of K is on the current stresses of the power devices. Fig. 5(a) gives the LC parameters of the APF with different selections of K at a fixed resonance frequency of 250 Hz. Fig. 5(b) gives the peak value of the fundamental current i_{cs}, the peak value of the switching ripple current, and the sum of them, which is a good indication of the maximum current flowing through the power devices. It can be seen that when K increases, L_{cs} gets smaller as a result of the increased capacitance. While an increased C_{cs} lowers the fundamental component of the current, a smaller L_{cs} brings a higher switching ripple component. The minimum total stress of the power devices occurs at K = 1.4.

Taking all of the factors mentioned above into consideration, K is finally selected as 1.4. The corresponding capacitance C_{cs} and the inductance L_{cs} are 130μF and 3mH, respectively.

IV. CONTROL SYSTEM DESIGN

The APF can successfully compensate the ripple power if either the capacitor voltage is controlled according to (19) or the capacitor current is controlled according to (20). Due to the high pass feature of the capacitor, the current command given by (20) contains heavier high frequency components, which are difficult to follow given the limited switching frequency. Therefore, the capacitor voltage is selected as a control object.

Taking the bridge midpoint voltage as an input, the transfer function of the capacitor voltage is:

$$G_c(s) = \frac{1}{L_{cs}C_{cs}s^2 + rC_{cs}s + 1} \tag{24}$$

in which r represents the equivalent resistance in the circuit. It includes the ESRs of the capacitor and the inductor, and also the dead time effect, which offers some damping. Usually r is quite small, rendering the circuit prone to oscillations.

Due to the fact that the voltage command contains harmonics, the best way to achieve high steady-state accuracy with a limited bandwidth seems to be a repetitive control [15]-[19]. Since repetitive control does not perform well for plants with a bad transient response, a dual-loop control is added in the first place. The latter achieves active damping of the circuit and curbs the oscillation tendency. Fig. 6 shows the control system overview.

A. Dual-loop Control

The dual loop control structure consists of a capacitor current inner loop and a capacitor voltage outer loop.

1. Current-loop design

With feed-forwarding of the capacitor voltage, the plant model of the inner current loop can be simplified as the first order element in Fig. 6. Taking the zero-order hold (ZOH) into account, the discrete transfer function is:

$$G_I(z) = Z\left(\frac{1-e^{-Ts}}{s}\frac{1}{L_{cs}s+r}\right) = \frac{1-e^{-\frac{rT}{L}}}{r\left(z-e^{-\frac{rT}{L}}\right)}, \tag{25}$$

where T is the sample time.

If proportional control is used, the closed-loop characteristic equation is:

$$z - e^{-\frac{rT}{L}} + K_C\frac{\left(1-e^{-\frac{rT}{L}}\right)}{r} = 0, \tag{26}$$

where K_C is the gain of the inner-loop controller.

Setting $z = 0$ for deadbeat effect, K_C can be derived as:

$$K_C = \frac{re^{-\frac{rT}{L}}}{1-e^{-\frac{rT}{L}}}. \tag{27}$$

2. Voltage-loop design

When compared with the current loop, the response of the voltage loop is much slower. Seen from the point of view of the voltage controller, the current loop can be considered as a unity gain element, which means that the current command is realized instantly.

To achieve the deadbeat effect, the voltage-loop controller gain can be derived as:

$$K_V = \frac{C_{cs}}{T}. \tag{28}$$

Fig. 7 gives the frequency response of an APF with the dual-loop control. When compared with the open-loop response, the dual-loop control eliminated the resonant peak, enlarged the phase margin, and extended the bandwidth. This makes repetitive control of the APF much easier.

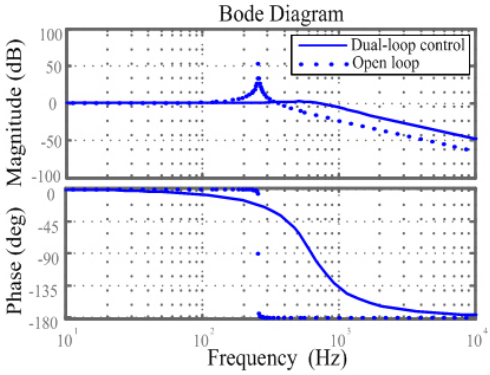


Fig. 7. Frequency response of APF.

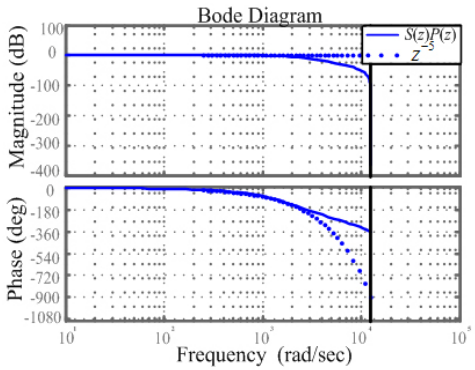


Fig. 8. Design of the time advance unit.

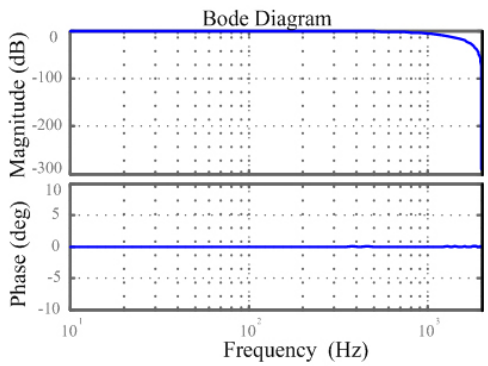


Fig. 9. Bode diagram of *Q(z)*.

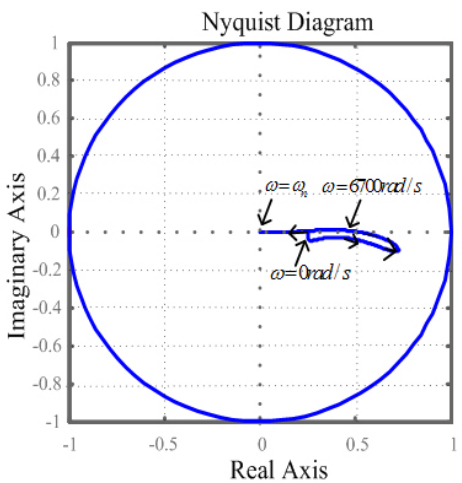
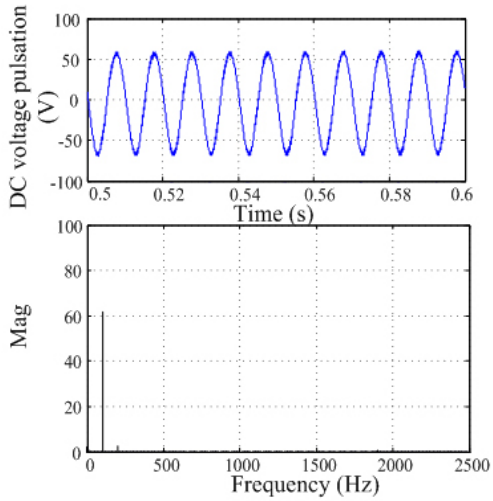
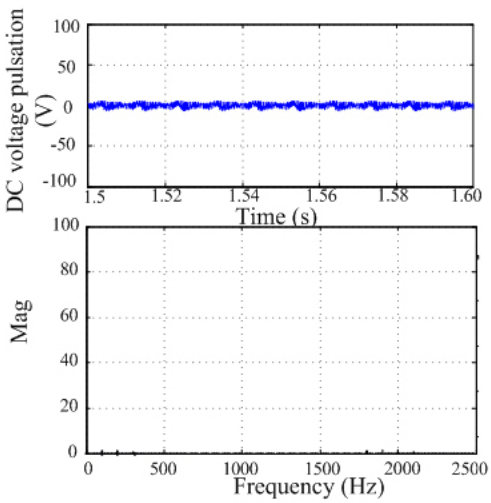


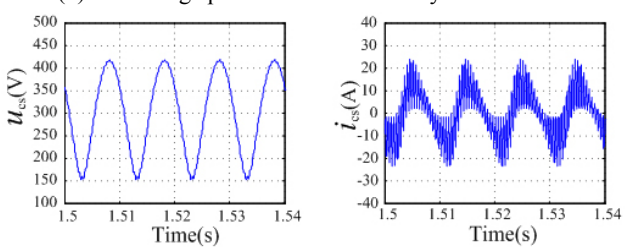
Fig. 10. Verification of stability.



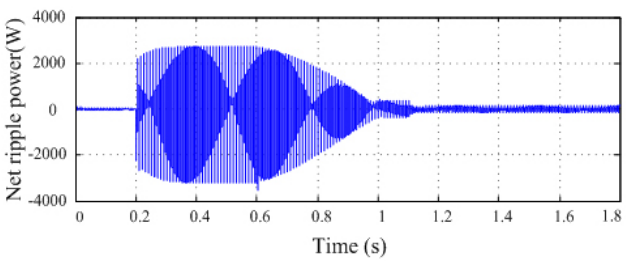
(a) DC voltage pulsation and FFT analysis without APF.



(b) DC voltage pulsation and FFT analysis with APF.



(c) APF capacitor voltage and current waveforms.



(d) Net ripple power into the dc link.

Fig. 11. Simulation results of the proposed control strategy.

B. Repetitive Control

With a low switching frequency, the assumptions (e.g. the dynamics of the current loop being negligible) taken in the dual-loop controller design do not hold well. As a result, the steady-state error tends to increase. Repetitive control can help reduce this steady-state error due to its repetitive nature.

As shown in Fig. 6, the core of the repetitive controller is the $Q(z)z^{-N}$ part, which integrates the error in a cycle-by-cycle manner. N denotes the number of samples within one fundamental cycle (i.e. the 10 ms ripple cycle). The filter $Q(z)$ improves stability by suppressing the integration of the high frequency content in the error. $P(z)$ represents the plant, i.e. the APF under dual-loop control. With the improved frequency response of $P(z)$, as already shown in Fig. (7), the compensator $S(z)$ can be simply chosen as a second-order filter to give extra high frequency attenuation.

The time advance unit z^k, in conjunction with the period delay unit z^{-N}, advances the repetitive compensation by k steps in the next ripple cycle, so that the time delay within the control loop can be compensated. The gain K_r allows for a tradeoff between the stability margin and the error convergence speed.

$S(z)$ is chosen as a critically-damped second order filter with a natural frequency of 2200rad/s. It is found that z^5 can cancel out the time delay of $S(z)P(z)$ up to 300 Hz, as shown in Fig. 8.

A sufficient condition for system stability based on the small gain theorem is:

$$\left| m(e^{j\varpi T}) = Q(e^{j\varpi T}) - L(e^{j\varpi T}) \right| < 1, \varpi \in [0, \pi/T], \quad (29)$$

where $L(e^{j\varpi T}) = K_r e^{j\varpi kT} S(e^{j\varpi T}) P(e^{j\varpi T})$.

The filter $Q(z)$ is chosen as:

$$Q(z) = \frac{z + 2 + z^{-1}}{4}. \quad (30)$$

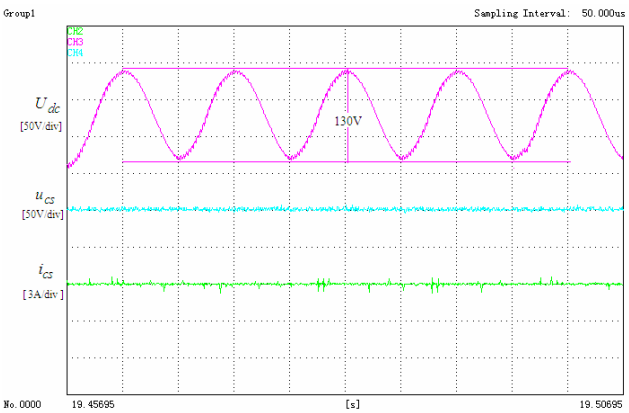
A Bode diagram is shown in Fig. 9. When compared with conventional low pass filters, it has a zero phase shift, and its low frequency gains are closer to 1, which is better for reducing the steady-state error.

Fig. 10 is the locus of $m(e^{j\omega T})$ with K_r = 0.75. The locus remains in the unity circle, indicating that the system is stable.

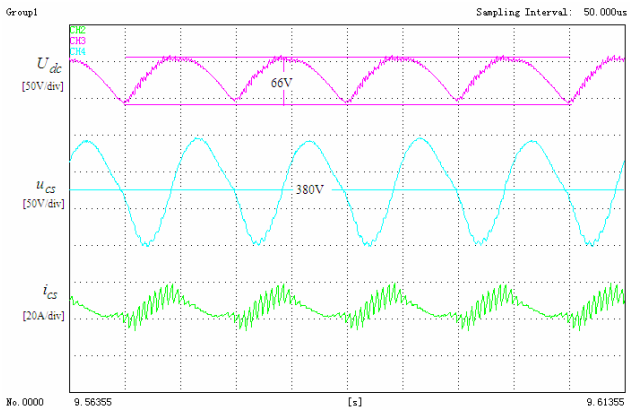
C . Simulation results

Fig. 11 presents the ripple suppression effect using the proposed control strategy. Fig. 11(a) and 11(b) give the dc link voltage pulsation with and without the APF, respectively. From the FFT analysis of the dc link voltage, the 100 Hz ripple component is found to have been reduced from 61.09V to 1.44V with the APF. The 200 Hz component is also reduced from 2.51V to 1.06V. Fig. 11(c) shows the steady-state waveforms of the APF capacitor voltage and current, which are in compliance with Fig. 3.

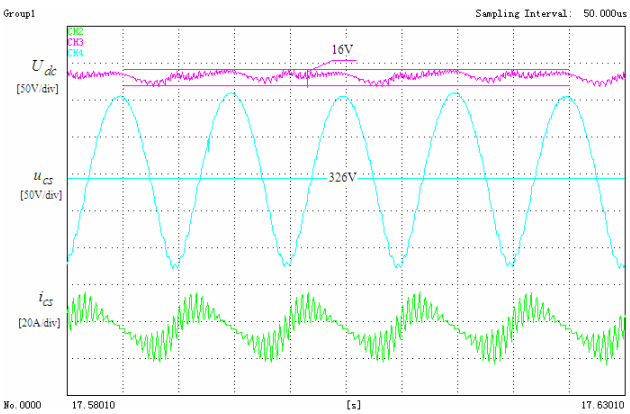
Fig. 11(d) depicts the net ripple power (the ripple power of the rectifier minus the compensating power of the APF) flowing into the dc link during the compensating process. The



(a) Without APF.



(b) With APF but under dual-loop control only.

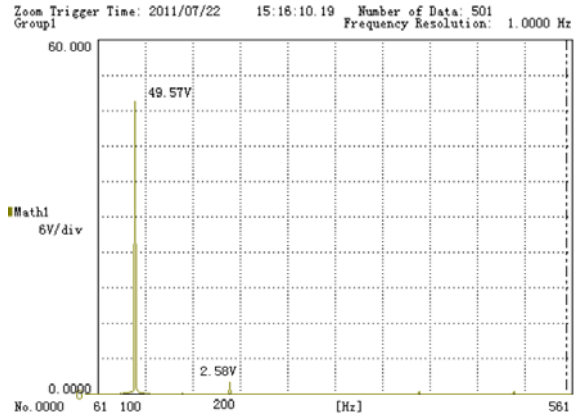


(c) With APF under dual-loop and repetitive control.

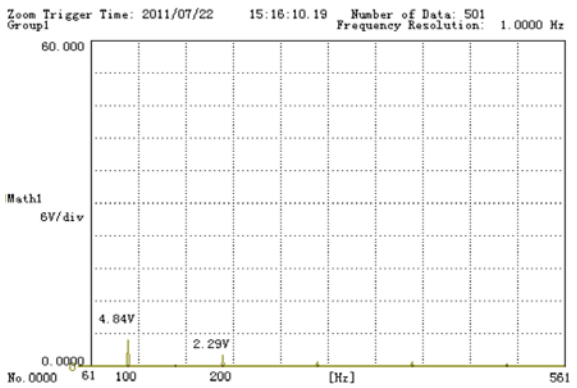
Fig. 12. Experimental results.

rectifier starts operation at t=0.2s. The APF is switched on at t=0.6s. The voltage command u_{cs}^* is ramped up slowly to avoid current rush. Initially only the dual-loop control is in effect. The repetitive control is put into action at t=1.1s. It can be seen that the ripple power flowing into the dc link was reduced considerably by the dual-loop control after t=0.9s, and then it was further reduced by the repetitive control.

V. EXPERIMENTAL RESULTS



(a) Without APF.



(b) With APF.

Fig. 13. FFT analysis of dc link voltage.

Experiments were made on the 3.5 kW test setup mentioned in Section III. The proposed control scheme is implemented with a DSP2812 control board. The sampling frequency is 4 kHz, so that the control algorithm is executed twice within each switching period.

Fig. 12(a) shows the dc link voltage, the APF capacitor voltage, and the APF capacitor current when the APF is not working. The peak-to-peak value of the dc link ripple voltage is 130V. Fig. 12(b) shows the same waveforms when the APF is working but with the dual-loop control strategy only. The APF current is continuous, and the dc link ripple voltage is reduced to 66V.

In Fig. 12(c), the APF is working with both the dual-loop control and the repetitive control. The ripple voltage is further reduced to 16V (peak to peak). It can also be noticed that the voltage and current of the APF capacitor now bear a closer resemblance to the theoretical waveforms shown in Fig. 3. This indicates a higher precision of the command realized with the repetitive control.

Fig. 13 gives the FFT analysis of the dc link voltage. It can be seen that the 100 Hz component is reduced from 49.57V to 4.84V. The 200 Hz component is reduced from 2.58V to 2.29V. These results are less perfect than the simulation

results due to the fact that there are more non-ideal factors and disturbances in the experiments, such as the limited word-length effects of digital control, detection noise, harmonics in the grid voltage, etc. Nonetheless, the results are still quite acceptable for practical applications.

In the experiments, a 220μF film capacitor is used as the main dc link capacitor. The APF capacitor is 130μF. To obtain the same filter effect as shown in Fig. 12(c), nearly a 1600μF capacitor is needed in the dc link. The capacitance is reduced by a total of 4.5 times when compared with the passive filter topology, where only a dc link capacitor is used.

VI. CONCLUSIONS

This paper proposed a ripple power compensation method based on a simple and effective dc-link APF topology for single phase converters. The circuit works in CCM mode, and with a low switching frequency, which is suitable for high power applications. By careful design of the circuit parameters, the requirement for the closed-loop bandwidth can be reduced to a reasonable level. The dual-loop control improves the dynamic response and the repetitive control further reduces the steady-state error. Simulation and experimental results verified the proposed method.

REFERENCES

[1] P. T. Krein and R. S. Balog, "Cost-effective hundred-year life for single-phase inverters and rectifiers in solar and LED lighting applications based on minimum capacitance requirements and a ripple power port," *Applied Power Electronics Conference and Exposition* (APEC), pp. 620-625, 2009.

[2] A. Cheok, S. Kawamoto, T. Matsumoto, and H. Obi, "AC drive with particular reference to traction drives, " *in Proc. Advances in Power System Control, Operation and Management Conference*, Vol. 1, pp. 348-353 , 1997.

[3] J. Klima, "Analytical investigation of influence of DC-link voltage ripple on PWM VSI fed induction motor drive," *in Proc. IEEE Industrial Electronics and Applications Conference*, pp. 1-7, 2006.

[4] J. Klima, M. Chomat, and L. Schreier, "Analytical closed-form investigation of PWM inverter induction motor drive performance under DC bus voltage pulsation," *Electric Power Applications*, Vol. 2, No. 6, pp. 341-352, Nov. 2008.

[5] P. Chapas and Bohong Wang, "The electric locomotive PRIMA 3U15 of ALSTOM Transport," *Converter Technology & Electric Transactions*, Vol. 3, pp. 43-49, 2005.

[6] Liu Yujie, Sheng Caifei, Lin Fei, et. al., "Harmonic analysis of power grid-side for high speed train," *Electric Drive*, Vol. 1, No. 40, pp. 33-37, 2010.

[7] C. Yanping, X. Li, and L. Zhonghao, "Research on the secondary resonant circuit of single-phase voltage-pulse rectifier," *Electric Drive For Locomotives*, No. 2, pp. 28-32, 2010.

[8] T. Larsson and S. Ostlund, "Active DC link filter for two frequency electric locomotives," *Electric Railways in a United Europe*, pp. 97-100, 1995.

[9] T. Shimizu, Y. Jin, and G. Kimura, "DC ripple current reduction on a single-phase PWM voltage-source rectifier," *IEEE Trans. Ind. Appl.*, Vol. 36, No. 5, pp. 1419-1429, Sep./Oct. 2000.

[10] K. Tsuno, T. Shimizu, K. Wada, and K. Ishii, "Optimization of the DC ripple energy compensating circuit on a single-phase voltage source PWM rectifier," *Power Elecronics Specialists Conference*, Aachen, Germany, Vol. 1, pp. 316-321, 2004.

[11] T. Shimizu, T. Fujita, G. Kimura, and J. Hirose, "A unity power factor PWM rectifier with DC ripple compensation," *IEEE Trans. Ind. Electron.*, Vol. 44, No. 4, pp. 447-455, Aug. 1997.

[12] K.-H. Chao, P.-T. Cheng, and T. Shimizu, "New control methods for single phase PWM regenerative rectifier with power decoupling function," Power Electronics and Drive System Conference, pp. 1091-1096, 2009.

[13] R. Wang, F. Wang, D. Boroyevich, and P. Ning, "A high power density single phase PWM rectifier with active ripple energy storage," *IEEE Applied Power Electronics Conference*, pp. 1378-1383, 2010.

[14] R. Wang, F. Wang, P. Ning, R. Burgos, and D. Boroyevich, "Study of energy storage capacitor reduction for single phase PWM rectifier," *IEEE Applied Power Electronics Conference*, pp. 1177-1183, 2009.

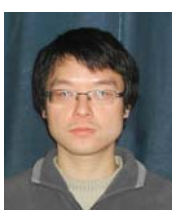
[15] T. Haneyoshi, A. Kawamura, and R. G. Hoft, "Waveform compensation of PWM inverter with cyclic fluctuating loads," *IEEE Trans. Ind. Appl.*, Vol. 24, No. 4, pp. 582-589, Jul./Aug. 1988.

[16] Y.-Y. Tzou, R.-S. Ou, S.-L. Jung, and M.-Y Chang, "High-performance programmable AC power source with low harmonic distortion using DSP-based repetitive control technique," *IEEE Trans. Power Electron.*, Vol. 12, No. 4, pp. 715-725, Jul. 1997.

[17] K. Zhang, Y. Kang, J. Xiong, and J. Chen, "Direct repetitive control of SPWM inverter for UPS purpose," *IEEE Trans. Power Electron.*, Vol. 18, No. 3, pp. 784-792, May 2003.

[18] X. H. Wu, S. K. Panda, and J. X. Xu, "DC link voltage and supply-side current harmonic minimization of three phase PWM boost rectifiers using frequency domain based repetitive current controllers," *IEEE Trans. Power Electron.*, Vol. 23, No, 4, pp.1987-1997, Jul. 2008.

[19] K. Zhou, D. Wang, B. Zhang, and Y. Wang, "Plug-in dual-mode-structure repetitive controller for CVCF PWM inverters," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 3, pp. 784-791, Mar. 2009.



Hongbo Li was born in Henan, China. He received his B.E. and M.E. from the Wuhan University of Science and Technology (WUST), Wuhan, China, and the Huazhong University of Science and Technology (HUST), Wuhan, China, in 2006, and 2008, respectively. His research interests include railway traction drives and active power filters.

Kai Zhang was born in Henan, China. He received his B.E., M.E., and Ph.D. from the Huazhong University of Science and Technology (HUST), Wuhan, China, in 1993, 1996, and 2001, respectively. In 1996, he joined HUST as an Assistant Lecturer. He was a Visiting Scholar at the University of New Brunswick, Fredericton, NB, Canada, from 2004 to 2005. He was promoted to a Full Professor in 2006. His research interests include uninterruptible power systems, railway traction drives, and electromagnetic compatibility techniques for power electronic systems. He is the author of more than 40 technical papers.

Hui Zhao was born in Hubei, China. He received his B.E. from the Huazhong University of Science and Technology (HUST), Wuhan, China, in 2010, where he is currently working toward his M.E. in the School of Electrical and Electronic Engineering. His research interests include active power filters and motor drives.