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Single-Stage High-Power-Factor Electronic Ballast with a Symmetrical Class-DE Resonant Rectifier

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Abstract

This paper presents the use of a novel, single-stage high-power-factor electronic ballast with a symmetrical class-DE low-*dv/dt* resonant rectifier as a power-factor corrector for fluorescent lamps. The power-factor correction is achieved by using a bridge rectifier to utilize the function of a symmetrical class-DE resonant rectifier. By employing this topology, the peak and ripple values of the input current are reduced, allowing for a reduced filter inductor volume of the EMI filter. Since the conduction angle of the bridge rectifier diode current was increased, a low-line current harmonic and a power factor near unity can be obtained. A prototype ballast, operating at an 84-kHz fixed frequency and a 220-V_{rms}, 50-Hz line input voltage, was utilized to drive a T8-36W fluorescent lamp. Experimental results are presented which verify the theoretical analysis.

Key words: Class-DE resonant rectifier, Electronic ballast, Power-factor correction, Single-stage

I. INTRODUCTION

High-frequency resonant inverters have played a very important role in the development of gas-discharge lamps, especially fluorescent lamps, since they can improve the light quality and prolong the lamp lifetime [1]. Most electronic ballasts use class-D resonant inverters because they can provide a high striking voltage during startup. In addition, they provide current-limiting control to allow for steady-state operation with a low crest factor for fluorescent lamps. However, this type of circuit causes a large and sharp input current when the input ac source voltage reaches its peak. The distorted current waveform affects the power quality and results in a lower total power factor. In order to alleviate this drawback, a power-factor correction (PFC) circuit must be attached to the electronic ballast, thus reducing the harmonics in the utility line current and satisfying the IEC 61000-3-2 class-C standard for lighting equipment. The high-power-factor, electronic ballast is developed using a two-stage circuit, which has been presented in previous studies [2]-[5]. The main problem associated with a two-stage electronic ballast is the increasing number of components it requires, which results in higher costs. Recently, many researchers have focused on a single-stage approach in which the power-factor-corrector stage and the dc/ac resonant inverter stage are integrated into single-stage electronic ballasts (SSEBs) [6]-[17]. However, most single-stage electronic ballasts use a large electromagnetic interference (EMI) filter due to the high levels of harmonic distortion from line input current, making this ballast unattractive for commercial applications. The objective of this paper is to introduce a new SSEB topology in which a symmetrical class-DE rectifier is used as a power-factor corrector while the volume of the inductor in the EMI filter is reduced.

This paper is organized as follows. In Section II, the circuit description is presented. In Section III, the principle of operation is described. The design procedure for the components is presented in Section IV. Simulation and experimental results to support the theoretical analysis are presented in Section V. In Section VI, a simplified circuit is presented. Some conclusions are given in Section VII.

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II. CIRCUIT DESCRIPTION

Figure 1 shows the circuit of the proposed single-stage electronic ballast. The circuit consists of a filter inductor, L_f,

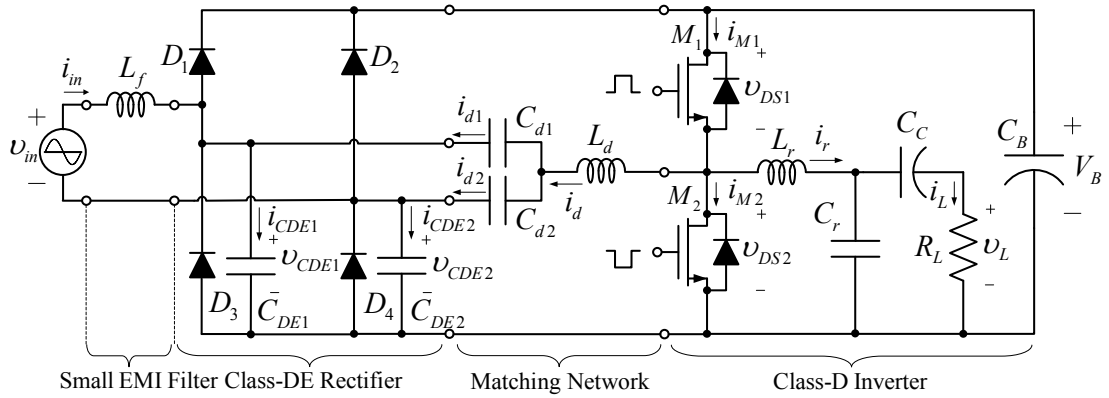


Fig. 1. Proposed electronic ballast with symmetrical class-DE resonant rectifier as a PFC stage.

a bridge rectifier, $D_1 - D_2 - D_3 - D_4$, and two high-frequency capacitors, C_{DE1} and C_{DE2}, which are connected in parallel with the two diodes, D_3 and D_4, of the bridge rectifier in order to form a symmetrical class-DE resonant rectifier. Additionally, an inductor, L_d, and two capacitors, C_{d1} and C_{d2}, serve the function of high-frequency current shaping, while coupling capacitors and a bulk-filter capacitor, C_B, supply the class-D parallel resonant inverter. The voltage, V_B, across this capacitor is nearly constant, which results in constant lamp current and voltage amplitudes, and a class-D parallel resonant inverter, $L_r - C_r - C_C - R_L$. All power switches are operated under the zero-voltage switching (ZVS) condition. The matching network, $L_d - C_{d1} - C_{d2}$, is fed by a square-wave output voltage from the class-D resonant inverter and is converted to a high-frequency current source to drive the symmetrical class-DE rectifier.

III. PRINCIPLE OF OPERATION

The principle of operation of the symmetrical class-DE resonant rectifier in the PFC stage is demonstrated by the equivalent circuit shown in Fig. 2(a). The diodes, D_1 and D_4, of the bridge rectifier operate during the positive half-cycle of the line voltage, which is represented as $\upsilon_{in} = V_{in} \sin \omega_L t$, where ω_L is the line angular frequency and the diodes, D_2 and D_3, operate during the negative half-cycle. The model of the line-voltage rectifier output is a full-wave rectified sinusoidal voltage source (i.e., $|\upsilon_{in}| = V_{in} |\sin \omega_L t|$). Because the dc voltage source, V_B, appears as a short circuit to the ac component, the capacitor, C_{DE1}, and the high-frequency current source, i_{d1}, can be connected in parallel with D_1, as shown in Fig. 2(b). In addition, the parallel connection of D_1, C_{DE1}, and the high-frequency current source, i_{d1}, is connected in series with the voltage source, $|\upsilon_{in}|$. The order of these elements is interchangeable, as shown in Fig. 2(c). In this circuit, the

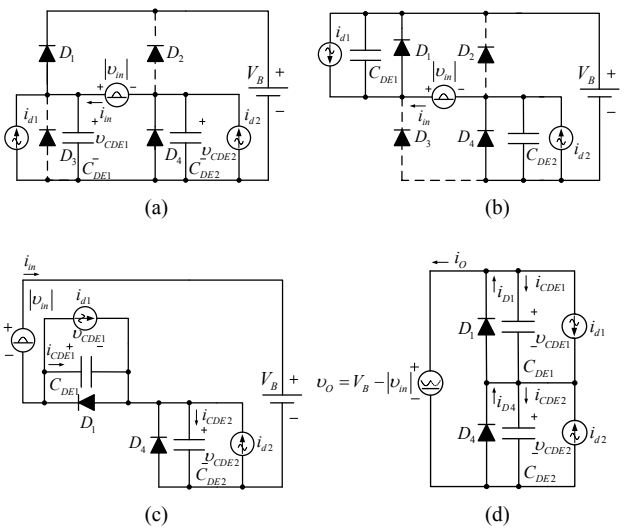


Fig. 2. Circuit derivation of the PFC with a symmetrical class-DE rectifier during the positive half-cycle of the line voltage: (a) equivalent circuit; (b) equivalent circuit when moving the capacitor (C_{DE1}) and the current source (i_{d1}); (c) equivalent circuit when moving D_1, C_{DE1}, i_{d1}, and $|\upsilon_{in}|$; (d) equivalent, symmetrical circuit with a combined voltage source, $V_B - |\upsilon_{in}|$.

voltage sources V_B and $|\upsilon_{in}|$ are connected in series and can be combined into an output voltage, $\upsilon_O = V_B - |\upsilon_{in}|$, of the class-DE rectifier, as can be seen in Fig. 2(d). The output characteristics of the symmetrical class-DE low-*dυ/dt* rectifier with a varying resistive load roughly match the conceptual waveforms of the proposed PFC shown in Fig. 3. Fig. 3(a) shows the sinusoidal line-voltage waveform. Fig. 3(b) and (c) show the rectified line voltage, $|\upsilon_{in}|$, and the combined voltage waveform, $V_B - |\upsilon_{in}|$, respectively. If the instantaneous value of υ_{in} is positive and low, the voltage of the class-DE low-*dυ/dt* rectifier, $V_B - |\upsilon_{in}|$, is high, and the duty ratio, D_d, of the

rectifier diode current is low. Therefore, the average value of the rectifier diode current over one switching cycle is low. Conversely, if the instantaneous value of υ_{in} is positive and high the voltage of the class - DE rectifier, $V_B - |\upsilon_{in}|$, is low, and the duty ratio, D_d, of the rectifier diode is high. Thus, the average value of the diode current over one switching cycle is high. For a half-cycle with a negative line voltage, the bridge rectifier rectifies the negative values of υ_{in} to positive values and rectifies those of the diode duty ratio as a half-cycle with a position line voltage. The conduction angle modulation of the rectifier diode over the line frequency, f_L, and the line-input current, i_{in}, are shown in Fig. 3(d).

The idealized current and voltage waveforms in a class-DE low-$d\upsilon/dt$ rectifier are shown in Fig. 4. Current flows through diodes D_1 and D_4 when each diode is ON and it passes through capacitors C_{DE1} and C_{DE2} when the diodes are OFF. The diodes begin to turn off when their current reaches zero. The current passing through the capacitors, C_{DE1} and C_{DE2}, shapes the voltage across the diodes in accordance with the equation $i_{CDE} = C_{DE} d(\upsilon_{CDE}) / dt$. Because i_{CDE1} and i_{CDE2} are zero at turn-off, each diode turns off at $d\upsilon/dt = 0$. The diodes turn on at a low $d\upsilon/dt$ to reduce the turn-on switching loss and noise. The principles of operation of the class-D parallel resonant inverter in the proposed circuit are explained by the equivalent circuit in Fig. 5(a). The input impedance of the class-DE rectifier is represented by a series combination of the input resistor, R_i, and the input capacitor, C_i, as shown in Fig. 5(b). The capacitor, C_r, and the lamp resistance, R_L, are converted into a series $R_s - C_{rs}$ circuit, as shown in Fig. 5(c). The $C_d - C_i$ circuit is replaced by an equivalent capacitor, which is represented as $C_{di} = C_d C_i / (C_d + C_i)$. The MOSFETs are modeled by switches with the on-resistances, r_{DS1} and r_{DS2}. The resistances, r_{Ld} and r_{Lr}, represent the equivalent resistances of the inductors, L_d and L_r, respectively. The equivalent circuits of the class - D parallel resonant inverter are modeled by a square-wave voltage source, υ_S, with an equivalent resistor, $r_S = (r_{DS1} + r_{DS2}) / 2 \approx r_{DS}$, and are loaded by two sub-circuits, $r_{Ld} - R_i - L_d - C_{di}$ and $r_{Lr} - R_s - L_r - C_{rs}$. The proposed electronic ballast can be divided into two parts: a PFC semi-stage and an inverter semi-stage. Fig. 6(a) shows an equivalent circuit of the PFC semi-stage. Fig. 6(b) depicts a simplified circuit of the PFC symmetrical class-DE low-$d\upsilon/dt$ rectifier. Fig. 6(c) shows an equivalent circuit of the inverter semi-stage. From Fig. 6(a), the minimum value of the load resistance, R_{DEmin}, occurs at the minimum output voltage, υ_{Omin}, as does the maximum output current, i_{Omax}, of the symmetrical class-DE low-$d\upsilon/dt$ rectifier. The minimum load resistance, R_{DEmin}, is defined as [16]:

$$R_{DEmin} = \frac{\upsilon_{Omin}}{i_{Omax}} = \frac{V_B - V_{in}}{I_{in}}. \tag{1}$$

The ratio of the dc bus voltage and the amplitude of the input line voltage, V_B/V_{in}, is obtained as (2). Figure 7 illustrates the voltage ratio (V_B/V_{in}), which is a function of the maximum duty ratio of the class-DE rectifier diode, D_{dmax}, according to (2). The minimum conduction angle, ϕ_{min}, which is a function of the duty ratio of the maximum class-DE rectifier, is shown in Fig. 8. The normalized effective input impedance [18] of the class-DE resonant rectifier is $Z_i' = \omega_s 2 C_{DE} Z_i = R_i' + jX_{Ci}'$. The normalized input resistance, R_{i_fl}', and the reactance, X_{Ci_fl}', are plotted versus D_{dmax} and shown in Figs. 9 and 10, respectively. The numerical values of the class-DE rectifier parameters at selected maximum duty ratio values, D_{dmax}, are given in Table I.

$$\frac{V_B}{V_{in}} = \left\{ \left(2\pi + \frac{2\pi(1 - \cos\pi - 2\pi D_{dmax})}{(1 + \cos\pi - 2\pi D_{dmax})} \right)^2 \times \left(\frac{P_{in}(\sin\pi - 2\pi D_{dmax})^2}{16 f_s C_{DE} V_{in}{}^2 \pi^2} \right) + 1 \right\}. \tag{2}$$

TABLE I

PARAMETERS OF CLASS-DE RECTIFIER FOR PFC

D_{dmax}	ϕ_{min}	$2\omega_s C_{DE} R_{DEmin}$	$2\omega_s C_{DE} R_{i\_fl}$	$2\omega_s C_{DE} X_{Ci\_fl}$	V_B/V_{in}
0.10	2.513	58.929	0.110	- 0.951	5.617
0.15	2.199	24.108	0.208	- 0.851	2.889
0.20	1.884	11.866	0.288	- 0.692	1.929
0.25	1.570	6.283	0.318	- 0.499	1.492
0.30	1.256	3.309	0.287	- 0.306	1.259
0.35	0.942	1.626	0.208	- 0.148	1.127
0.40	0.628	0.661	0.109	- 0.048	1.051
0.45	0.314	0.156	0.030	- 0.006	1.012
0.50	0.000	0.000	0.000	- 0.000	1.000

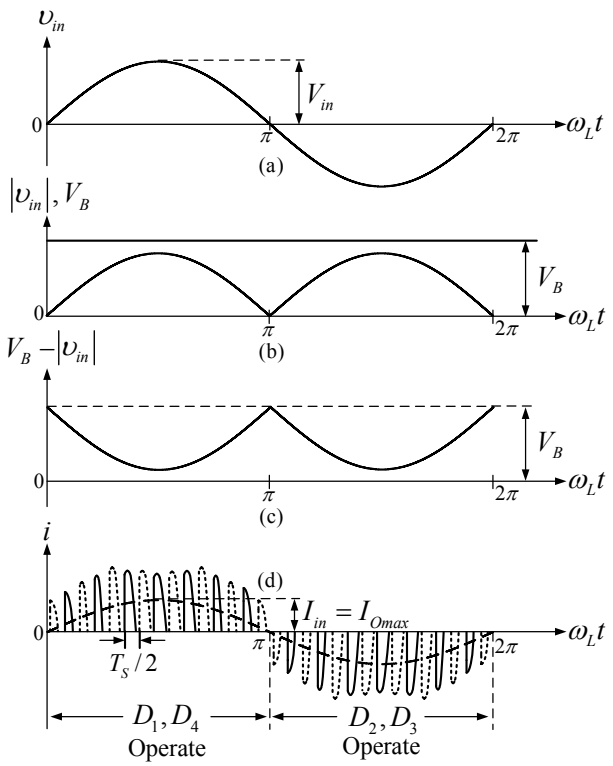


Fig. 3. Conceptual waveforms of the symmetrical class-DE resonant rectifier as a PFC: (a) line voltage waveform, υ_{in}; (b) the rectified line voltage, $|\upsilon_{in}|$; (c) the combined voltage, $V_B - |\upsilon_{in}|$; (d) the input current waveform, i_{in}, is the filtered average diode current and follows the shape of the line voltage, υ_{in}.

IV. Design Procedure

The design of the proposed SSEB can be divided into two parts: the PFC semi-stage and the ballast semi-stage. The ballast semi-stage can be designed as detailed in [16]. The design procedure for the PFC semi-stage, using a symmetrical class-DE low-*dv/dt* rectifier, is given as follows:

1. To design the PFC symmetrical class-DE rectifier, the no-load condition, at the duty ratio $D_d = D_{dmin} = 0$, and the full-load condition, at the duty ratio $D_d = D_{dmax}$, were considered. In addition, a near-sinusoidal input line current was assumed, and an expected efficiency η was estimated. The input power, P_{in}, and amplitude of the input line current, I_{in}, which is the maximum output current, I_{Omax}, of the class-DE resonant rectifier, was obtained for a given output power, P_{out}, and rms value of the input line voltage, V_{irms}.
2. Choose a maximum duty ratio, D_{dmax}, taking into consideration the tradeoffs regarding the ratio of the dc bus voltage and the amplitude of the input line voltage, V_B/V_{in}. If a low value of D_{dmax} is used, then the main switches have high voltage stresses. If a high value of D_{dmax} is chosen, then the main switches have low voltage stresses.
3. Find the ϕ_{min} value from the same line as the selected D_{dmax} value in Table I.
4. Determine the dc bus voltage, V_B, from the specified input line voltage, V_{in}, and add it to the calculated I_{in}, thus obtaining the class-DE resonant rectifier's full load resistance, R_{DEmin}.
5. Find f_s with a desired C_d, which is obtained by $2\omega_s C_{DE} R_{DEmin}$ from the same line as the selected D_{dmax} value in Table I.
6. Find the normalized full load inputs, R'_{i_fl} and X'_{Ci_fl}, from the same line as the selected D_{dmax} value in Table I.
7. To simplify the design procedure, we assume that the capacitance $C_d \gg C_i$. Therefore, the total capacitance, C_{di}, is approximately equal to capacitor C_i. Under the full load condition, the amplitude of the driving current, I_{d_fl}, can be determined.
8. Find the amplitude of υ_1 under the full load condition.
9. Calculate the amplitude of the driving current, I_{d_nl}, under no load.
10. Find the amplitude of υ_1 with no load.
11. Find the value of inductor L_d from the results of procedures 8 and 10.
12. Add an additional inductance, L_e, to L_d to cancel the reactance of C_d.

A. The PFC Semi-Stage Design

To mimic the design criteria of the proposed ballast, the electronic ballast was designed to handle a line rms voltage, V_{inrms}, of 220 V and a line frequency, f_L, of 50 Hz. It was assumed that the total ballast efficiency, η, was equal to 0.9. The ballast drew a sine-wave input current. The input power is given by:

$$P_{in} = \frac{P_{out}}{\eta} \approx 40 \text{ W}. \tag{3}$$

The amplitude of the ballast input current is calculated from:

$$I_{in} = I_{Omax} = \frac{\sqrt{2} P_{in}}{V_{irms}} = 0.257 \text{ A}. \tag{4}$$

With D_{dmax} equal to 0.4, the diode conduction angle is:

$$\phi_{min} = \pi - 2\pi D_{dmax} = 0.628 \text{ rad/s}. \tag{5}$$

From Table I, the following are obtained: V_B/V_{in} = 1.051;

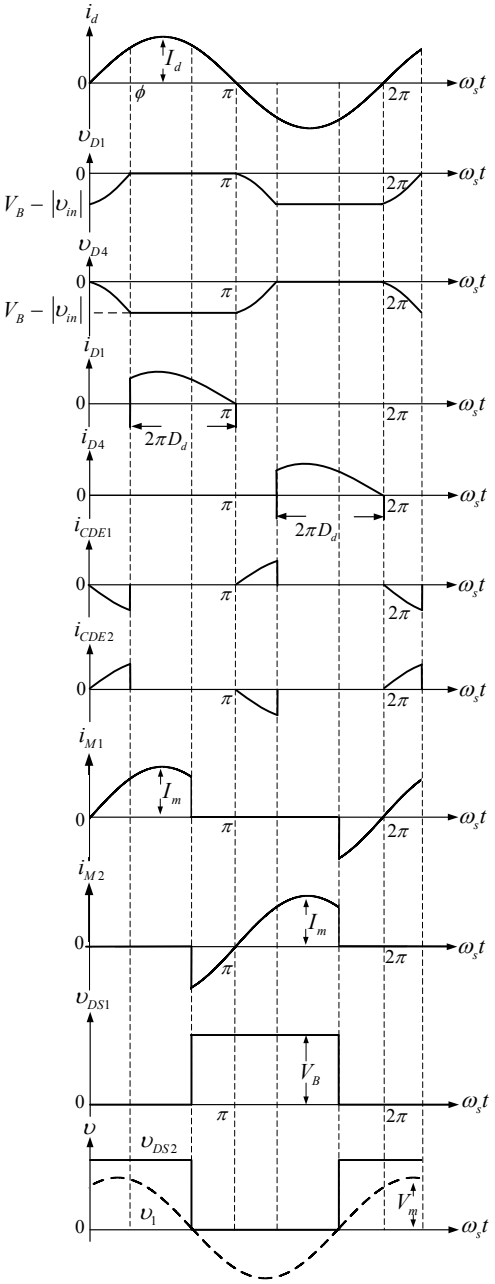


Fig. 4. Idealized current and voltage waveforms of the proposed circuit.

V_{in} (i.e., the amplitude of the line voltage) = $\sqrt{2}V_{irms} \approx 311$ V; and the dc bus voltage, V_B, is approximately 327 V. From these values, the full-load resistance is calculated as:

$$R_{DEmin} = \frac{(V_B - V_{in})}{I_{Omax}} = 62.256\ \Omega. \tag{6}$$

High-frequency, stored-charge capacitors were selected to have the following configuration: $C_{DE} = C_{DE1} = C_{DE2} = 10$ nF. The switching frequency, f_s, is given by:

$$f_s = \frac{0.661}{4\pi C_{DE} R_{DEmin}} \approx 84\ \text{kHz}. \tag{7}$$

Under a full load, the normalized effective input impedance of the class-DE resonant rectifier is:

$$Z'_{i\_fl} = \omega_s 2C_{DE} Z_{i\_fl} = R'_{i\_fl} + jX'_{Ci\_fl}, \tag{8}$$

$$\text{where} \quad R'_{i\_fl} = \frac{\sin^2 \phi_{min}}{\pi} = 0.109, \tag{9}$$

$$\text{and} \quad X'_{Ci\_fl} = \frac{\sin\phi_{min}\cos\phi_{min} - \phi_{min}}{\pi} = -0.048. \tag{10}$$

The input impedance value of the class-DE rectifier is obtained by solving (7) – (10). The resulting value is $Z_{i\_fl} = 10.9 - j4.8\ \Omega$. The magnitude of $i_d = i_{d1} + i_{d2}$, under a full load, is determined by:

$$I_{d\_fl} = \sqrt{\frac{2I_{Omax}(V_B - V_{in})}{R_{i\_fl}}} = 0.868\ \text{A}. \tag{11}$$

The bus voltage, V_B, is equal to 327 V; therefore, $I_{d\_fl} = 0.868$ A. The magnitude of the equivalent voltage source, υ_1, is:

$$V_1 = I_{d\_fl}\left|Z_{i\_fl}\right| \tag{12}$$

where the magnitude of the impedance of Z_{i_fl} is given by:

$$\left|Z_{i\_fl}\right| = \sqrt{R_{i\_fl}^2 + \left(\omega_s L_d - \frac{1}{\omega_s C_{i\_fl}}\right)^2}. \tag{13}$$

Under the no-load condition, the magnitude of the driving current, i_d, is determined by:

$$I_{d\_nl} = \frac{V_B/2}{\left|-j/\omega_s 2C_{DE}\right|} = 1.635\ \text{A}. \tag{14}$$

Therefore, I_{d_nl} = 1.635 A, and the magnitude of the equivalent voltage source, υ_1, is determined by:

$$V_1 = I_{d\_nl}\left|j\omega_s L_d - \frac{j}{\omega_s 2C_{DE}}\right|. \tag{15}$$

The values of V_1 and L_d are obtained by solving (12), (13),

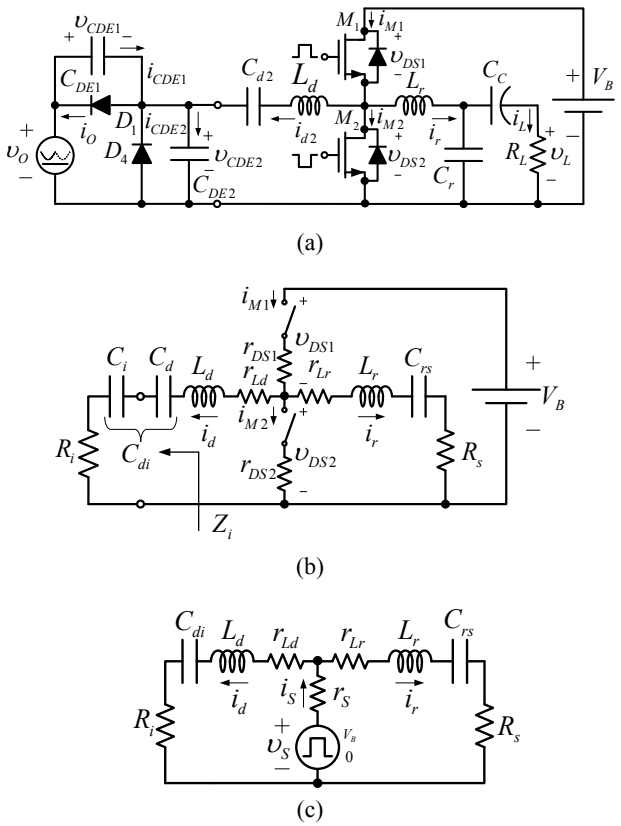


Fig. 5. Circuit of the symmetrical class-DE rectifier semi-stage and the class-D parallel resonant inverter: (a) circuit with a symmetrical class-DE rectifier and a parallel-resonant circuit; (b) the symmetrical class-DE rectifier is replaced by the equivalent circuit, $C_i - R_i$, and the $R_L - C_r$ circuit is transformed into an $R_s - C_{rs}$ circuit; (c) equivalent circuit of the inverter.

and (15). The resulting value of L_d equals 394.120 μH. For a finite value of the capacitance (C_d), an additional L_e can be added to L_d to compensate for the reactance of $C_d = C_{d1} = C_{d2} = 100$ nF. The value of the additional inductance is:

$$L_e = \frac{1}{\omega_s^2 C_d} = 35.898\ \mu\text{H}. \tag{16}$$

The total inductance $L_{d(\text{total})}$ is:

$$L_{d(\text{total})} = L_d + L_e = 430.018\ \mu\text{H}. \tag{17}$$

To achieve a ripple voltage of less than 1%, the value of the bulk filter capacitor is determined by:

$$C_B \geq \frac{P_{in}}{2V_B^2 V_{ripple}\omega_L} = 59.53\ \mu\text{F}. \tag{18}$$

Therefore, the standard value of 68 μF is selected for C_B.

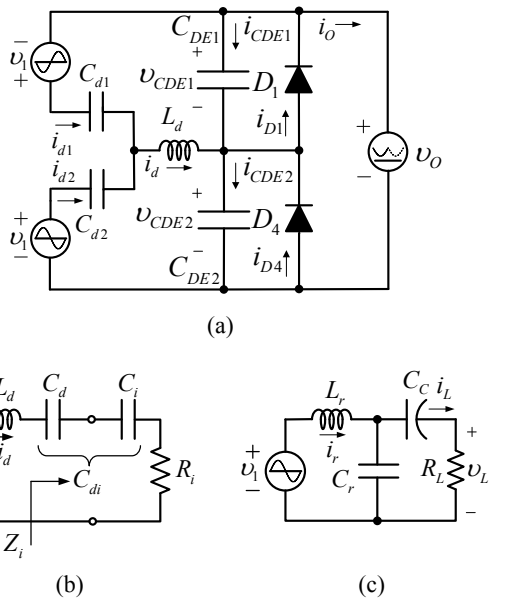


Fig. 6. Equivalent circuits of the electronic ballast: (a) PFC symmetrical class-DE rectifier with an equivalent sine-wave voltage source, υ_1; (b) simplified equivalent circuit of (a); (c) equivalent circuit of the inverter semi-stage.

B. Ballast Semi-Stage Design

A class-D parallel resonant inverter is shown in Fig. 6(c), the design of which can be found in [2]. The class-D parallel resonant inverter is easy to design.

C. Conduction Loss Analysis

The calculated conduction loss of the electronic ballast, as a function of the load resistance, R_L, is depicted in Fig. 5. Therefore, the maximum value of the drain current (i.e., $I_M = I_S = I_d + I_r$) is shown in Fig. 5(c). Thus the power loss in each MOSFET's forward resistance, r_{DS}, is given by:

$$P_{rDS} = \frac{I_M^2 r_{DS}}{4} = 607\ \text{mW}. \tag{19}$$

The converter employs (STMicroelectronics IRF740) MOSFETs, each with an on-resistance, r_{DS}, of 0.48 Ω. The power loss in the diodes, $D_1 - D_4$, due to the forward voltage, V_D, is obtained as:

$$P_{DB} = \frac{V_D I_D}{2} = 156\ \text{mW}. \tag{20}$$

The bridge rectifier was built using a (Philips BYM36C) fast-recovery diode with a *pn* junction diode ($V_D = 1.22$ V). The ESR of the filter inductor is $r_{Lf} = 1.391$ Ω. Thus, the conduction loss in the filter inductor, L_f, can be obtained as:

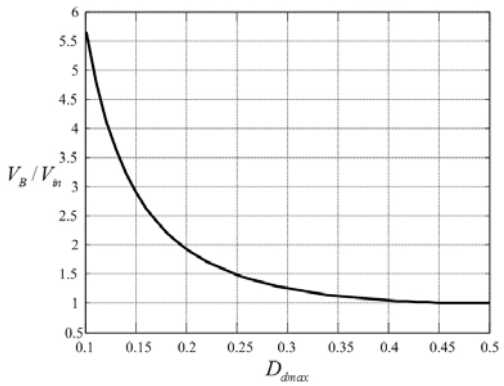


Fig. 7. V_B/V_{in} as a function of D_{dmax}.

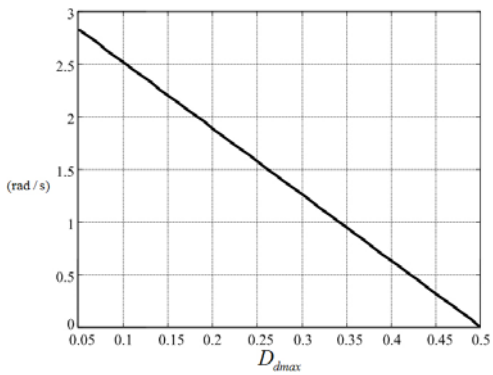


Fig. 8. Conduction angle ϕ_{min} versus D_{dmax}.

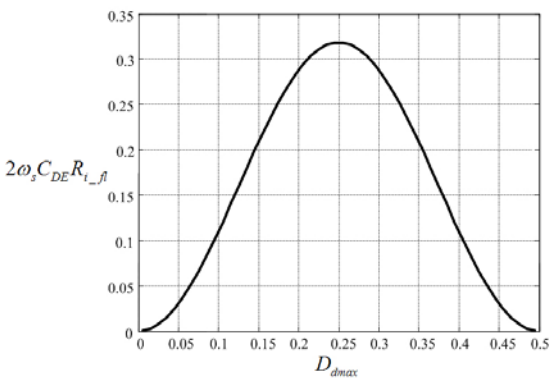


Fig. 9. $2\omega_s C_{DE} R_{i\_fl}$ as a function of D_{dmax}.

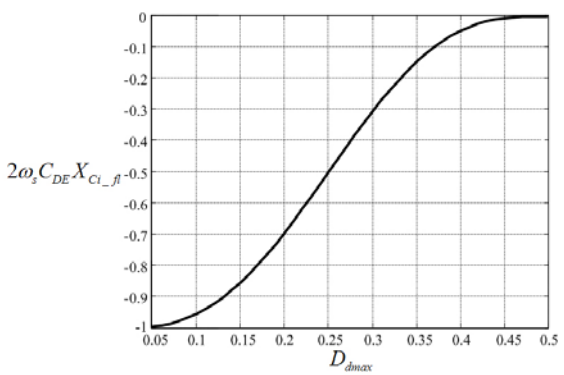


Fig. 10. $2\omega_s C_{DE} X_{Ci\_fl}$ as a function of D_{dmax}.

TABLE II

CIRCUIT PARAMETERS OF THE PROTOTYPE

Parameter	*Value and Part Number*
M_1 and M_2	N-Channel MOSFETs IRF740
D_1–D_4	Fast Recovery Diodes BYM36C
L_f	1 mH (DRWW10x16 N-series-YTE)
L_d	430 μH (EE30/15/7 N27-EPCOS)
L_r	775 μH (EE25/13/7 N27-EPCOS)
C_{d1} and C_{d2}	100 nF (polypropylene)
C_{DE1} and C_{DE2}	10 nF (polypropylene)
C_r	4.7 nF (polypropylene)
C_C	1 μF (polypropylene)
C_B	68 μF (electrolytic)

$$P_{rLf} = \frac{I_{in}^2 r_{Lf}}{2} = 45.937 \text{ mW}. \quad (21)$$

The parasitic resistance of the series inductor, r_{Ld}, is 0.119 Ω. Thus the conduction loss in the inductor, L_d, is obtained from:

$$P_{rLd} = \frac{I_d^2 r_{Ld}}{2} = 159 \text{ mW}. \quad (22)$$

The parasitic resistance of the inductor, r_{Lr}, is 0.371 Ω, and the maximum value of the resonant current, I_r, is given by (23). Therefore, the conduction loss in the inductor, L_r, is given by:

$$I_r = \frac{2V_B\sqrt{Q_L^2+1}}{\pi Z_O} = 615 \text{ mA}. \quad (23)$$

$$P_{rLr} = \frac{I_r^2 r_{Lr}}{2} = 70 \text{ mW}. \quad (24)$$

Conduction losses due to the parasitic resistance in the overall capacitors are very small. Therefore, their affects were neglected.

V. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

Figure 11 shows the simulated input line-current waveforms of the asymmetrical and symmetrical class-DE resonant rectifiers without a filter inductor, L_f. These waveforms show that the input line current in the symmetrical class-DE resonant rectifier has half the peak value and double the frequency when compared to the asymmetrical rectifier. The higher value for the peak line input current is the main drawback of the asymmetrical topology.

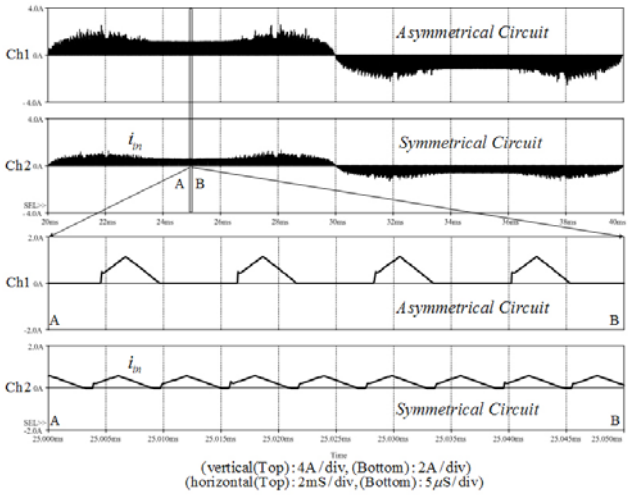


Fig. 11. Comparison of the simulated waveforms of the input line-current of the asymmetrical and symmetrical circuits, with the bottom two waveforms as zoomed-in views of the top two waveforms.

B. Experimental Results

A prototype ballast was constructed using the component values obtained from the design procedure given above. The details of these calculations are given in design procedures A and B. The circuit parameters are presented in Table II. The switching frequency was fixed at about 84 kHz. The line voltage was set to 220 V_{rms}, and the line frequency, f_L, was 50 Hz. The measured input line power was approximately 39.9 W, while the input power-factor was approximately 0.99 (as shown in Fig. 12). The THD of the input current, THDi, was about 1%, as shown in Fig. 13. The proposed electronic ballast can be operated with a line voltage of 220 V_{rms} ± 20%. The measured THDi and PF are shown in Fig. 14. Otherwise, the electronic ballast will suffer from a wide range of lamp power variations. Near the zero crossing, the line current can not reach zero if the line voltage is too high. On the other side, the line current shows a dead band near the zero crossing when the line voltage is too low. In such cases, a near-sinusoidal line input current can be obtained by using switching frequency modulation over a wide range of line input voltages.

Figure 15 illustrates the experimental waveforms of the diode current, i_{D1}, and the capacitor voltage, υ_{CDE1}, of the symmetrical class-DE low-*dυ/dt* rectifier near the peak and zero-crossing of the line voltage, respectively. As expected, the duty ratio of the diode current decreased as the instantaneous line voltage decreased. The switch voltage and the switch current waveforms of D_1 of the class-DE resonant rectifier are shown in Fig. 16. The waveforms of the switch voltage and the switch current of M_2 are shown in Fig. 17.

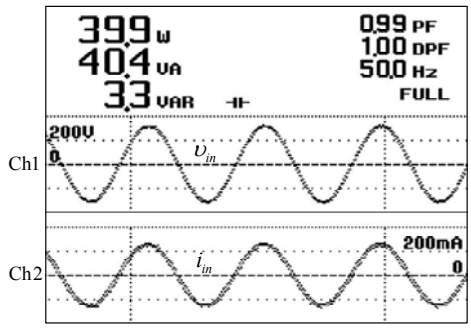


Fig. 12. Input line voltage and the current waveforms.

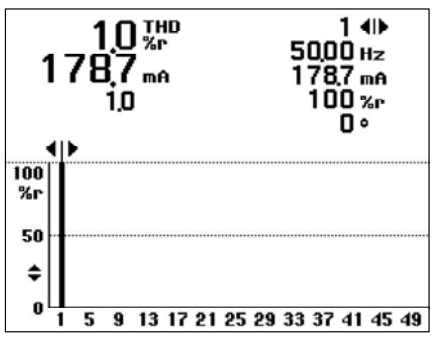


Fig. 13. Measured THD of i_{in} from the power analyzer.

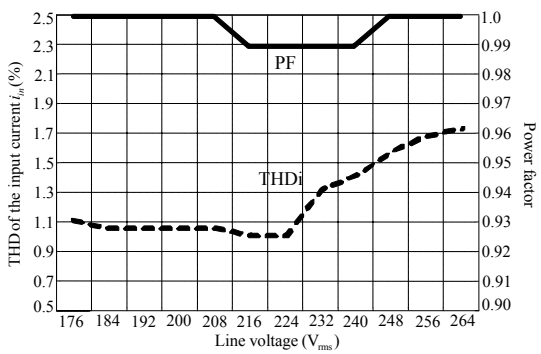


Fig. 14. THDi and PF versus line voltage.

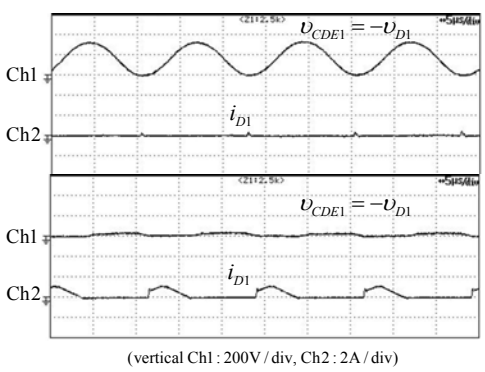
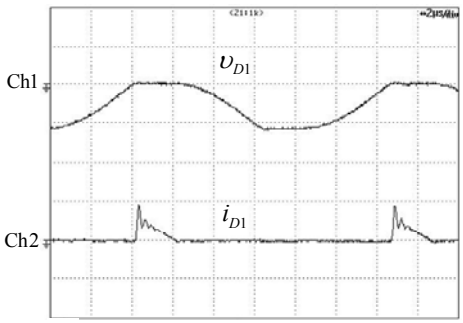
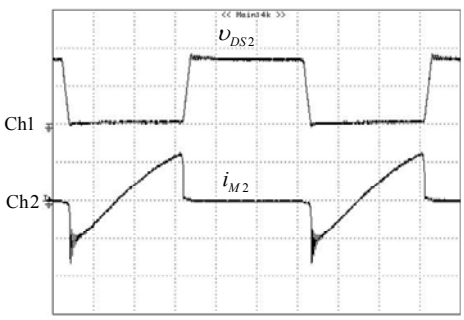


Fig. 15. Measured waveforms of i_{D1} and υ_{CDE1}; the top two waveforms are near the zero-crossing of the line voltage, while the bottom two waveforms are near the line-voltage peak.



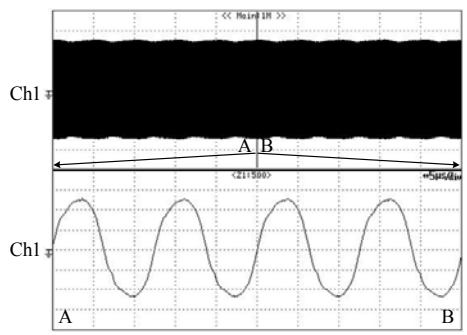
(vertical Ch1 : 200V / div, Ch2 : 2A / div)
(horizontal : 2μS / div)

Fig. 16. Measured diode voltage and current waveforms of D_1 at 40 degrees of the line voltage.



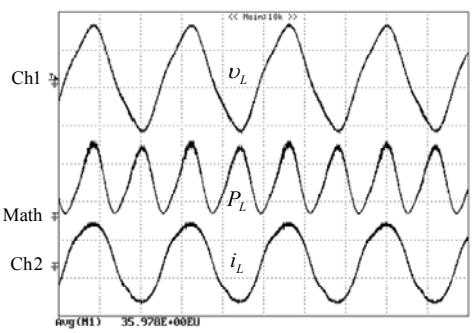
(vertical Ch1 : 200V / div, Ch2 : 2A / div)
(horizontal : 2μS / div)

Fig. 17. Measured switch voltage and current waveforms of M_2.



(vertical Ch1 : 500mA / div)
(horizontal(Top) : 2mS / div, (Bottom) : 5μS / div)

Fig. 18. Experimental envelope waveform of the lamp current; the lower waveform is a zoomed-in view of the top waveform.



(vertical Ch1 : 100V / div, Ch2 : 0.5A / div, Math : 40W / div)
(horizontal : 5μS / div)

Fig. 19. Measured voltage, power, and lamp-current waveforms.

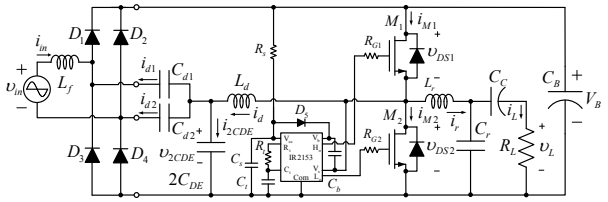


Fig. 20. Simplified electronic ballast using a single, high-frequency capacitor.

The proposed scheme provides a more systematic and feasible solution. Because the previous ballasts had an interaction between the current in the PFC semi-stage and the current in the inverter semi-stage, they had a high lamp-current crest factor when trying to achieve a low THD in the line-input current. Fig. 18 illustrates the measured waveform of the lamp current. The crest factor of the lamp current was 1.42, which meets the general lamp manufacturer recommendation of a value below 1.7. Fig. 19 shows the measured waveforms of the lamp voltage and the lamp current. The lamp power, P_L, was 35.978 W. The measured efficiency of the ballast was approximately 90%.

VI. Simplified Circuit

The circuit for the proposed electronic ballast can be simplified by combining the two high-frequency capacitors, C_{DE1} and C_{DE2}, into one, as shown in Fig. 20. The number of capacitor components is reduced. An (IR2153) IC, which is a high-side low-side driver, was used to drive a pair of MOSFETs, which were connected to form the half-bridge inverter.

VII. Conclusion

A novel, single-stage, high-power-factor, electronic ballast with a symmetrical class-DE low-*dυ/dt* rectifier as a PFC is proposed in this paper. The proposed PFC was achieved by using a bridge rectifier that serves as a symmetrical class-DE resonant rectifier. The two active power switches were operated under the ZVS condition. By using this topology, the conduction angle of the bridge rectifier diode current was increased, resulting in a low-line current harmonic, a power factor near unity, and reductions in the size and weight of the EMI filter. The prototype ballast was implemented to drive a T8-36W fluorescent lamp. The switching frequency was fixed to approximately 84 kHz. Experimental results verified the theoretical analysis. The designed electronic ballast had a power factor of 0.99, a 1% THD_i (which satisfies the lighting equipment IEC 61000-3-2 class-C standard), a 1.42 lamp-current crest factor (which meets the lamp manufacturer recommendations), and an efficiency of 90%.

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