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Direct Current Control Method Based On One Cycle Controller for Double-Frequency Buck Converters

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Abstract

In this paper, a direct current control method based on a one-cycle controller (DCOCC) for double frequency buck converters (DF buck) is proposed. This control method can make the average current through the high frequency and low frequency inductors of a DF buck converter equal. This is similar to the average current control method. However, the design of the loop compensator is much easier when compared with the average current control. Since the average current though the high frequency and low frequency inductors is equivalent, the current stress of the high frequency switches and the switch losses are minimized. Therefore, the efficiency of the DF buck converter is improved. Firstly, the operation principle of DCOCC is described, then the small signal models of a one cycle controller and a DF buck converter are presented based on the state space average method. Eventually, a system block diagram of the DCOCC controlled DF buck is established and the compensator is designed. Finally, simulation and experiment results are given to verify the correction of the theory analysis.

Key words: DF buck, One cycle controller, Small signal model

I. INTRODUCTION

In order to improve the performance of a power converter, it is necessary to increase the switching frequency. However, a higher switching frequency means higher switching losses and lower efficiency of the converter. The soft-switching technique is an effective method to solve the contradiction between the performance and efficiency of a converter and has become a hotspot in the research of power electronics [1]-[5]. In [6], a novel DF buck converter was proposed. This converter is composed of two buck cells, where the switching frequency of one of the cells is much higher than the other. Therefore, one of the cells is called the high frequency buck cell and the other one is called the low frequency buck cell. The output characteristics of the DF buck converter are determined by the high frequency cell and can be improved by increasing its switching frequency. Because the current through the high frequency switches is shunted by the low frequency buck cell, the switching losses will not increase too much due to the increases in the switch frequency. As a result, the performance of the DF buck converter is improved while the efficiency does not decrease. This is another effective way to solve the contradiction mentioned above. To shunt the current through the switches of the high frequency cell effectively, it is necessary to control the current through the inductor of the low frequency buck cell so that it is approximately equal to that of the high frequency buck cell. As a result, a current type control needs to be adopted to control the DF buck converter, such as the average current control [7], the peak current control [8], the hysteretic current control [9], etc. Adopting the average current control can make the average current through the high and low frequency inductors equal and insure that the current stresses of the high frequency switches are theoretically minimal. However, the inner current loop and the outer voltage loop compensator must be designed carefully. When adopting the peak current control, the current stress of the high frequency switch is higher and the sub-harmonic oscillation has to be eliminated. The hysteretic current control is a kind of variable frequency control and the design of the filters is quiet difficult. In this paper, a direct current control method based on a one cycle controller [10] for DF buck converters is proposed. This method has the following characteristics:

- The average current value through the high frequency inductor and the low frequency inductor can be controlled to be equal, while the current stress of the high frequency switch and the switch losses are minimized. Therefore,

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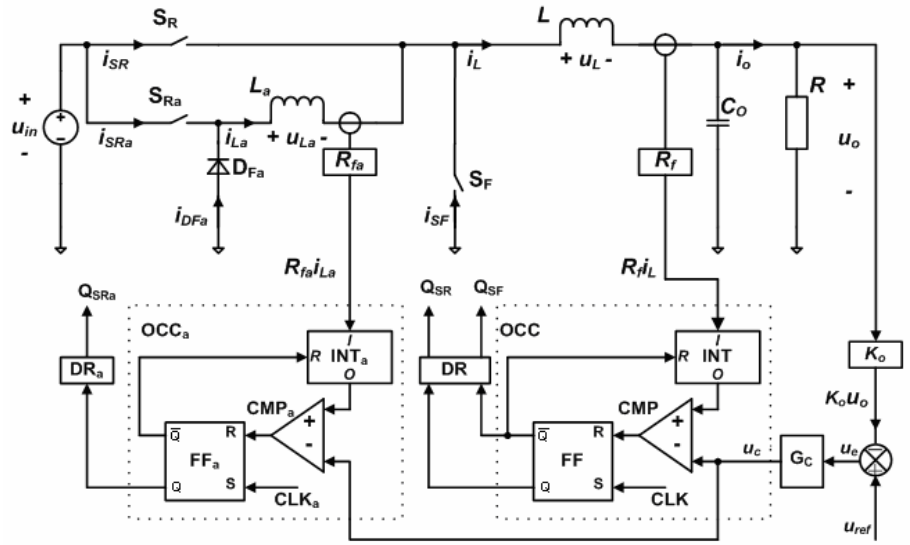


Fig. 1. The schematic of DCOCC controlled DF buck converter.

the efficiency of DF buck converter is improved.

- Unlike the average current control, there is only one voltage loop compensator and its design is very easy.
- The analog circuit to realize the controller is very simple.

In section II, the operation principle of the DCOCC controlled DF buck converter is described. In section III, the small signal models of a one cycle controller and a DF buck converter are presented, eventually, a system block diagram is established. The simulation and experimental verification are shown in section IV and section V, respectively. Finally, some conclusions are given in section VI.

In the following analysis, the capital letter represents the variable's quiescent value; the small letter represents the variable's instantaneous value, and $\hat{x}$ represents the variable's small ac variation.

II. The Operation Principle of DCOCC Controlled DF Buck Converter

Fig. 1 shows a schematic of the DCOCC controlled DF buck converter. There are two one cycle controllers in the schematic, a high frequency one cycle controller OCC and a low frequency one cycle controller OCCa. The sensed output voltage $K_o u_o$ is compared with the reference voltage u_{ref}. The difference between them is called the error voltage u_e, which is applied to the input of the voltage loop compensator G_c. The output of G_c is called the compensated voltage u_c, which is applied to the inverting input of the comparators COM and COMa. The sensed current $R_f i_L$ is applied to the input of the integrator with the reset INT. The output of the INT is connected to the non-inverting input of the COM and the output of the COM is connected to the reset input of the flip-flop FF. The clock pulse CLK at the set input of the FF determines the switching frequency of the high frequency switches S_R and S_F. The output of the FF is connected to the input of the driver DR and the output of the DR is the drive signals Q_{SR} and Q_{SF} for S_R and S_F, respectively. The inverting output of the FF is applied to reset the INT. Similarly, the drive signal Q_{SRa} for the low frequency switch S_{Ra} is derived. The frequencies f_H and f_L of the clock pulses CLK and CLKa are equal to the operation frequency of the high frequency BUCK cell and the low frequency BUCK cell, and f_H is much greater than f_L.

When the clock pulse CLK comes, the switch S_R is turned on and S_F is turned off, and the integrator INT begins to integrate the sensed current $R_f i_L$. The output of the comparator COM changes its state and triggers the flip-flop FF when the output of the INT reaches u_c. This in turn, turns on S_F, turns off S_R and resets the output of the INT to zero. The operation principle of the OCCa is the same as for the OCC described above.

The condition where the average values of i_L and i_{La} are controlled to be equal will be discussed in the following. It is assumed that the DF buck converter is working in continuous current mode (CCM), and that all of the power devices are ideal. Let the integration constants T_i and T_{ia} of the integrators INT and INTa be equal to the periods T_H and T_L of the clock pulses CLK and CLKa, respectively. That is:

$$T_i = T_H \quad T_{ia} = T_L \tag{1}$$

During the turn on of SR, i_L is:

$$i_L = I_L - \frac{u_{in} - u_o}{2L} dT_H + \frac{u_{in} - u_o}{L} t \ (0 \le t \le dT_H) \tag{2}$$

where d is the duty ratio of S_R.

During the turn on of S_{Ra}, i_{La} can be approximately expressed as:

TABLE I
SWITCHING STATES

State	Active Switches	
	S_R	S_{Ra}
a	ON	ON
b	OFF	ON
c	ON	OFF
d	OFF	OFF

$$i_{\mathrm{La}} \approx I_{\mathrm{La}} - \frac{u_{\mathrm{in}} - u_{\mathrm{o}}}{2L_{\mathrm{a}}} d_{\mathrm{a}} T_{\mathrm{L}} + \frac{u_{\mathrm{in}} - u_{\mathrm{o}}}{L_{\mathrm{a}}} t \ (0 \le t \le d_{\mathrm{a}} T_{\mathrm{L}}) \tag{3}$$

where d_a is the duty ratio of S_{Ra}.

According to [6], when the DF buck converter is in the steady state, the duty radios of S_R and S_{Ra} are equal to satisfy the voltage-second balance requirement of inductor L_a, which is assumed as d.

Referring to Fig. 1, the following can be obtained:

$$\frac{1}{T_{\mathrm{i}}} \int_0^{dT_{\mathrm{H}}} R_{\mathrm{f}} i_{\mathrm{L}} dt = \frac{1}{T_{\mathrm{ia}}} \int_0^{d_{\mathrm{a}} T_{\mathrm{L}}} R_{\mathrm{fa}} i_{\mathrm{La}} dt = u_{\mathrm{c}} \tag{4}$$

From (1), (2), (3), and (4), if the average values of i_L and i_{La}, denoted as I_L and I_{La}, are equal, the following equation must be satisfied:

$$R_{\mathrm{f}} = R_{\mathrm{fa}} \tag{5}$$

That is to say, if the sensor coefficients of i_L and i_{La} are equal, assumed as R_a, then the average value of i_L and i_{La} is controlled to be equal, which is assumed as I_a.

Based on the conditions described above, the operation principle of the DCOCC controlled DF buck converter is analyzed as follows. The key waveforms in one low frequency switching period are shown in Fig. 3, where f_H is three times f_L with the same duty cycle of 0.6. There are four switching states according to the status of the switches S_R and S_{Ra}, which are listed in Table I. State a denotes that both of the switches S_R and S_{Ra} are on and the equivalent circuit is shown in Fig. 2(a). In a similar manner, the equivalent circuits of states b, c, and d are shown in Fig. 2(b)-(d), respectively.

According to the operation principle of the DCOCC controlled DF buck converter described above, the average values of the low frequency inductor current i_{La} and the high frequency inductor current i_L are controlled to be equal with only one voltage loop compensator G_c. In the following, the small signal model of the DCOCC controlled DF buck converter is established to design the voltage compensator G_c.

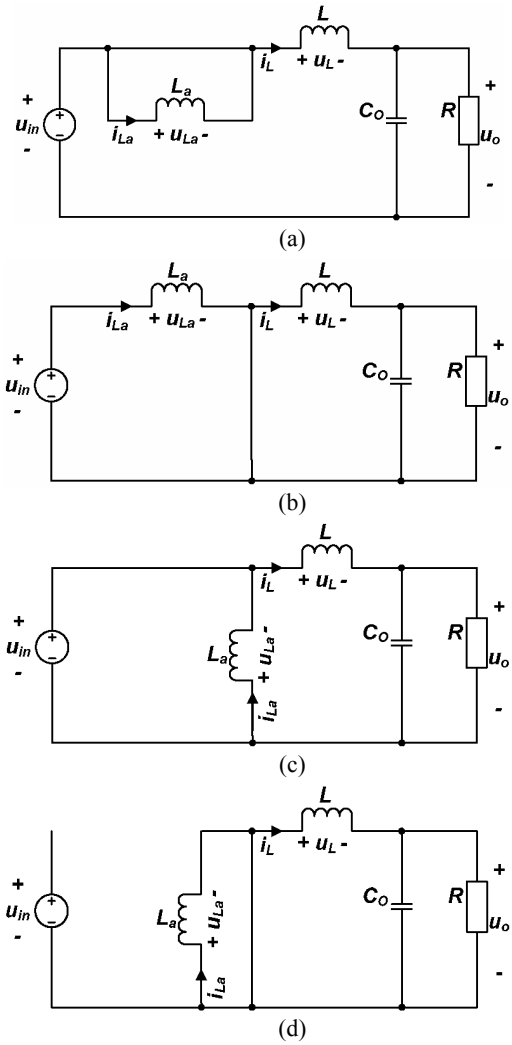


Fig. 2. Equivalent circuit in different switching states. (a) State a. (b) State b. (c) State c. (d) State d.

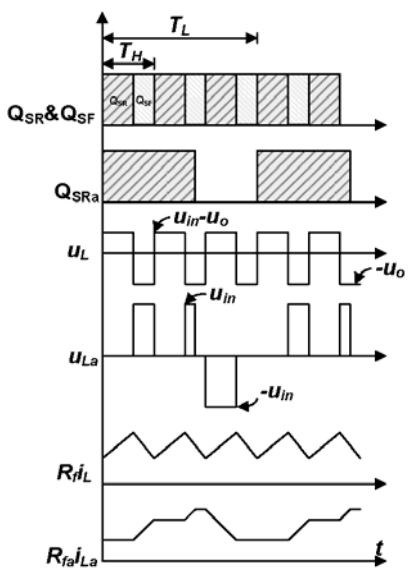


Fig. 3. Voltage and current waveforms in one low frequency switching period.

III. THE SMALL SIGNAL MODEL OF THE DCOCC CONTROLLED DF BUCK CONVERTER

Firstly, the small signal model of the one cycle controller is derived. Then this is done for the DF buck converter. Finally, the system block diagram of the DCOCC controlled DF buck converter will be established, and the transfer function for the input to output and the output impedance will be determined.

A. The Small Signal Model of the One Cycle Controller

Assuming that the ripples of i_L and i_{La} are very small, from (1), (4), and (5), the following can be obtained:

$$R_a i_L d = R_a i_{La} d_a = u_c \tag{6}$$

Perturb the variables in (6), that is:

$$\begin{aligned} i_L &= I_a + \hat{i}_L & i_{La} &= I_a + \hat{i}_{La} \\ d &= D + \hat{d} & d_a &= D + \hat{d}_a \\ u_c &= U_c + \hat{u}_c \end{aligned} \tag{7}$$

Substituting (7) into (6), and neglecting the second order nonlinear terms, the following is obtained:

$$R_a I_a D = U_c \tag{8}$$

$$R_a I_a \hat{d} + R_a D \hat{i}_L = R_a I_a \hat{d}_a + R_a D \hat{i}_{La} = \hat{u}_c \tag{9}$$

From (9):

$$\hat{d} = F_m\left(\hat{u}_c - F_L \hat{i}_L\right) \tag{10}$$

$$\hat{d}_a = F_m\left(\hat{u}_c - F_L \hat{i}_{La}\right) \tag{11}$$

where:

$$F_m = \frac{1}{R_a I_a} \tag{12}$$

$$F_L = R_a D \tag{13}$$

From (10) to (13), the block diagram of the one cycle controller is obtained, as shown in Fig. 4.

B. The Small Signal Model of the DF Buck Converter

Utilizing the state-space averaging method [11], the block diagram of the DF buck converter is established, as shown in Fig. 5, where:

$$G_{du} = \frac{\hat{u}_o}{\hat{d}} = U_{in} \frac{1}{LCs^2 + \frac{L}{R}s + 1} \tag{14}$$

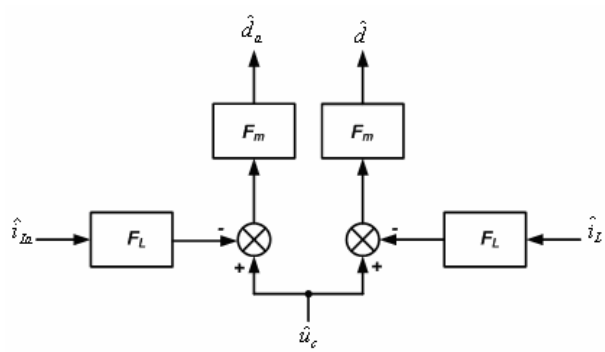


Fig. 4. The block diagram of the one cycle controller.

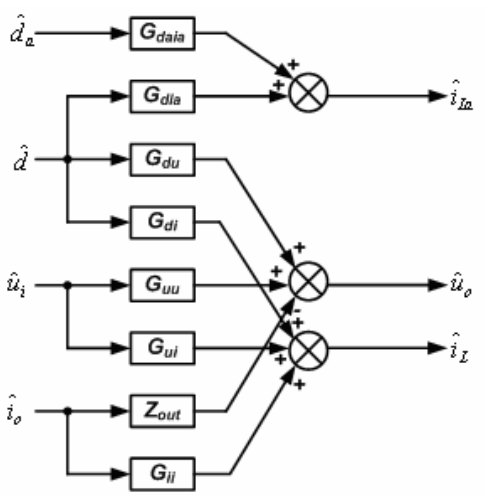


Fig. 5. The block diagram of the DF buck converter.

$$G_{uu} = \frac{\hat{u}_o}{\hat{u}_{in}} = D \frac{1}{LCs^2 + \frac{L}{R}s + 1} \tag{15}$$

$$Z_{out} = \frac{\hat{u}_o}{-\hat{i}_o} = \frac{Ls}{LCs^2 + \frac{L}{R}s + 1} \tag{16}$$

$$G_{di} = \frac{\hat{i}_L}{\hat{d}} = \frac{U_{in}}{R} \frac{RCs + 1}{LCs^2 + \frac{L}{R}s + 1} \tag{17}$$

$$G_{ui} = \frac{\hat{i}_L}{\hat{u}_{in}} = \frac{D}{R} \frac{RCs + 1}{LCs^2 + \frac{L}{R}s + 1} \tag{18}$$

$$G_{ii} = \frac{\hat{i}_L}{\hat{i}_o} = \frac{1}{LCs^2 + \frac{L}{R}s + 1} \tag{19}$$

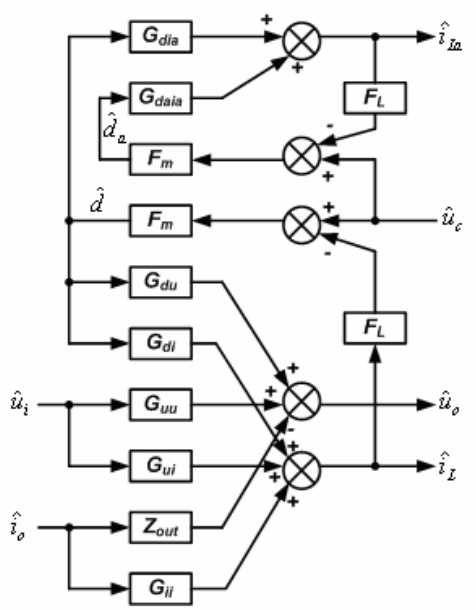


Fig. 6. The block diagram of the open loop DCOCC controlled DF buck converter.

$$G_{\mathrm{dia}}=\frac{\hat{i}_{\mathrm{La}}}{\hat{d}}=-\frac{U_{\mathrm{in}}}{L_{\mathrm{a}}s} \tag{20}$$

$$G_{\mathrm{daia}}=\frac{\hat{i}_{\mathrm{La}}}{\hat{d}_{\mathrm{a}}}=\frac{U_{\mathrm{in}}}{L_{\mathrm{a}}s} \tag{21}$$

C. The Small Signal Model of the DCOCC Controlled DF Buck Converter

Based on the block diagram of the one cycle controller and the DF buck converter, the open-loop block diagram of the DCOCC controlled DF buck converter is obtained, as shown in Fig. 6.

Utilizing the Mason equation, the following open-loop transfer function is established. The open-loop control-to-output transfer function is:

$$G_{\mathrm{cuo}}=\frac{\hat{u}_{\mathrm{o}}}{\hat{u}_{\mathrm{c}}}=\frac{F_{\mathrm{m}}G_{\mathrm{du}}}{1+F_{\mathrm{L}}F_{\mathrm{m}}G_{\mathrm{di}}}=\frac{\dfrac{RU_{\mathrm{in}}}{R_{\mathrm{a}}}}{I_{\mathrm{a}}R\left(LCs^{2}+\dfrac{L}{R}s+1\right)+DU_{\mathrm{in}}\left(RCs+1\right)} \tag{22}$$

The open-loop input-to-output transfer function is:

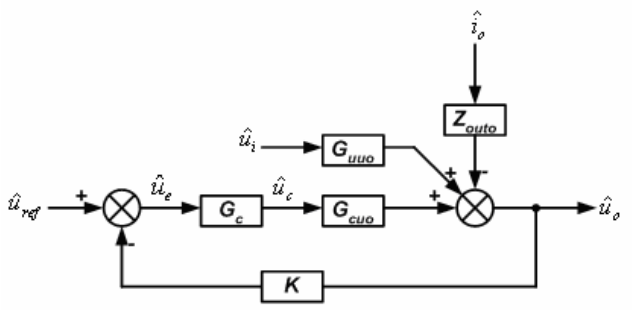


Fig. 7. The system block diagram of the DCOCC controlled DF buck converter.

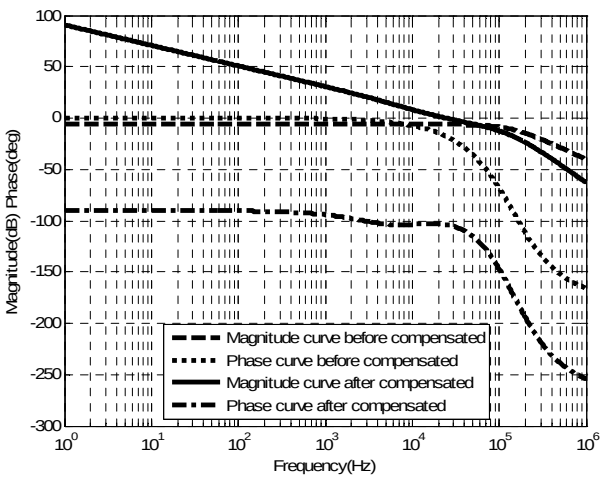


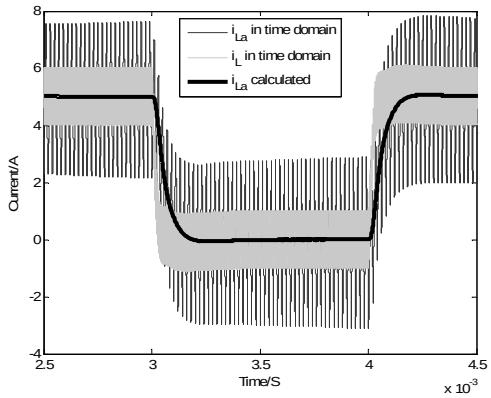
Fig. 8. The magnitude and phase curves of the loop gain T.

$$G_{\mathrm{uuo}}=\frac{\hat{u}_{\mathrm{o}}}{\hat{u}_{\mathrm{in}}}=G_{\mathrm{uu}}-\frac{F_{\mathrm{L}}F_{\mathrm{m}}G_{\mathrm{ui}}G_{\mathrm{du}}}{1+F_{\mathrm{L}}F_{\mathrm{m}}G_{\mathrm{di}}}=\frac{DRI_{a}}{I_{\mathrm{a}}R\left(LCs^{2}+\dfrac{L}{R}s+1\right)+DU_{\mathrm{in}}\left(RCs+1\right)} \tag{23}$$

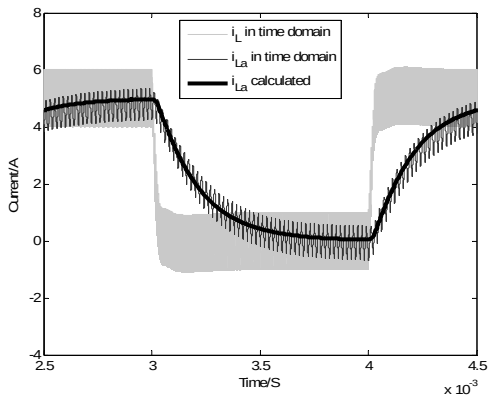
The open-loop output impedance is:

$$Z_{\mathrm{outo}}=\frac{\hat{u}_{\mathrm{o}}}{-\hat{i}_{\mathrm{o}}}=Z_{\mathrm{out}}+\frac{F_{\mathrm{L}}F_{\mathrm{m}}G_{\mathrm{ii}}G_{\mathrm{du}}}{1+F_{\mathrm{L}}F_{\mathrm{m}}G_{\mathrm{di}}}=\frac{R+Ls\left[\left(LCs^{2}+\dfrac{L}{R}s+1\right)+\left(RCs+1\right)\right]}{\left(LCs^{2}+\dfrac{L}{R}s+1\right)\left[\left(LCs^{2}+\dfrac{L}{R}s+1\right)+\left(RCs+1\right)\right]} \tag{24}$$

The transfer function from i_{L} to i_{La} is:

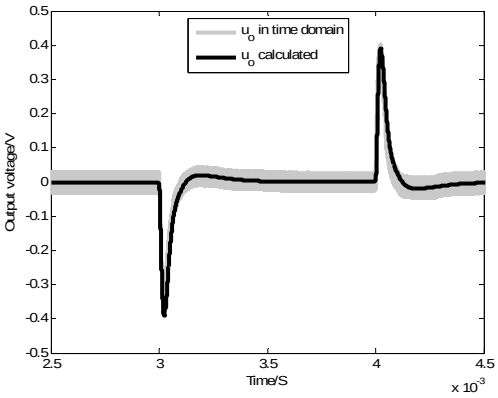


(a)

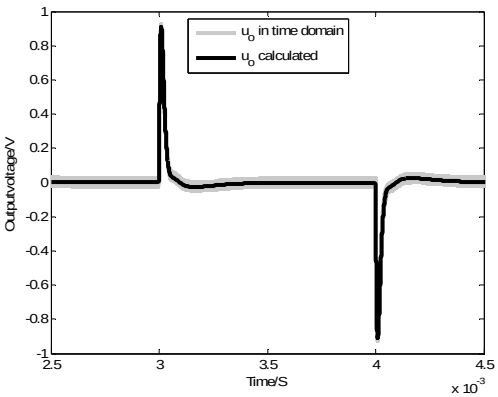


(b)

Fig. 9. The current waveforms through high frequency and low frequency inductors: (a) L_a=10μH. (b) L_a =50μH.



(a)



(b)

Fig. 10. The response waveforms of the output voltage: (a) Input voltage changing between 10V and 12V. (b) Load current changing between 20A and 25A.

$$G_{\text{iiao}} = \frac{\hat{i}_{\text{La}}}{\hat{i}_{\text{L}}} = \frac{-F_{\text{L}}F_{\text{m}}G_{\text{dia}}}{1+F_{\text{L}}F_{\text{m}}G_{\text{daia}}} = \frac{DU_{\text{in}}}{L_{\text{a}}I_{\text{a}}s+DU_{\text{in}}} \quad (25)$$

When the load current is changing, if i_{La} can keep up with i_{L} as quickly as possible, the current stress of the high frequency switches is lower, as are its switch losses. From (25), the smaller the value of L_a, the faster i_{La} keeps up with changes of i_{L}. However, if L_a is too small, the effect of shunting the current through the high frequency switches will be weakened. Therefore, there has to be a trade off between them.

Finally, the system block diagram of the DCOCC controlled DF buck converter is established, as shown in Fig. 7. As the disturbance of the reference voltage is nearly zero, the whole system can be treated as a two-input single-output system.

The loop gain of the system is:

$$T = KG_{\text{c}}G_{\text{cuo}} \quad (26)$$

The close loop input to the output transfer function is:

$$G_{\text{uuc}} = \frac{\hat{u}_{\text{o}}}{\hat{u}_{\text{in}}} = \frac{G_{\text{uuo}}}{1+T} \quad (27)$$

The close loop output impedance is:

$$Z_{\text{outc}} = \frac{\hat{u}_{\text{o}}}{-\hat{i}_{\text{o}}} = \frac{Z_{\text{outo}}}{1+T} \quad (28)$$

IV. SIMULATION VERIFICATION

The simulation parameters are as follows: U_{in}=10V, U_{o}=5V, R=0.25Ω, L=5μH, L_a=10μH, C=20μF, f_{H}=250kHz, f_{L}=50kHz, R_{f}=0.5, R_{fa} =0.5.

The traditional method described in [11] is used to design the voltage loop compensator G_c. After compensation, the cross frequency is 25kHz and the phase margin is 76°。The magnitude and the phase curves of the loop gain of the system before and after compensated are shown in Fig. 8.

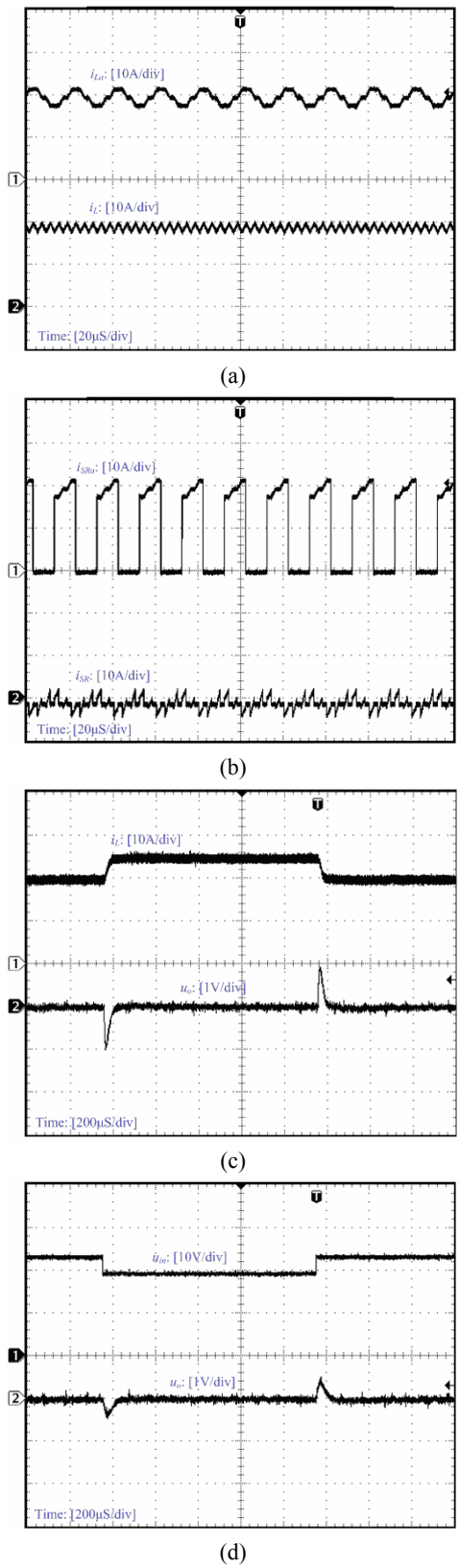


Fig. 11. Experimental waveforms: (a) i_L and i_{La}. (b) i_{SR} and i_{SRa}. (c) i_o and the response of u_o. (d) uin and the response of u_o.

Fig. 9(a) presents the simulation waveforms of i_L and i_{La} in the time domain and the calculated waveform of i_{La} based on G_{iiao} when the load current is changing between 20A and 25A and L_a=10μH. Fig. 9(b) shows the above waveforms when L_a=50μH. It can be seen that the simulation waveform of i_{La} in time domain approximately coincides with the calculated waveform. It can also be seen that the smaller the low frequency inductor L_a, the more quickly i_{La} can keep up with i_L, and the lower the current stresses of the high frequency switches S_R and S_f.

Fig. 10(a) shows the simulated output voltage waveforms in the time domain and the calculated output voltage waveform based on G_{uuc} when the input voltage is changing between 10V and 12V. Fig. 10(b) shows these two waveforms when the load current is changing between 20A and 25A. It can be seen that the simulated waveforms in the time domain coincide with those calculated, which verifies the correction of the theory analysis above.

V. EXPERIMENTAL VERIFICATION

The experimental parameters are almost the same as the simulation parameters. Fig. 11(a) shows the experimental waveforms of i_L and i_{La}. It can be seen that their average value is approximately equal. Fig. 11(b) shows the current waveforms of i_{SR} and i_{SRa}. Through S_R and S_{Ra}, it can be seen that the instantaneous value of i_{SR} is much smaller than i_{Sra}. Therefore, its switching losses are reduced. Fig. 11(c) shows the response of u_o when i_o is changing between 20A and 25A. Fig. 11(d) shows the response of u_o when u_{in} is changing between 10V and 12V. The experimental results are in accord with the simulation results.

VI. CONCLUSION

In this paper, a direct current control method based on the one cycle controller for a DF buck converter is proposed and the small signal model of it is established. Based on this model, the voltage loop compensator is designed. The simulation and experimental results have shown that:

- Adopting the DCOCC can make the average current through the high frequency and low frequency inductor equal. Therefore, the current stress and switching losses of the high frequency switches are minimized.
- The design of the voltage loop compensator is easy.
- The cross frequency and phase margin of the loop gain have no effect on the fact that the current through the low frequency inductor keeps up with the changing of the current through the high frequency inductor.

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