The Impact of Gate Leakage Current on PLL in 65 nm Technology: Analysis and Optimization

Jing Li, Ning Ning, Ling Du, Qi Yu, and Yang Liu

Abstract—**For CMOS technology of 65 nm and beyond, the gate leakage current can not be negligible anymore. In this paper, the impact of the gate leakage current in ring voltage-controlled oscillator (VCO) on phase-locked loop (PLL) is analyzed and modeled. A voltage -to-voltage (V-to-V) circuit is proposed to reduce the voltage ripple on V_{ctrl} induced by the gate leakage current. The side effects induced by the V-to-V circuit are described and optimized either. The PLL design is based on a standard 65 nm CMOS technology with a 1.8 V power supply. Simulation results show that 97 % ripple voltage is smoothed at 216 MHz output frequency. The RMS and peak-to-peak jitter are 3 ps and 14.8 ps, respectively**

Index Terms—**Phase-locked loop, jitter, ring voltage-controlled oscillator, voltage-to-voltage circuit, gate leakage current**

I. INTRODUCTION

PLL is a negative-feedback system which produces low-phase-noise and low-jitter frequency. Fig. 1 illustrates the traditional architecture of a charge pump PLL. It consists of a phase/frequency detector (PFD), a charge pump (CP), a second order low-pass loop filter (LPF), a ring voltage-controlled oscillator (VCO) and a frequency divider.

With the rapid increase of integration density and system complexity, noise cancelling in PLL becomes more and more important. The major source of noise in PLL originates from VCO. When designing a high-precision PLL, the main task is to reduce the phase noise induced by VCO. As described in [1], differential delay buffer cell with cross-coupled loads may reduce phase noise as it has a better symmetry.

However, with the feature size of device scaling down, the gate leakage current of MOS transistors becomes a non-negligible factor which may induce noise in PLL and lead to higher power consumption. Recently, some studies have been reported on this subject [2-4]. But all of them focused on the gate leakage current induced by MOS capacitors in the LPF and the gate leakage in the MOS transistors in ring VCO was not concerned with. In this paper, a model of gate leakage current has been built to study the influence of the gate leakage current in VCO on the jitter characteristics of the PLL. A voltage-to-voltage (V-to-V) converting circuit is proposed to smooth the voltage ripple and improve the jitter performance of the PLL.

II. GATE LEAKAGE CURRENT MODELING AND OPTIMIZATION

1. Modeling

Ideally, during the locked state, the ripple on the control voltage (V_{C1}) is very small. However, the gate leakage current (I_{leak}), as shown in Fig. 1, may discharge the LPF and consequently modifies the control voltage (V_{C1}) in the time frame in each locked cycle ($T=1/f_{ref}$, where f_{ref} is the input reference frequency). And thus the gate leakage current will result in a big period ripple

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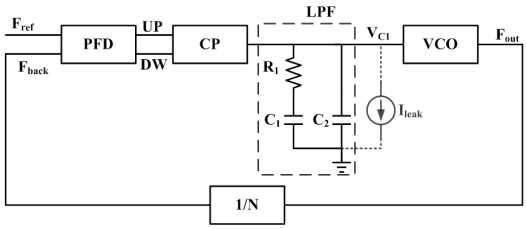

Fig. 1. Traditional PLL architecture.

(ΔV_{C1}) on the control voltage.

$$Jitter \propto \Delta V_{C1} \times K_{vco} \tag{1}$$

According to Eq. (1), jitter is proportional to ΔV_{C1}. Thus, to achieve a low-jitter and high-precision PLL, the gate leakage current should be reduced to the minimum.

In a PLL, the gate leakage current which may take effect on the control voltage (V_{C1}) can be divided into two parts: one part is induced from the MOS capacitors in the LPF, and the other part is caused by MOS transistors whose gates are connected to the node V_{C1} in VCO.

Normally the gate leakage current is proportional to the size of the MOS transistor and thus the gate leakage current originated from the MOS capacitors in the LPF is critical. In advanced CMOS technologies, i.e. 65 nm and beyond, the MOS capacitors can be realized by NMOS transistors which are implemented in N-well. The gate leakage current of transistor is not serious as its gate oxide is much thicker than that of normal device. Therefore, the present work focuses on the other origin of gate leakage current, which is induced by the MOS transistors with their gates connected with the node V_{C1} in VCO.

Fig. 2 shows the five-stage ring VCO and the delay cell used in this design. It is similar to the architecture described in [1]. M1 and M2 are the input differential pair. M3 and M4 constitute the cross-coupled load to produce the negative resistance. M5 and M6 are controlled by V_{C1} to regulate the output resistance. M7 is the current source whose gate is biased by Vb. In 65-nm CMOS technology, all the transistors are suffered from the gate leakage current. But only M5 and M6 are connected with and will influence the control voltage V_{C1}.

The LPF model when PLL is locked is shown in Fig. 3 To simplify the analysis, the gate leakage current on each

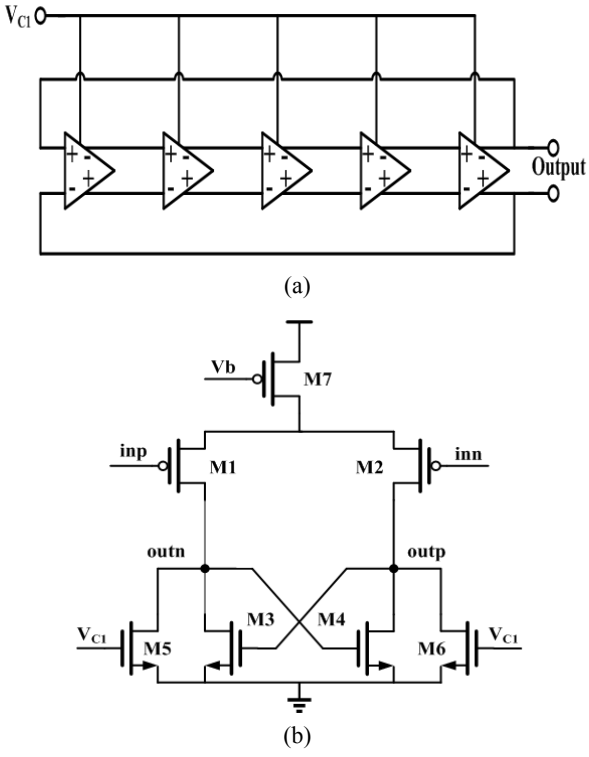

Fig. 2. (a) VCO block diagram, (b) Delay cell of one stage.

transistor is assumed to be constant and identical, and I_{leak} is defined as the total gate leakage current induced in VCO. According to the analysis of the RC circuit in Fig. 3 (b), the control voltage (V_{C1}) can be expressed as

$$V_{C1}(t) = V_{C1}(0) - \left[\frac{I_{leak} t}{C_1 + C_2} + \frac{C_1 I_{leak} \tau}{C_2 (C_1 + C_2)} \left(1 - e^{-\frac{t}{\tau}} \right) \right] \tag{2}$$

where $\tau = R_1 C_1 C_2 / (C_1 + C_2)$; and $V_{C1}(0)$ is the ideal lock voltage. As the period of locked cycle is very short and in the range of dozens of nanoseconds, Eq. (2) can be expressed with Taylor's expansion for the exponential term. Finally the control voltage (V_{C1}) can be simplified as following:

$$V_{C1}(t) \approx V_{C1}(0) - \frac{I_{leak} t}{C_2} \tag{3}$$

The control voltage V_{C1} is simulated based on the proposed model in Eq. (2) by Matlab. Fig. 4 shows the ripple (ΔV_{C1}) on V_{C1} is about 2.062 mV.

According to Eq. (3) and Fig. 4, the control voltage

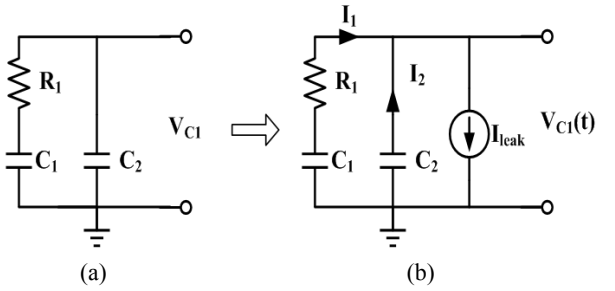

Fig. 3. (a) LPF model without gate leakage current, (b) with gate leakage current.

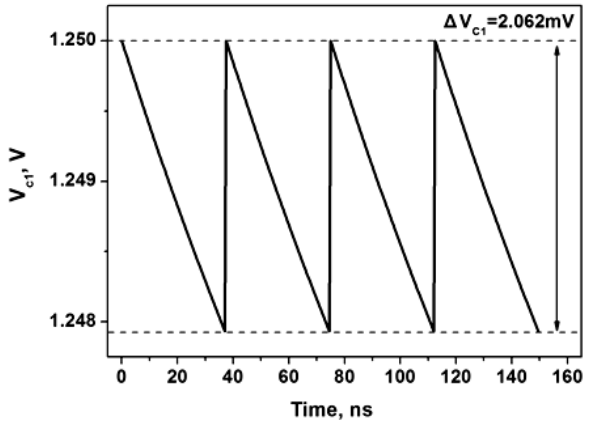

Fig. 4. Voltage ripple caused by the gate leakage current.

(V_{C1}) will fall down linearly in every locked period. The ripple voltage (ΔV_{C1}) is proportional to the gate leakage current (I_{leak}) and inversely proportional to the capacitance C_2. One of the methods to reduce the variation of the control voltage is to increase C_2. However, it is not easy to realize as the stability of the PLL strongly depends on the magnitude of C_2. Therefore, the reduction of the gate leakage current (I_{leak}) seems to be the possible approach.

2. Proposed PLL with V-to-V circuit

As mentioned above, the gate leakage in VCO results in a triangle ripple on the control voltage and thus deteriorates the jitter performance of the PLL. The reduction of the gate leakage becomes the bottleneck when designing a high-precision PLL. As the gate leakage current is proportional to the size of the MOS transistor, reduction of the amount and size of MOS transistors, whose gates are connected with the node V_{C1}, will be an effective way to reduce the gate leakage

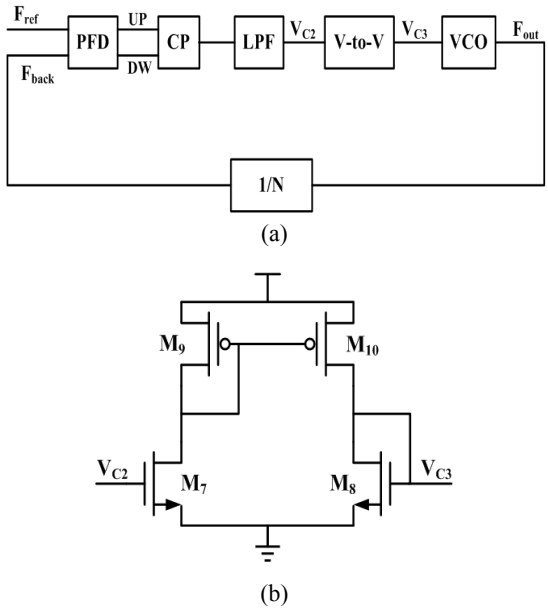

Fig. 5. (a) Proposed PLL with V-to-V converting circuit, (b) Implementation of V-to-V converting circuit.

current. Regarding this, a voltage-to-voltage (V-to-V) converting circuit is proposed as shown in Fig. 5.

The V-to-V converting circuit is an amplifier. If all the devices are perfectly matched, V_{C2} should be equaled to V_{C3} as illustrated in Fig. 5(b). Obviously, there is only one NMOS transistor M7 connected with V_{C2} in Fig. 5 (b), much less than the amount (normally 2•M transistors, where M is the stage of the delay cell in VCO) in the conventional PLL. Therefore, the gate leakage current on the node V_{C2} will be greatly reduced. Although the gate leakage current in VCO still exists and is connected to the node V_{C3}, it will be compensated by the current source M_4 and will not take much effect on the node voltage V_{C3}. Therefore, the V-to-V circuit can reduce the variation of the node voltage V_{C2} and improve the jitter performance of the PLL.

3. Noise analysis

However, the node voltage V_{C3} will be changed by the thermal noise in the devices forming the V-to-V circuit and the kickback noise coming from the VCO, causing timing jitter. The kickback noise can be filtered by adding a capacitor at the node V_{C3} while the thermal noise can not be eliminated.

The schematic of the V-to-V cell is presented in Fig. 6 with thermal noise sources. Similar to the first pass

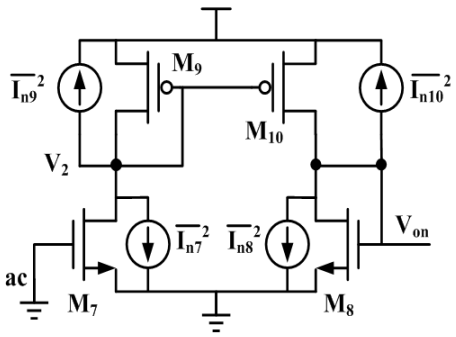

Fig. 6. V-to-V converting circuit with thermal noise.

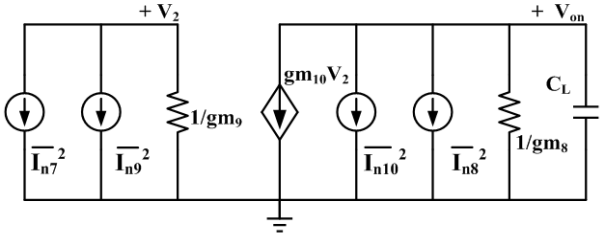

Fig. 7. Simplified small-signal equivalent circuit for V-to-V.

analysis in [5], the noise sources are assumed to be constant, with values given by the condition where the node voltage V_{C2} is biased with zero differential input. A simplified small-signal equivalent circuit for the V-to-V circuit is shown in Fig. 7.

As the noise sources are independent, the noise can be added together by power spectrum density [6]:

$$\overline{V_{on}}^2 = \int_0^\infty \overline{I_{n7}}^2(f)\left|H_7(f)\right|^2 + \cdots + \overline{I_{n10}}^2(f)\left|H_{10}(f)\right|^2 df \quad (4)$$

where $\overline{I_{ni}}^2(f)$ (i=7, 8, 9, 10) are the noise power spectral densities for transistors M_i (i=7, 8, 9, 10) in the V-to-V circuit (Fig. 5) and $H_i(f)$ (i=7, 8, 9, 10) are the transfer functions for those noise sources referred to the output. Using the noise expression in Eq. (4), the noise contribution of M_7 is given by:

$$\overline{V_{on7}}^2 = \int_0^\infty 4kT\gamma_7 gm_7 \left|\frac{gm_{10}}{gm_9}\frac{1}{gm_8 + sC_L}\right|^2 df \quad (5)$$

where γ is a function of V_{DS} and C_L is the load capacitance of the node V_{C3}. If the -3dB bandwidth of the RC circuit in Fig. 7 is defined as:

$$f_0 = \frac{gm_8}{2\pi C_L} \quad (6)$$

Eq. (5) can be simplified as:

$$\overline{V_{on7}}^2 = 4kT\gamma_7 gm_7 \left(\frac{gm_{10}}{gm_8 gm_9}\right)^2 \int_0^\infty \left|\frac{1}{1 + jf/f_0}\right|^2 df \quad (7)$$

The definite integral in Eq. (7) is commonly encountered in noise analysis. As described in [7], its value is $\pi/2 \cdot f_0$. Therefore, the simplified form of $\overline{V_{on7}}^2$ is given by:

$$\overline{V_{on7}}^2 = \frac{kT\gamma_7}{C_L}\frac{gm_7}{gm_8}\left(\frac{gm_{10}}{gm_9}\right)^2 \quad (8)$$

Similarly, the noise contribution of other MOS transistors can be concluded.

$$\overline{V_{on8}}^2 = \frac{kT\gamma_8}{C_L} \quad (9)$$

$$\overline{V_{on9}}^2 = \frac{kT\gamma_9}{C_L}\frac{gm_{10}{}^2}{gm_8 gm_9} \quad (10)$$

$$\overline{V_{on10}}^2 = \frac{kT\gamma_{10}}{C_L}\frac{gm_{10}}{gm_8} \quad (11)$$

Substitute Eqs. (8-11) into Eq. (4) and assume that $gm_7=gm_8=gm_9=gm_{10}$, then the total output voltage noise is given by:

$$\begin{aligned}\overline{V_{on}}^2 &= \overline{V_{on7}}^2 + \overline{V_{on8}}^2 + \overline{V_{on9}}^2 + \overline{V_{on10}}^2 \\ &= \frac{kT(\gamma_7 + \gamma_8 + \gamma_9 + \gamma_{10})}{C_L}\end{aligned} \quad (12)$$

From Eq. (12), we can conclude that the total thermal noise caused by the V-to-V circuit is inversely proportional to the load capacitance C_L. Thus, a large C_L is preferred to reduce both thermal noise and kickback noise.

4. Stability analysis

Primarily, the charge pump PLL with a second-order low-pass filter can be a stable system by regulating the value of R_1, C_1 and C_2. When the V-to-V circuit is added, an extra pole will be produced which could affect the stability of the PLL.

Z(s) and Y(s) are assumed to be the transfer function of the second-order low-pass filter and the V-to-V circuit, respectively. The expressions are given by:

$$Z(s) = \frac{1 + sR_1C_1}{s^2R_1C_1C_2 + s(C_1 + C_2)} \tag{13}$$

$$Y(s) = \frac{gm_7gm_{10}}{gm_8gm_9\left(1 + sC_L / gm_8\right)} \tag{14}$$

where gm_i (i=7, 8, 9, 10) is the transconductance of transistors M_i (i=7, 8, 9, 10) in the V-to-V circuit; and C_L is the load capacitance of the node V_{C3}.

Therefore, the open-loop transfer function of the PLL can be described as:

$$\begin{aligned} H(s) &= \frac{1}{N}\frac{I_{cp}\cdot Z(s)\cdot Y(s)\cdot K_{vco}}{2\pi s} \\ &= \frac{I_{cp}K_{vco}gm_7gm_{10}}{2\pi NC_Lgm_9}\frac{1 + sR_1C_1}{s^2\left(sR_1C_1C_2 + C_1 + C_2\right)\left(s + gm_8 / C_L\right)} \end{aligned} \tag{15}$$

Obviously, the extra pole is at w_0 ($=gm_8/C_L$). To reduce its impact on the phase margin of the PLL, w_0 should be at least 10 times larger than w_u (the frequency at the gain crossover point). Thus a smaller magnitude of C_L is preferred.

However, as described in the former section, the total thermal noise caused by the V-to-V circuit is inversely proportional to the load capacitance C_L. A larger C_L may do well in reducing both kickback noise and thermal noise on the node V_{C3}. Considering above factors, the value of C_L should be optimized to balance the phase margin and the noise performance.

III. SIMULATION RESULTS

The proposed charge pump PLL with V-to-V circuit is designed in a 65 nm CMOS process. The design parameters and post-layout-simulation results are shown in Table 1. In order to focus on the effect of gate leakage current, noises from circuits, such as power supply noise, substrate noise and reference noise, are not considered. To minimize the kickback noise and thermal noise on the node V_{C3} and keep the loop stable, the load capacitance C_L is optimized to 20 pF. The MOS capacitances C_1 and C_2 are 208 pF and 16 pF, respectively. The charge pump current is set to 20 uA to reduce the power consumption.

Table 1. The design parameters and simulation results of the proposed PLL with V-to-V circuit

Design parameters		Simulation results	
R_1	16 KΩ	VCO gain	266 MHz/V
C_1	208 pF	Bandwidth	160 KHz
C_2	16 pF	Phase Margin	56.8º
C_L	20 pF	Lock time	24.2 μs
Supply voltage	1.8 V	Static phase error	195.8 ps
Input frequency	27 MHz	Period Jitter(rms)	3.0 ps
Output frequency	216 MHz	Period Jitter(PP)	14.8 ps
Charge pump current	20 μA	Power consumption	6.3 mW

To identify the noise contribution made by the V-to-V circuit, the phase noise of VCO is simulated. As shown in Fig. 8, phase noise in VCO with V-to-V circuit is slightly worse than the original one. At the frequency of 1MHz, the reduction is 3 dB. In the whole frequency region, the difference is less than 5 dB which indicates that the noise contributed by the V-to-V circuit will do little effect on PLL's performance.

The stability of the PLL with V-to-V circuit is analyzed by Matlab. Fig. 9 shows the open loop analysis of the proposed PLL with the V-to-V circuit. As observed in this figure, the bandwidth is 160 KHz, the

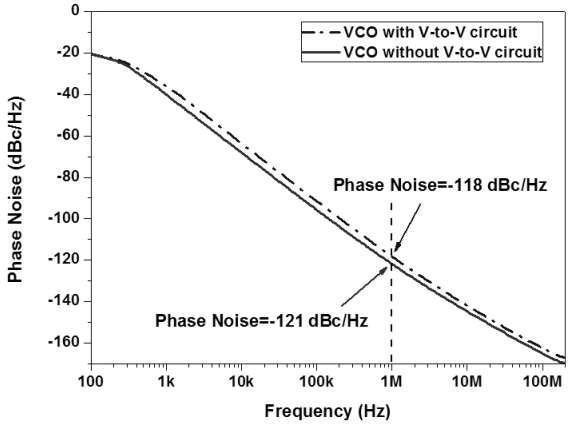

Fig. 8. Phase Noise analysis.

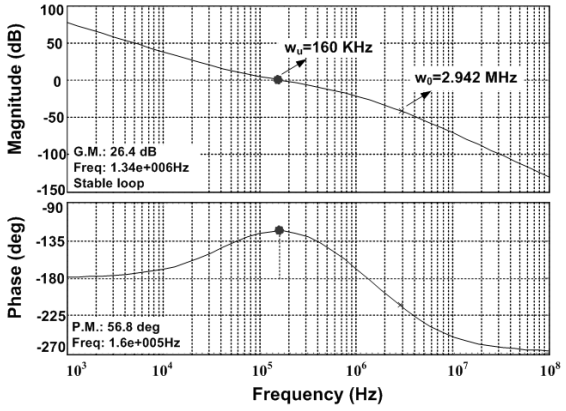

Fig. 9. Stability analysis.

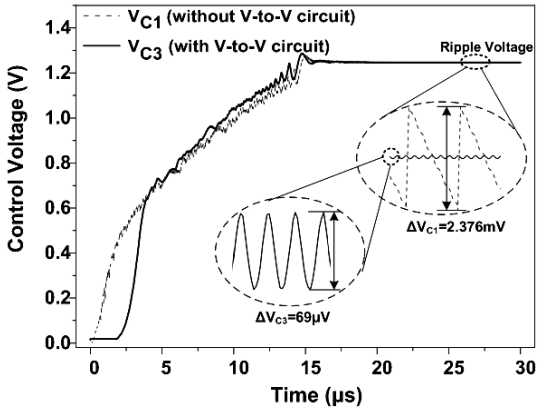

Fig. 10. Comparison of the ripples on the control voltage for PLL with and without V-to-V circuit.

extra pole w_0 is 2.942 MHz, and the phase margin is 56.8 degree. It indicates that the PLL can work in stable loop by proper design with the V-to-V circuit.

To find out the impact of gate leakage current in VCO on the PLL performance and verify the proposed model, the PLL with and without V-to-V circuit are both simulated. As shown in Fig. 10, V_{C1} and V_{C3} stand for the transition waveforms of the control voltage for the PLL with and without V-to-V circuit, respectively. The ripple voltage on V_{C1} fall down linearly in every locked period which quite agrees with the proposed model in Eq. (2) and Fig. 4. The value of ΔV_{C1} is 2.376 mV which is close to 2.062 mV calculated by the proposed model. Compared with the ripple voltage of ΔV_{C1}, the ripple voltage ΔV_{C3} is only 69 μV. 97% ripple voltage is eliminated at the output frequency of 216 MHz.

As shown in Fig. 11, the static phase error in the PLL with V-to-V circuit is 195.8 ps which is reduced by 90.3% of that for PLL without V-to-V circuit.

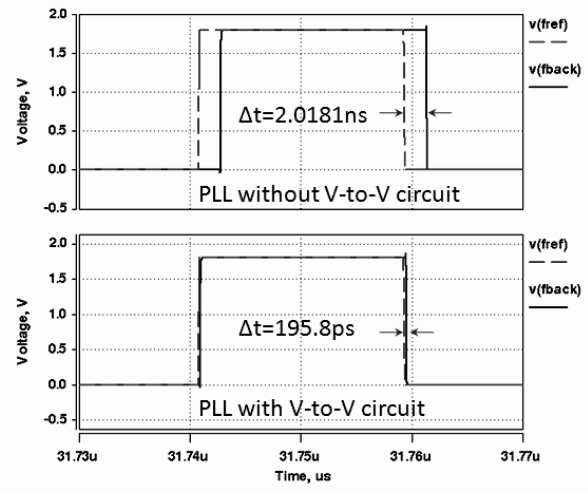

Fig. 11. Comparison of the static phase error (Δt) for PLL with and without V-to-V circuit.

Table 2. Comparison of key parameters between PLL with and without V-to-V circuit

Parameter	Without V-to-V circuit	With V-to-V circuit
Ripple voltage	2.376 mV	69 μV
Static phase error	2.0181 ns	195.8 ps
rms jitter	4.8 ps	3.0 ps
peak-to-peak jitter	22.3 ps	14.8 ps

The key performances are listed in Table 2. The root-mean-square (rms) jitter is 3.0 ps and the peak-to-peak jitter is about 14.8 ps in the PLL with V-to-V circuit. Both of the two parameters are much better than those for the PLL without V-to-V circuit.

IV. CONCLUSIONS

A V-to-V circuit is proposed to reduce the impact of the gate leakage in VCO on the PLL performance. The proposed charge pump PLL with V-to-V circuit is designed in a 65 nm CMOS process. The post-layout-simulation shows that both the ripple voltage and the static phase error are reduced for more than 90%. The jitter performance of the PLL with V-to-V circuit is greatly improved while the loop stability remains unchanged. The proposed design provides a useful guideline for implementation of high-precision PLL.

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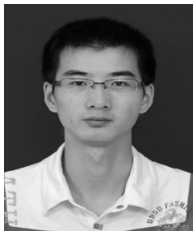

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