Design of CMOS Op Amps Using Adaptive Modeling of Transistor Parameters

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Abstract—A design paradigm using sequential geometric programming is presented to accurately design CMOS op amps with BSIM3. It is based on new adaptive modeling of transistor parameters through the operating point simulation. This has low modeling cost as well as great simplicity and high accuracy. The short-channel dc, high-frequency small-signal, and short-channel noise models are used to characterize the physical behavior of submicron devices. For low-power and low-voltage design, this paradigm is extended to op amps operating in the subthreshold region. Since the biasing and modeling errors are less than 0.25%, the characteristics of the op amps well match simulation results. In addition, small dependency of design results on initial values indicates that a designed op amp may be close to the global optimum. Finally, the design paradigm is illustrated by optimizing CMOS op amps with accurate transfer function.

Index Terms—CMOS op amp design, subthreshold region design, sequential geometric programming, adaptive transistor parameter modeling, short-channel weak inversion noise model

I. INTRODUCTION

Operational amplifiers are widely used analog circuit cells in mixed-signal integrated circuits. Design of high-performance complementary metal-oxide-semiconductor (CMOS) operational amplifiers (op amps) becomes more critical in low-power and low-voltage circuits. Moreover, transistor models have become more complex to characterize the physical behavior of submicron devices at high frequencies. As a result, analog circuit design consumes a significant portion of the total design time for mixed-signal integrated circuits. In order to enhance design productivity, various approaches have been presented for analog circuit design [1].

Analog circuit design by geometric program (GP) has the important advantages that *globally optimal circuits* can be designed and *infeasible constraints* can be identified. But this approach also has the limitation that design equations should be expressed as monomials or posynomials. Such expressions are possible only for special models like the square-law model. For this model, it has been shown that a CMOS op-amp design problem is formulated as a standard GP [2, 3]. For higher-order standard device models such as BSIM3, approximate approaches have to be used in the monomial or posynomial modeling. As a result, the discrepancy between the design and simulation results is inherent. In order to reduce this discrepancy and pursue the globally optimal property of GP, analog circuit design can be modeled as finding a solution by iteratively developing and solving approximate GPs. This is called sequential geometric programming (SGP) [3, 4].

GP modeling approaches for analog circuit design via SGP can be divided into two main categories for fitting *circuit performances* [4, 5] and *transistor parameters* [6-11]. Because typical op amp performances can be formulated as functions of transistor parameters, op amps can be designed using transistor parameters. In [4] and

[5], there is no need to derive such circuit performances. They are modeled by the local or *global prefitting* to huge simulation data before solving a GP. Since all performances can not be modeled accurately over the entire design space, SGP instead of a single GP can be used to reduce modeling error. In [6-9], transistor parameters are modeled by the piecewise or global prefitting to many data points obtained by sweep simulations over the size and bias of a transistor. Then a single GP is solved without iteration. The approach [10] use the piecewise prefitting in the overdrive voltage ranges. Owing to nonmonomial factors to model the v_{ds} effect, SGP is used. In [11], transistor parameters used in SGP are indirectly calculated using the model parameters analytically obtained from performance comparision.

The proposed transistor parameter modeling uses the *timely fitting* for a design point instead of piecewise or global prefitting over a large design space. But all transistor parameters including bias currents are directly fitted by simple division from transistor parameters simulated at a design point without performance comparision. So there is no need to simulate op amp performances. To model transistor parameters, the operating point is simulated just once every iteration. As a result, it has low modeling cost as well as great simplicity and high accuracy. The small modeling error of 0.25% improves accuracy 10 times comparing with published results. This efficient fitting is called *adaptive modeling* of transistor parameters. Therefore this new modeling can be usefully used in initial sizing, design tuning, and optimal design of op amps.

In this paper, a design approach using SGP will be presented to accurately design CMOS op amps with BSIM3. It is based on the proposed adaptive modeling of monomial transistor parameters. Thus there is no initial simulation cost for setting up the design paradigm. Monomial transistor parameters are associated with a short-channel transistor model. So updated some fitting parameters are used in the transistor model to match transistor parameters between geometric program and operating point simulation. For low-power design, this concept will be extended to transistors with exponential characteristic in the subthreshold region. In addition, a simple noise model is suggested to consider both weak inversion and velocity saturation in short-channel devices [12]. Finally, the design paradigm will be illustrated by

optimizing a two-stage op amp and a fully differential folded-cascode op amp with each transfer function accurately derived for the high-frequency model.

II. SEQUENTIAL GEOMETRIC PROGRAMMING

GP is a nonlinear optimization problem of the special form with monomials or posynomials. A monomial is defined as $g_i(x) = c_i x_1^{a_{i1}} x_2^{a_{i2}} \cdots x_n^{a_{in}}$ where $x = (x_1, x_2, \cdots x_n)$ are positive design variables and c_i is a positive coefficient, but the exponents a_{ij} are real constants. A posynomial $f(x)$ is defined as sum of monomials. If coefficients c_i are allowed to be negative, then $f(x)$ becomes a signomial. Typically, a standard GP can be formulated as

$$\begin{aligned} &\text{minimize } f_0(x) \\ &\text{subject to } f_i(x) \leq 1, \ i = 1, \cdots, \text{p} \\ &\qquad\qquad g_i(x) = 1, \ i = 1, \cdots, \text{q} \end{aligned} \qquad (1)$$

where f_0 is the objective function, f_i are inequality constraints, and g_i equality constraints. The GP can be transformed into a convex form by logarithmic change of variables and logarithmic transformation of the objective and constraint functions [13]. Then the globally optimal solution of this convex GP can be easily obtained by efficient methods [14, 15].

Generally, op-amp design problem involves nonposynomials in circuit performances. Thus such design problem is not a standard GP, but it can be modeled as a standard GP by fitting nonposynomials to posynomials. Moreover, there are no monomial transistor parameters for higher-order device models. But these parameters can be obtained by fitting transistor parameters at a design point to monomials. To reduce the fitting or modeling error, the design problem should be solved by SGP. If the design problem is not too far from a standard GP, it will work well in practice for a good starting point.

The design flow of op amps using SGP is shown in Fig. 1. The design specs routine initializes fitting parameters. The necessary model parameters such as XJ, TOX, LINT, CJ, and CJSW are inputted by parsing the op-amp circuit file with the method given in Appendix. With these parameters in the adaptive modeling routine, monomial
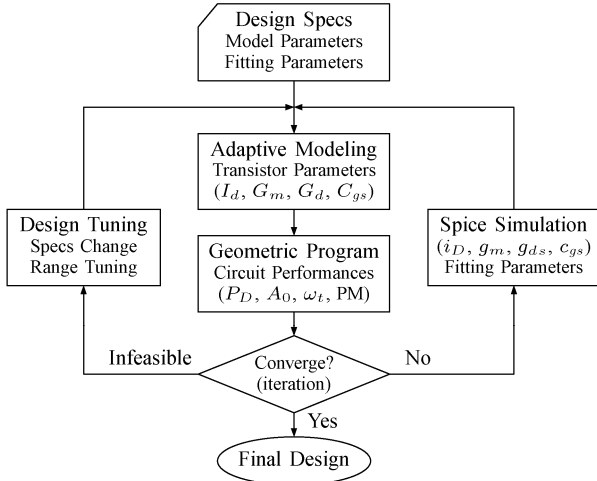
Fig. 1. Design flow of op amps using sequential geometric programming.

transistor parameters consisting of bias and small-signal parameters are obtained for every transistor in an op amp circuit. Using these transistor parameters in circuit performances, a GP is formulated and solved in the geometric program routine. When convergence is not achieved, a resultant circuit file is simulated, transistor parameters such as i_D, g_m, g_{ds}, and c_{gs} are accepted by parsing the output file of Spice, and the fitting parameters are updated. Then this process is repeated. If a design is infeasible, redesign can be performed through tuning infeasible constraints, the ranges of transistor sizes, and design specifications.

III. DESIGN PARADIGM IMPLEMENTATION

To implement the design paradigm accurately, the adaptive modeling of transistor parameters independent of op amp circuits will be described with short-channel dc, high-frequency small-signal, subthreshold, and short-channel noise models.

1. Short-Channel DC Model

The most important short-channel effect comes from velocity saturation of carriers in the channel. This significantly changes the square-law characteristic in the saturation region. The drain current and overdrive voltage with velocity saturation factor ρ and bulk charge factor α can be obtained as

$$i_D = \frac{\mu C_{ox}}{2\alpha}\frac{W}{L}\frac{v_{OV}^2}{(1+\rho)}, \quad \rho \equiv \frac{v_{OV}}{\alpha V_C} \quad (2)$$

$$v_{OV} = v_{GS} - v_t = \alpha v_{Dsat}(1 + \rho) \quad (3)$$

where v_{Dsat} is the drain saturation voltage, α is given by $(1 + g_{mb}/g_m)$, and the critical voltage V_C and electric field E_C are related by $V_C \equiv LE_C$ [16]. Assuming constant V_C in above equations, the transconductance can be found as

$$g_m = \mu C_{ox}\frac{W}{L}\frac{v_{OV}}{\alpha}\frac{(1+\rho/2)}{(1+\rho)^2} \quad (4)$$

When velocity saturation is significant, $\rho \gg 1$. Then $i_D = C_{ox}W v_{sat}v_{OV}$ where the saturation velocity $v_{sat} = \mu E_C/2$. This shows that the drain current is a linear function of the overdrive voltage, then the transconductance is independent of v_{OV} and L. When velocity saturation is neglected or $\rho \ll 1$, the drain current is expressed as the square-law model.

2. High-Frequency Small-Signal Model

Spice directly solves for small-signal voltages and currents using the large-signal equations of BSIM3. But a small-signal equivalent circuit is needed to obtain the frequency responses for op amp design. A simplified high-frequency small-signal model shown in Fig. 2 can be used in signal analysis of op amp circuits [17]. Here complex transconductance is given by $g_m^* = g_m - sC_m$ where s is complex frequency and transcapacitance C_m is $(C_{dg} - C_{gd})$. These capacitances include extrinsic capacitances like overlap or junction capacitances. Spice usually reports these total capacitances at a bias point.
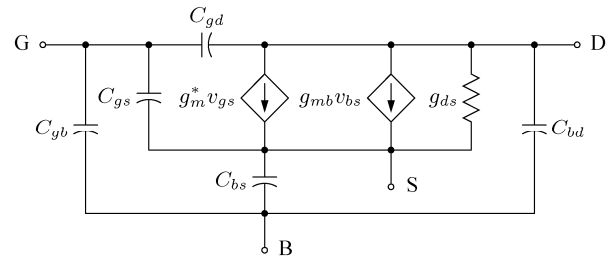

Fig. 2. A simplified high-frequency MOSFET model with complex transconductance.

3. Adaptive Modeling of Transistor Parameters

Adaptive monomial modeling will be described for transistor parameters independent of circuit topology. At a bias or design point, the characteristics of transistors can be approximated as those of the short-channel model with fitting parameters. From Eqs. (2, 4) and the drain bias current I_d, monomial transistor parameters like transconductance G_m, overdrive voltage V_{ov}, and drain conductance G_d can be modeled as

$$G_m = \frac{(1 + \rho/2)}{(1 + \rho)^2} \left[\frac{2k_p I_d (W/L)}{\alpha(1 + \rho)} \right]^{1/2} \quad (5)$$

$$V_{ov} = k_v \left[\frac{2\alpha I_d (1 + \rho)}{k_p (W/L)} \right]^{1/2} \quad (6)$$

$$G_d = \lambda_d I_d \quad (7)$$

where $k_p \propto \mu C_{ox}$, k_v, and λ_d are fitting parameters. For these transistor parameters to be monomials, the factors α and ρ should be treated as constants updated in each iteration. In this modeling, the channel-length modulation coefficient was taken into account only in Eq. (7). Hence, these fitting parameters can be updated from

$$k_p = \frac{g_m^2 \alpha (1 + \rho)^3}{2 I_d (W/L)(1 + \rho/2)^2} \quad (8)$$

$$k_v = v_{ov} / \left[\frac{2\alpha I_d (1 + \rho)}{k_p (W/L)} \right]^{1/2} \quad (9)$$

$$\lambda_d = g_{ds} / I_d \quad (10)$$

where g_m, v_{ov}, and g_{ds} are the transconductance, overdrive voltage, and drain conductance simulated at the design point, respectively. The overdrive voltage v_{ov} can be simply modeled as $(v_{dsat} + 2V_T)$ where v_{dsat} is the drain saturation voltage and $2V_T$ is added to account for some margin and $v_{ov} \simeq 3V_T$ in weak inversion. Fig. 3 shows these voltages overlaid with drain current versus drain voltage curves. The extrapolated threshold voltage $V_t = v_{GS} - V_{ov}$ will be used in the constraints on common-mode range and output swing.
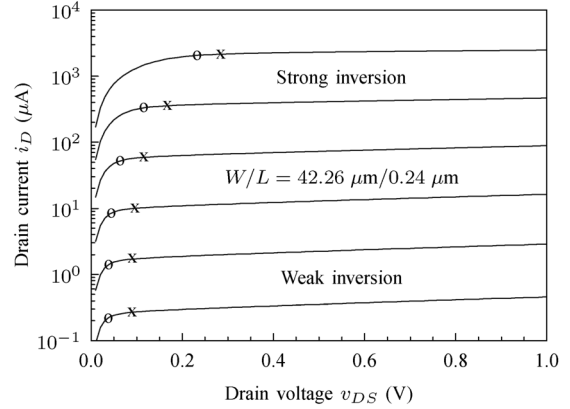

Fig. 3. Drain currents of an nMOSFET from weak through strong inversion for a 0.18 μm process. Mark 'o' and 'x' indicate v_{dsat} and v_{ov} respectively.

These parameters can be obtained through the operating point analysis by Spice, and I_d will be determined from the current mirrors. The transistor parameters I_d, V_{ov}, G_m, and G_d will be used as core monomials in the objective and constraint functions.

Typically, the intrinsic capacitances of an MOSFET depend on not only bias point but also its gate area and oxide capacitance [17]. Thus total gate-source and gate-body capacitances including overlap capacitances can be simply modeled as

$$C_{gs} = k_g (C_{ox}L + C_{gso})W \quad (11)$$

$$C_{gb} = k_b (C_{ox}W + C_{gbo})L \quad (12)$$

where k_g and k_b are fitting parameters. Similarly, the capacitances C_{gd} and C_{dg} can be expressed like C_{gs}.

The expressions for the junction capacitances of source and drain are not posynomial because of having posynomial denominator [2]. Besides, they depend on junction structure as well as bias point. For simplicity, these capacitances including intrinsic capacitances can be simply expressed as

$$C_{bs} = k_s (C_{ox}L + C_j L_j + C_{jswg} + C_{jsw})W \quad (13)$$

where k_s is a fitting parameter and L_j is the diffusion length for source and drain areas. C_j, C_{jswg}, and C_{jsw} are zero-bias junction capacitances of the bottom wall,

gate sidewall, and field sidewall, respectively. Similarly, C_{bd} can be expressed like C_{bs}. The fitting parameters can be updated using capacitances reported by Spice.

4. Subthreshold Region Modeling

The drain current of an MOS transistor in the sub-threshold or weak inversion region can be expressed as

$$i_D = I_{D0} \frac{W}{L} e^{v_{GS}/nV_T}(1 - e^{-v_{DS}/V_T}) \qquad (14)$$

where I_{D0} is a specific current dependent on v_{BS} and n is a slope factor [18]. For an n-channel transistor operating in the subthreshold region, both $i_D - v_{GS}$ and $i_D - v_{DS}$ characteristics are shown in Fig. 4. In the subthreshold region, the transistor is saturated for v_{DS} larger than a few V_T. At the bias point labeled Q, the exponential characteristic of the $i_D - v_{GS}$ curve can be fitted by the square-law model as follows.

$$i_D \simeq I_{D0} \frac{W}{L} e^{v_{GS}/nV_T} = \frac{k_p}{2\alpha} \frac{W}{L}(v_{GS} - V_t)^2 \qquad (15)$$

This square-law relationship is also drawn in Fig. 4. It can be ascertained that this fitting is fine near the bias point Q.

Using Eqs. (6, 15) with $\rho = 0$, the equivalent overdrive voltage in the subthreshold region can be found as

$$V_{ov} = k_v \sqrt{2\alpha I_d/(k_p W/L)} = k_v 2nV_T \qquad (16)$$

which is about $3V_T$ and independent of v_{GS}. This voltage is marked in Fig. 4. The boundary between linear and saturation region can be characterized by the same expression $v_{DS} = V_{ov}$ as in the strong inversion region. In addition, the drain conductance can be modeled with the same fitting parameter λ_d as used for strong inversion. To complete the model fitting, V_t in the subthreshold region can be expressed as $v_{GS} - V_{ov}$. This threshold voltage is also indicated in Fig. 4. Therefore, the transistors in the subthreshold region can be treated with the same approach as in the strong inversion region.
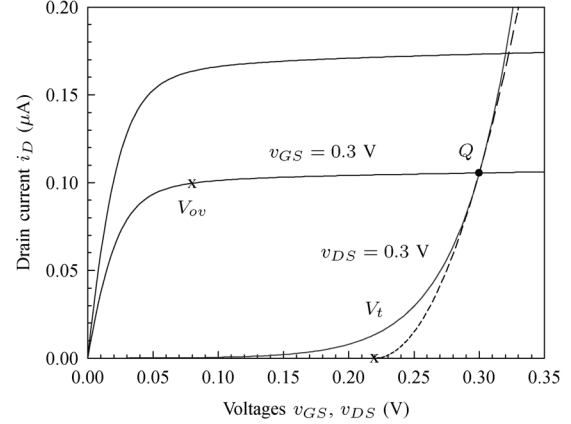

Fig. 4. Drain currents in the subthreshold region for a 0.18 μm process. Solid curves: Spice simulation results; dashed curve: square-law model fitting.

5. Short-Channel Noise Model

To account for both weak inversion and velocity saturation, a new simple expression for the drain current spectral density of thermal noise in the saturation region is suggested as

$$S_{it} = 4kTg_m\gamma = 4kTg_m\alpha \, \gamma_i\gamma_s \qquad (17)$$

where the thermal noise factor is associated with the product of an inversion-level factor γ_i and a short-channel factor γ_s. The inversion-level factor is used to predict thermal noise from strong through weak inversion. This factor can be obtained as

$$\gamma_i = \frac{2}{3} \frac{(\sqrt{4c_i + 1} + 0.5)}{(\sqrt{4c_i + 1} + 1)} = \begin{cases} 1/2 \ (\text{weak}) \\ 2/3 \ (\text{strong}) \end{cases} \qquad (18)$$

where c_i is the inversion coefficient [19]. It can be related to the interpolated overdrive voltage V_{ov} as follows [20].

$$c_i = [\ln(1 + e^{v_{ov}/2nV_T})]^2 \equiv \left[\frac{V_{ov}}{2nV_T}\right]^2 \qquad (19)$$

The thermal noise current spectral density in strong-inversion saturation region [21] can be expressed as

$$S_{it} = 4kT \frac{2}{3}\mu C_{ox} \frac{W}{L} v_{ov} \frac{1 + 3\rho + 3\rho^2}{(1 + \rho)(1 + 2\rho)} \qquad (20)$$

where $u \equiv \alpha v_{Dsat}/v_{OV} = 1/(1+\rho)$ has been used. Using Eq. (4) and $\gamma_i = 2/3$ for strong inversion, the short-channel factor can be obtained as

$$\gamma_s = \frac{S_{it}}{4kTg_m\alpha\gamma_i} = \frac{(1+\rho)(1+3\rho+3\rho^2)}{(1+\rho/2)(1+2\rho)} \quad (21)$$

In weak inversion where $c_i \ll 1$, velocity saturation can be neglected, namely $\rho \ll 1$ since drift current is negligible [19]. Thus the velocity saturation factor can be interpolated as

$$\rho \equiv \frac{v_{OV}}{\alpha V_C} \simeq \frac{V_{OV}}{\alpha V_C} \quad (22)$$

from strong through weak inversion. The electrical channel length $L = L_{\text{eff}} - \Delta L$ is used in $V_C = LE_C$. For long-channel transistors, $\rho \ll 1$ due to high V_C. Finally, the induced gate noise can be ignored for operating frequency much lower than transition frequency $f_T \simeq 5$ GHz of a 0.18 μm process.

The simple unified flicker noise model for MOSFETs in weak, moderate, and strong inversions is given by

$$S_{vf} = \frac{S_{if}}{g_m^2} = \frac{K_{F0}(1 + V_{OV}/V_{KF})^2}{C_{ox}WLf^{AF}} \quad (23)$$

where S_{vf} is gate flicker-noise voltage spectral density [20]. Also K_{F0} is 3.78×10^{-25} V^{2}F and 2.83×10^{-25} V^{2}F, V_{KF} is 1.0 V and 0.25 V, and AF is 0.85 and 1.05 for nMOS and pMOS devices of a 0.18 μm CMOS process, respectively.

6. Iteration Scheme and Design Cost

Since an approximate GP is obtained for a bias point, it is valid only for design points close to the bias point. So the update of core parameters for each transistor is limited as

$$\begin{pmatrix} k_p^{i+1} \\ k_v^{i+1} \\ \lambda_d^{i+1} \end{pmatrix} = \begin{pmatrix} k_p^i \\ k_v^i \\ \lambda_d^i \end{pmatrix} + \delta \begin{pmatrix} k_p^{i+1} - k_p^i \\ k_v^{i+1} - k_v^i \\ \lambda_d^{i+1} - \lambda_d^i \end{pmatrix} \quad (24)$$

where a step length δ can be selected as $0 < \delta \leq 1$. In order to improve convergence toward a feasible solution,

the fitting parameters k_5, k_7, and k_o associated with bias point can be updated after a few iterations. Also the constraints causing infeasibility can be imposed after some iterations. SGP will be stopped if the relative error of objective values between two successive steps is smaller than a tolerance of 0.1% and the number of iterations exceeds a predefined value of 50. If numerical divergence occurs in the op analysis of op amps, SGP can not continue the iterative design process. To enhance the robustness of SGP, techniques for avoiding the divergence can be needed like in circuit simulation. But owing to good mathematical continuity of BSIM3v3.2, this divergence does not occurs in the many design processes of the CMOS op amps. Finally, each iteration of SGP involves a GP solving and an operating point analysis of an op amp. On a 1.8 GHz GNU/Linux computer, it takes 27 iterations or four minutes to design a two-stage op amp with eight transistors.

7. Modeling Accuracy and Global Design

Table 1 shows some biasing and modeling errors in the two-stage op amp designed for the 0.18 μm process (MOSIS T77A: MM NON-EPI). The maximum relative error is less than 0.25% when the number of iterations is 50 and all transistors are operating in the strong inversion region. This is greatly improved result than a few percent of published results shown in Table 2. Here a data point means an op analysis for an nMOS transistor. Table 3 shows a comparision of some performance errors with published approaches. It can be seen that the design paradigm has good performance prediction. This op amp has a low input offset voltage of 0.35 μV. Hence these results indicate that small-signal parameters as well as bias parameters well match Spice simulation results.

For the given specifications, Table 4 shows maximum relative deviations of the power dissipation and design

Table 1. Biasing and modeling errors in transistor parameters

Parameter	Spice	Error	Parameter	Spice	Error
I_{d5}	16.09 μA	0.08 %	I_{d6}	96.6 μA	0.09 %
g_{m1}	158.0 μS	0.08 %	g_{ds1}	1.96 μS	0.09 %
g_{m3}	120.7 μS	0.22 %	g_{ds3}	1.08 μS	0.08 %
g_{m6}	1.758 mS	0.04 %	g_{ds6}	32.1 μS	0.11 %
g_{m7}	1.080 mS	0.22 %	g_{ds7}	13.5 μS	0.08 %
C_{gs3}	23.15 fF	0.19 %	C_{gs6}	47.90 fF	0.13 %
C_{bd3}	5.016 fF	0.24 %	C_{bd6}	15.80 fF	0.13 %

Table 2. Comparision of modeling error and simulation cost with previously published approaches for 0.18 μm process

Approach	Modeling error ϵ	Simulation cost
[6]	$0.79\% < \epsilon < 9.8\%$	2000 data points
[7]	$2.3\% < \epsilon < 17.6\%$	1800 data points
[8]	$0.47\% < \epsilon < 9.36\%$	unavailable
[9]	$0.05\% < \epsilon < 3.01\%$	70000 data points
[10]	$3.4\% < \epsilon < 25.3\%$	unavailable
This work	$0.04\% < \epsilon < 0.24\%$	< 70 op analyses

Table 3. Comparision of some performance errors with previously published approaches for two-stage CMOS op amps

Approach	Performance	A_0 (dB)	f_t (MHz)	PM (°)
[6]	Predition	73.8	74.0	60.0
	Error	5.0 %	10.6 %	9.7 %
[8]	Predition	76.7	10.0	70.0
	Error	4.1 %	10.1 %	7.7 %
[10]	Predition	60.0	50.0	86.4
	Error [1]	0.6 %	1.8 %	9.4 %
[11]	Predition [2]	70.0	65.7	90.0
	Error	0.0 %	6.7 %	2.3 %
This work	Predition	66.0	100.0	40.0
	Error	0.0 %	0.8 %	5.4 %
	Error [1]	0.0 %	0.1 %	1.6 %

[1] errors for a basic or fully differential folded-cascode op amp
[2] performances adjusted iteratively through Spice ac analysis

Table 4. Maximum relative deviations of power dissipation and design variables for final designs obtained by starting from eight initial values of (k_p, k_v, λ_d). These have corner values from (50, 0.6, 0.03) to (100, 1, 0.05) in units of (μA/V², V/V, V⁻¹)

Design variable	Average value	Maximum deviation
P_D	0.246 mW	0.080 %
I_B	24.15 μA	0.207 %
C_c	0.181 pF	0.091 %
W_1, W_2	13.43 μm	0.083 %
W_3, W_4	3.878 μm	0.227 %
W_5	3.968 μm	0.165 %
W_6	24.52 μm	0.112 %
W_7	22.44 μm	0.328 %
W_8	5.781 μm	0.447 %
L_1, L_2	0.200 μm	0.000 %
L_3, L_4	0.802 μm	0.061 %
L_5, L_7, L_8	0.200 μm	0.000 %
L_8	0.200 μm	0.000 %

variables for final designs obtained by starting from eight initial values of (k_p, k_v, λ_d). Dependency of design results on these initial values is less than 0.5%. This result indicates that the designed op amp may be close to the global optimum. Naturally, this does not always guarantee the globally optimal design that is the ultimate goal of every op amp designer [22].

IV. DESIGN EXAMPLES

In order to express a op-amp design problem as an approximate geometric program, some fitting parameters will be also used in performances and constraints. Using these parameters, modeling techniques for accuracy improvement will be illustrated for two op amps. Also design results for these op amps will be presented.

1. Two-Stage CMOS Op Amp

A basic two-stage CMOS op amp is shown in Fig. 5. This has 18 design variables which are width W_i and length L_i of each transistor, bias current I_B, and compensation capacitance C_c. For this op amp, most of performances and constraints can be expressed like the posynomial functions described in [2]. Here those will not be repeated. But adaptive bias constraints for accuracy, accurate small-signal transfer function with a new zero z_3, phase lead compensation, and subthreshold op amp design will be described in this section.
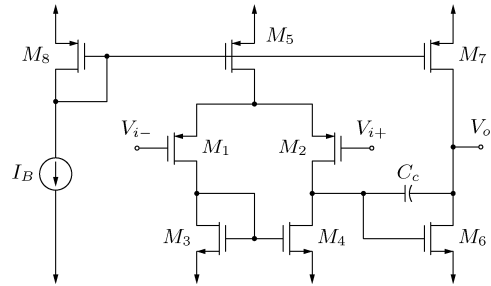

Fig. 5. A basic two-stage CMOS operational amplifier.

A. Adaptive Bias Constraints

Transistors M_5 and M_7 form current mirrors with M_8. The current ratios of these mirrors are not accurately determined by only aspect ratios of transistors. These current ratios depend on channel-length modulation coefficients and threshold voltages of transistors in the mirrors. To obtain accurate bias parameters I_{d5} and I_{d7} including those effects, they can be expressed from the current mirrors as

$$\frac{I_{d5}}{I_B} = k_5 \frac{W_5/L_5}{W_8/L_8} \; , \; \frac{I_{d7}}{I_B} = k_7 \frac{W_7/L_7}{W_8/L_8} \qquad (25)$$

where fitting parameters k_5 and k_7 are updated from drain currents i_{D5} and i_{D7} simulated at a design point. For example, $k_5 = (i_{D5}/I_B)(W_8/L_8)/(W_5/L_5)$.

In order to minimize the systematic offset voltage, the drain current of M_6 must be exactly equal to the current supplied by M_7. It follows that the constraints $v_{GS6} = v_{DS4} = v_{GS3}$ due to circuit structure and symmetry should be satisfied. From $I_{d3} = I_{d5}/2$ and $I_{d6} = I_{d7}$, a constraint can be found as

$$\frac{k_5}{2k_7} \frac{(W_5/L_5)(W_6/L_6)}{(W_3/L_3)(W_7/L_7)} = k_o \qquad (26)$$

where k_o is a fitting parameter whose initial value is 1. When $v_{GS6} > v_{GS3}$ at a bias point, v_{GS6} will have to be decreased. If k_o is increased, (W_6/L_6) will increase. Then v_{GS6} will be reduced for the given bias current of M_6. As a result, $(v_{GS6} - v_{GS3})$ will decrease and eventually v_{GS6} will be equal to v_{GS3}. Thus k_o can be updated with a gain of 10 as

$$k_o = k_o + 10(v_{GS6} - v_{GS3}) \qquad (27)$$

B. Accurate Small-Signal Transfer Function

Adding a new zero z_3, the small-signal transfer function of the op amp with balanced driving can be approximated as

$$A(s) = \frac{A_0(1 + s/\omega_{z1})(1 + s/\omega_{z2})(1 + s/\omega_{z3})}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})(1 + s/\omega_{p3})} \qquad (28)$$

where A_0 is the dc gain, ω_{zi} is the frequency of zero

Table 5. Dc gain, zero frequencies, pole frequencies, and node capacitances derived for the two-stage CMOS op amp

$$A_0 = \frac{g_{m1}g_{m6}}{g_{o1}g_{o2}}, \quad \omega_{z1} = \frac{2g_{m3} + g_{o1}}{C_3 - C_{dg3}}, \quad \omega_{z2} = -\frac{g_{m6}}{C_c + C_{dg6}}$$

$$\omega_{z3} = -\frac{g_{m1}}{C_{dg1}}, \quad \omega_{p1} \simeq \frac{g_{o1}g_{o2}}{C_2 g_{o1} + (C_c + C_{gd6})g_{m6} + C_1 g_{o2}}$$

$$\omega_{p2} \simeq \frac{C_2 g_{o1} + (C_c + C_{gd6})g_{m6} + C_1 g_{o2}}{C_2 C_1 - (C_c + C_{gd6})(C_c + C_{dg6})}, \quad \omega_{p3} = \frac{g_{m3} + g_{o1}}{C_3}$$

$$g_{o1} \equiv g_{ds1} + g_{ds3}, \quad g_{o2} \equiv g_{ds6} + g_{ds7}$$

$$C_1 = C_c + C_{gs6} + C_{bd1} + C_{bd3} + C_{gb6} + C_{gd1} + C_{gd3} + C_{gd6}$$

$$C_2 = C_c + C_L + C_{bd6} + C_{bd7} + C_{gd6} + C_{gd7}$$

$$C_3 = 2C_{gs3} + 2C_{gb3} + C_{bd1} + C_{bd3} + C_{gd1} + C_{gd3} - C_{m3}$$
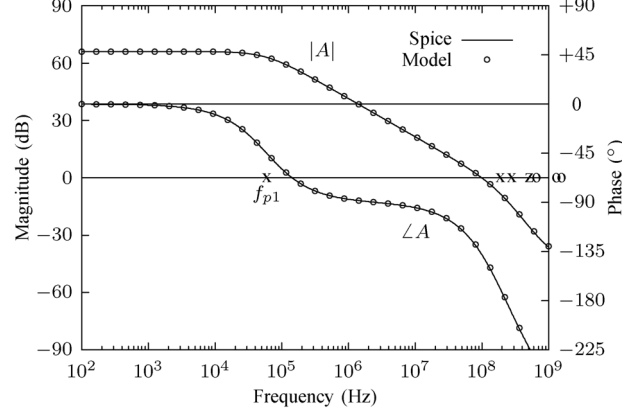

Fig. 6. Comparision of the transfer function model to Spice simulation for a designed op amp. Mark 'x' indicates a pole frequency, mark 'o' a zero frequency, and mark 'z' a pole-zero doublet due to the bias current mirror.

z_i, and ω_{pi} is the frequency of pole p_i. These can be derived as shown in Table 5. For the two-stage op amp designed for the 0.18 μm process, a comparision between this transfer function and Spice simulation is shown in Fig. 6. It can be seen that Eq. (28) is an accurate model of the transfer function.

From Table 5, the frequencies of the dominant pole and output pole can be expressed as

$$\omega_{p1} \simeq \frac{G_{o1}G_{o2}}{k_1 g_{m6} C_c}, \quad \omega_{p2} \simeq \frac{G_{m6} C_c}{k_2 C_1 C_2} \qquad (29)$$

$$k_1 \equiv \left[1 + \frac{C_{gd6}}{C_c}\right]\left[1 + \frac{g_{o1}C_2 + g_{o2}C_1}{g_{m6}(C_c + C_{gd6})}\right] \qquad (30)$$

$$k_2 \equiv \frac{1}{k_1}\left[1 - \frac{(C_c + C_{gd6})(C_c + C_{dge6})}{C_1 C_2}\right] \qquad (31)$$

where C_1 is the total capacitance at the drain node of M_2 and C_2 is that at the output node. These poles can be determined from the small-signal parameters simulated at a design point. The total capacitance C_3 at the drain node of M_3 can be approximated as a posynomial by neglecting the negative term of C_{m3}. Also the zero and pole frequencies of the load mirror can be approximated as $\omega_{p3} \simeq g_{m3}/C_3 \simeq \omega_{z1}/2$.

The unity-gain frequency of the two-stage op amp is an implicit nonposynomial. Using $|A(j\omega_t)| \equiv 1$ and $\omega_t/\omega_{p1} \gg 1$, the unity-gain frequency ω_t can be modeled as

$$\omega_t = A_0 \omega_{p1} H(\omega_t) = k_t \frac{G_{m1}}{C_c} \qquad (32)$$

$$H(\omega_t) \equiv \sqrt{\frac{\prod_{i=1}^{3}[1+(\omega_t/\omega_{zi})^2]}{\prod_{i=2}^{3}\left[1+\left(\omega_t/\omega_{pi}\right)^2\right]}} \qquad (33)$$

where $k_t = H(\omega_t)/k_1$ is an updating parameter. The phase margin of the op amp is also a complicate nonposynomial. Using $\tan^{-1}(x) \simeq x$ for $x < 0.5$ and $1/\omega_{p3} - 1/\omega_{z1} \simeq 0.5/\omega_{p3}$, the phase margin PM can be obtained from

$$\frac{90° - \text{PM}}{180°} \simeq \frac{\omega_t}{\pi}\left[\frac{k_2 C_1 C_2}{G_{m6} C_c} + \frac{k_3 C_c}{G_{m6}} + \frac{0.5 C_3}{G_{m3}} + \frac{C_{dg1}}{G_{m1}}\right] \quad (34)$$

where a parameter $k_3 \equiv (1 + C_{dg6}/C_c)$. The positive power supply rejection ratio of the op amp is inverse signomial. Thus the constraint on PSRR⁺ was not handled in [2]. But it will be simply handled by using an updating parameter k_r as

$$\text{PSRR}^+ = \frac{G_{m2} G_{m6}}{k_r(G_{d1} + G_{d3})G_{d7}} \qquad (35)$$

where k_r is given by $|1 - g_{m6}g_{ds5}/2g_{m3}g_{ds7}|$ at a design point.

In practice, there is a pole-zero doublet due to the bias mirror. The frequency of this doublet can be obtained as

$$\omega_{z4} \simeq \frac{g_{m8}}{C_4} > \omega_{p4} \qquad (36)$$

where C_4 is the total capacitance at the gate of M_8. If this doublet is in the passband, it may cause severe degradation of settling time while only causing minor changes in the frequency response [23]. Besides, the doublet near ω_t may give rise to errors in estimating ω_t and PM. To enhance stability and accuracy, it is desirable to impose a constraint $\omega_{z4} > 5\omega_t$.

C. Phase Lead Compensation

The phase margin can be improved by including a resistance R_c in series with C_c. Due to inserting R_c, the pole p_2 and RHP zero z_2 move while a new pole p_5
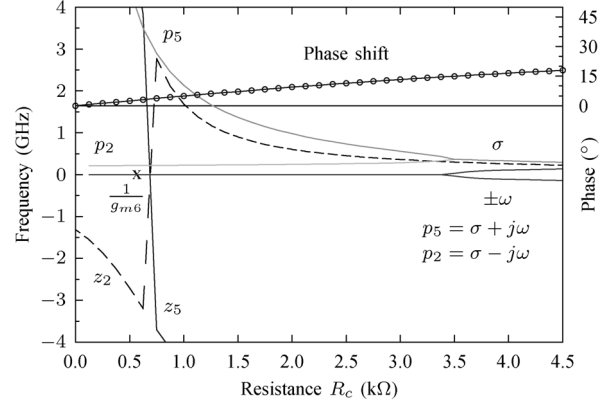

Fig. 7. Pole-zero movements and the phase shift as R_c is increased.

and a new zero z_5 are introduced into the transfer function. The movement of these poles and zeros for increasing R_c is shown in Fig. 7. Making R_c greater than $1/g_{m6}$ moves the RHP zero z_2 into the left half plane and moves the zero z_5 to a very high frequency. In addition, the poles p_2 and p_5 will eventually become two complex poles. As R_c is increased, the phase shift associated with these poles and zeros increases monotonically as shown in Fig. 7. Then the phase margin will increase too and actually the unity-gain frequency will somewhat increase. As a result, the op amp can be simply compensated by increasing R_c only. This is somewhat different from the simple model.

The sensitivity information from GP shows that the phase margin is a critical performance in reducing quiescent power. For low power design, after designing

Table 6. Specifications, predicted performances, and simulated performances for a designed two-stage CMOS op amp

Performance	Specification	Prediction	Simulation
A_0 (dB)	≥ 60	66.0	66.0
f_t (MHz)	≥ 100	100	99.2 (109) *
PM (°)	≥ 40	40.0	42.3 (60) *
CMR (V)	$-0.70/0.13$	$-0.71/0.15$	$-0.72/0.15$
OS (V)	$-0.70/0.60$	$-0.74/0.60$	$-0.79/0.77$
SR (V/μs)	≥ 80	80.0	53.0
CMRR (dB)	≥ 60	72.2	72.4
PSRR+ (dB)	≥ 60	80.2	80.6
PSRR− (dB)	≥ 60	69.1	69.0
S_n (nV/$\sqrt{\text{Hz}}$)	≤ 300	300	unavailable
Area (μm²)	≤ 50	50	50
P_D (mW)	minimize	0.247	0.246
0.18 μm CMOS process, power supply = ±0.9 V, C_L = 1 pF			

* after phase lead compensation with $R_c = 3.97$ kΩ

an op amp with zero R_c and less phase margin of 40°, its phase margin can be improved by increasing R_c. After lead compensation with $R_c = 3.97$ kΩ, the phase margin improves to 60° as given in Table 6. This table shows the specifications, predicted performances, and simulated performances for the two-stage CMOS op amp designed using the 0.18 μm BSIM3 parameters. In this design, a spot noise constraint is imposed on the input-referred noise spectral density at 1 kHz and the active area of the op amp is $(a_c C_c + \sum_{i=1}^{8} W_i L_i)$ where a_c is the ratio of capacitor area to capacitance between polysilicon and n$^+$ diffusion region. Except for the slew rate, the predicted performances are very close to the simulated values.

D. Subthreshold Region Design

MOS transistors operating in the subthreshold region can be used to design low-power low-voltage op amps [24]. In order to allow a transistor to operate in the subthreshold region, a constraint for strong inversion operation $v_{OV} \geq v_{OV\min}$ should not be imposed on the transistor. Table 7 shows the results of subthreshold region design for the two-stage CMOS op amp with a load capacitance C_L of 0.1 pF. Here all the transistors operate in the subthreshold region with their overdrive voltage $v_{OV} < -100$ mV. This op amp has low performances of 1.1 MHz unity-gain frequency and 0.3 V/μs slew rate, but operates with very low power

Table 7. Specifications, predicted performances, and simulated performances for a subthreshold two-stage CMOS op amp

Performance	Specification	Prediction	Simulation
A_0 (dB)	≥ 60	66.0	65.9
f_t (MHz)	≥ 1	1.16	1.13 (1.16) *
PM (°)	≥ 40	40.0	39.7 (60) *
CMR (V)	$-0.7/0.3$	$-0.76/0.50$	$-0.76/0.50$
OS (V)	$-0.7/0.7$	$-0.81/0.80$	$-0.81/0.81$
SR (V/μs)	≥ 0.7	0.70	0.30
CMRR (dB)	≥ 60	73.5	73.7
PSRR+ (dB)	≥ 60	93.6	95.8
PSRR− (dB)	≥ 60	70.2	70.1
S_n (nV/√Hz)	≤ 300	300	unavailable
Area (μm²)	≤ 50	47.6	47.6
P_D (μW)	minimize	0.473	0.475

* after phase lead compensation with R_c = 542 kΩ

dissipation of 0.475 μW.

2. Fully Differential Folded-Cascode CMOS Op Amp

A fully differential folded-cascode CMOS op amp [25] is shown in Fig. 8. Here the common-mode feedback circuit with zero v_{CM} has been modeled as a bias voltage and dependent sources. Besides, a transistor M_{12} has been added for biasing.
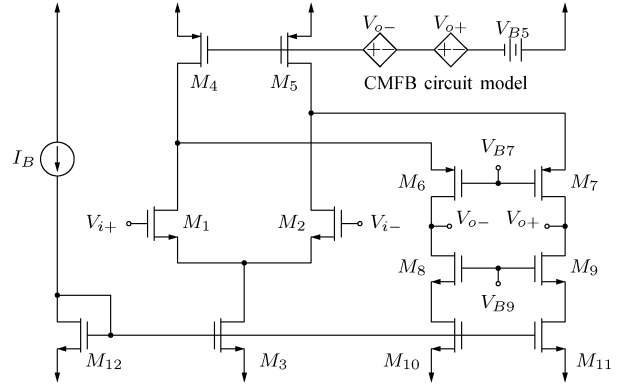

Fig. 8. A fully differential folded-cascode CMOS operational amplifier.

A. Adaptive Bias Constraints

Transistors M_3, M_{10}, and M_{11} form current mirrors with M_{12}. To obtain accurate bias currents I_{d3} and $I_{d10} = I_{d11}$, they can be expressed as

$$\frac{I_{d3}}{I_B} = k_3 \frac{(W_3/L_3)}{(W_{12}/L_{12})}, \ \frac{I_{d10}}{I_B} = k_{10} \frac{(W_{10}/L_{10})}{(W_{12}/L_{12})} \qquad (37)$$

where fitting parameters k_3 and k_{10} are updated from drain currents i_{D3} and i_{D10} simulated at a design point.

B. Transfer Function Constraints

Small-signal analysis results are summarized in Table 8. Here g_{m7} and g_{m9} include each body transconductance, C_1, C_2, and C_3 are the total capacitances at the drain of M_2, M_9, and M_{11}, respectively. There is a pole-zero doublet at $\omega_{z1} \simeq \omega_{p3}$. Various design constraints for the transfer function of this folded-cascode op amp can be modeled like those of the two-stage op amp.

Table 8. Dc gain, zero frequencies, pole frequencies, and node capacitances derived for the folded-cascode CMOS op amp

$$A_0 \simeq \frac{g_{m1}}{g_o}, \quad g_o \equiv \frac{g_{ds9}g_{ds11}}{g_{m9}} + \frac{(g_{ds1}+g_{ds5})g_{ds7}}{g_{m7}}$$

$$\omega_{z1} = \frac{g_{m9}+g_{o3}}{C_3 - C_{m9}}, \quad \omega_{z2} = -\frac{g_{m7}+g_{ds7}}{C_{m6}}, \quad \omega_{z3} = -\frac{g_{m1}}{C_{dg1}}$$

$$\omega_{p1} \simeq \frac{g_o}{C_2}, \quad \omega_{p2} \simeq \frac{g_{m7}+g_{o1}}{C_1 - C_{m7}}, \quad \omega_{p3} \simeq \frac{g_{m9}+g_{o3}}{C_3 - C_{m9}}$$

$$g_{o1} \equiv g_{ds1} + g_{ds5} + g_{ds7}, \quad g_{o3} \equiv g_{ds9} + g_{ds11}$$

$$C_1 = C_{gs7} + C_{bs7} + C_{bd1} + C_{gd1} + C_{bd5} + C_{gd5}$$

$$C_2 = C_L + C_{bd7} + C_{gd7} + C_{bd9} + C_{gd9}$$

$$C_3 = C_{gs9} + C_{bs9} + C_{gd11} + C_{bd11}$$

C. Other Constraints

The bias constraint that all transistors remain in saturation for the common-mode voltage v_{CM} and output voltage v_O is given by the following inequalities.

$$V_{SS} + V_{ov3} + V_{ov1} + V_{t1} \leq v_{CM} \leq V_{DD} - |V_{ov5}| + V_{t1} \quad (38)$$

$$V_{SS} + V_{ov9} + V_{ov11} \leq v_O \leq V_{DD} - |V_{ov5}| - |V_{ov7}| \quad (39)$$

The three bias voltages for maximum swing are given by

$$V_{B5} = V_{DD} - |V_{ov5}| - |V_{t5}| \quad (40)$$

$$V_{B7} = V_{DD} - |V_{ov5}| - |V_{ov7}| - |V_{t7}| \quad (41)$$

$$V_{B9} = V_{SS} + |V_{ov9}| + |V_{ov11}| + |V_{t9}| \quad (42)$$

The slew rate is expressed as $SR = I_{d1}/C_L$, the active area of the op amp is $\sum_{i=1}^{12} W_i L_i$, and the power dissipation is given by $(V_{DD} + V_{SS})(I_{d4} + I_{d5} + I_B)$.

Table 9. Specifications, predicted performances, and simulated performances for a folded-cascode CMOS op amp

Performance	Specification	Prediction	Simulation
A_0 (dB)	≥ 60	60.0	60.0
f_t (MHz)	≥ 500	500.0	500.6
PM (°)	≥ 60	61.1	62.1
CMR (V)	0.2/0.8	−0.02/1.21	−0.36/1.33
OS (V)	−0.5/0.5	−0.52/0.50	−0.53/0.53
SR (V/μs)	≥ 200	200	111
Area (μm^2)	≤ 50	50.0	50.0
P_D (mW)	minimize	0.739	0.732
0.18 μm CMOS process, power supply = ±0.9 V, C_L = 0.5 pF			

Table 10. Specifications, predicted performances, and simulated performances of the folded-cascode CMOS op amp for an IBM 0.13 μm process

Performance	Specification	Prediction	Simulation
A_0 (dB)	≥ 48	48.1	48.1
f_t (MHz)	≥ 500	571.9	569.2
PM (°)	≥ 60	66.0	67.1
CMR (V)	0.1/0.7	0.01/0.79	0.00/0.80
OS (V)	−0.3/0.3	−0.36/0.31	−0.32/0.30
SR (V/μs)	≥ 200	200	160
Area (μm^2)	≤ 35	34.9	34.9
P_D (mW)	minimize	0.348	0.347
0.13 μm CMOS process, power supply = ±0.6 V, C_L = 0.35 pF			

Table 9 shows design results of the fully differential folded-cascode CMOS op amp. Like the two-stage op amp, the predicted performances are very close to the simulated values except for the slew rate. Table 10 shows design results of the fully differential folded-cascode CMOS op amp for an IBM 0.13 μm process. This op amp with C_L of 0.35 pF uses less area and less quiescent power, but has somewhat low dc gain of 48 dB.

V. CONCLUSIONS

A design paradigm using sequential geometric programming has been presented to accurately design CMOS op amps with BSIM3. This is based on new adaptive monomial modeling of transistor parameters instead of piecewise or global prefitting. As a result, it has low modeling cost as well as great simplicity and high accuracy. The short-channel dc, high-frequency small-signal, and short-channel noise models have been used to characterize the physical behavior of submicron devices. In addition, this paradigm has been extended to design low-power op amps operating in the subthreshold region.

The design paradigm has been illustrated by optimizing two CMOS op amps with the transfer function accurately derived for the high-frequency model. Since the biasing and modeling errors are less than 0.25%, the characteristics of the op amps well match simulation results. In addition, small dependency of design results on initial values indicates that a designed amplifier may be close to the global optimum. Therefore, this paradigm can be a useful approach to accurately design or tune high-performance op amps with higher-order device models.

APPENDIX

The simple methods to accept Spice model and transistor parameters can be described as the following procedures. Of course these should be modified according to file format. Get Model Parameter ( ) accepts the model parameters by parsing the input file 'opa.cir'. Get Transistor Parameter ( ) accepts transistor parameters by parsing the output file 'opa.out'.

```
Get Model Parameter ( ) {
    open 'opa.cir';
    // model parameters for nMOST
    while ( not end of file ) {
        get a line and scan it;
        if ( '.model cmosp pmos' found ) break;
        find 'xj'; scan its value;
        find 'tox'; scan its value;
        find 'lint'; scan its value;
        find 'cj'; scan its value;
        find 'cjsw'; scan its value;
    }
    // model parameters for p MOST
    while ( not end of file ) {
        get a line and scan it;
        if ( '.end' found ) break;
        find 'lint'; scan its value;
        find 'cj'; scan its value;
        find 'cjsw'; scan its value;
    }
    close 'opa.cir';
}

Get Transistor Parameter ( ) {
    open 'opa.out';
    while ( not end of file ) {
        get a line and scan it;
        if ( '**** mosfets' found ) break;
    }
    new = 1;
    while ( not end of file ) {
        get a line and scan it;
        if ( '***** job' found ) break;
        if ( 'model' found ) {
            get a line; n = count 'cmos';
            skip a line; // 'region'
```

```
            get a line; scan drain currents x[n];
            if ( new ) id = x;
            else id = catenate (id, x);
            skip a line; // 'ibs'
            skip a line; // 'ibd'
            get a line; scan gate voltages x[n];
            if ( new ) vgs = x;
            else vgs = catenate (vgs, x);
            repeated for other parameters;
        }
        if ( new ) new = 0;
    }
    close 'opa.out';
}
```

ACKNOWLEDGMENTS

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