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Impact of Segregation Layer on Scalability and Analog/RF Performance of Nanoscale Schottky Barrier SOI MOSFET

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***Abstract*—In this paper, the impact of segregation layer density (N_{DSL}) and length (L_{DSL}) on scalability and analog/RF performance of dopant-segregated Schottky barrier (DSSB) SOI MOSFET has been investigated in sub-30 nm regime. It has been found that, although by increasing the N_{DSL} the increased off-state leakage, short-channel effects and the parasitic capacitances limits the scalability, the reduced Schottky barrier width at source-to-channel interface improves the analog/RF figures of merit of this device. Moreover, although by reducing the L_{DSL} the increased voltage drop across the underlap length reduces the drive current, the increased effective channel length improves the scalability of this device. Further, the gain-bandwidth product in a common-source amplifier based on optimized DSSB SOI MOSFET has improved by ~40% over an amplifier based on raised source/drain ultrathin-body SOI MOSFET. Thus, optimizing N_{DSL} and L_{DSL} of DSSB SOI MOSFET makes it a suitable candidate for future nanoscale analog/RF circuits**

***Index Terms*—Scalability, analog/RF performance, dopant-segregation, Schottky barrier**

I. INTRODUCTION

Due to better electrostatic integrity and planar structure ultrathin-body (UTB) single-gate silicon-on-insulator (SOI) MOSFET has attracted the attention of researchers [1]. However, since source/drain (S/D) series resistance (R_{SD}) is inversely proportional to junction depth, with reduction in SOI film thickness R_{SD} increases. To alleviate this problem, raised S/D UTB SOI MOSFET (RSD UTB) has been proposed, in which the increased S/D area due to raised S/D reduces the R_{SD} [2]. However, the Miller capacitance between gate and the raised S/D increases the parasitic capacitances of the device [3]. Despite replacing doped S/D by metal silicides can reduce R_{SD}, the desirability of zero Schottky barrier (SB) height at metal-semiconductor (M-S) junction formed between metal S/D and the channel is a major challenge for SB SOI MOSFETs [4-5]. In addition, ambipolar conduction and the increased subthreshold swing (S) limit the use of this device for analog/RF circuits [6].

Recently, dopant-segregated SB (DSSB) SOI MOSFET has been proposed, in which SB lowering and thinning induced by dopant segregation layer (DSL) not only suppresses the ambipolar conduction but also improves the drive current of the device [7]. In spite of having improved drive current due to DSL, the high frequency performance of DSSB SOI MOSFET deteriorates as compared to RSD UTB [6, 8]. In order to improve the high frequency performance of this device lot of work has been carried out by different groups through experiments [9-10] and by simulations [11-12]. However, the impact of segregation layer doping density (N_{DSL}) and the length (L_{DSL}) on scalability and analog/RF performance of this device in sub-30 nm regime has not been investigated.

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In this work, the impact of N_{DSL} and L_{DSL} on scalability and analog/RF performance of nanoscale DSSB SOI MOSFET has been investigated by using the MEDICI simulator. Further, the detailed guidelines for optimizing the performance of this device have also been presented. The organization of rest of the paper is as follows, Section II presents the device structures and the simulation methodology used in this work. Section III compares and discusses about the scalability, analog/RF performance and analog circuit performance of RSD UTB and DSSB SOI MOSFETs. Finally the conclusion is given in Section IV.

II. SIMULATION SETUP

Fig. 1 shows the cross-sectional view of RSD UTB and DSSB SOI MOSFETs used in the simulations. The range of physical gate length (L_G) has been taken as per ITRS-2009 high performance logic technology nodes [13]. The gate oxide thickness, buried oxide thickness, SOI film thickness and the spacers of thickness 1 nm, 50 nm, 8 nm and 10 nm respectively have been considered for both the devices. In case of RSD UTB structure, raised S/D height of 20 nm with uniform doping density of 1×10^{20} cm^{-3} and S/D extension (SDE) region of doping 1×10^{19} cm^{-3} have been considered. The $ErSi_{1.7}$ having electron SB height (Φ_{bn}) of 0.28 eV has been considered as S/D material for DSSB SOI MOSFET. However, since the interface trap states at the M-S junction have not been considered, Φ_{bn} of 0.3 eV has been taken in the simulations. The L_{DSL} has been defined as the distance between M-S junction edge and the p-n junction edge where N_{DSL} drops to 1×10^{15} cm^{-3}. Further, to realize an underlap, overlap and the gate edge channel structures L_{DSL} of 5 nm, 11 nm and 10 nm respectively have been considered by changing the lateral doping straggle in the DSL [14].

The drift-diffusion simulations incorporating image force SB lowering, SB tunneling and the mobility models have been carried out. Further, the analog/RF figures of merit have been extracted from the *Y*-parameter matrix generated by performing the small-signal ac analysis. In order to capture the gate induced drain leakage (GIDL) effect, band-to-band tunneling and the trap-assisted tunneling models from the MEDICI simulator [15] have been enabled. It has been shown that inclusion of quantum effects (QEs) which shifts the peak electron concentration away from the gate oxide interface towards the center of SOI film leads to shift in the threshold voltage of the device. Further, this effect is more significant for $T_{Si} < 5$ nm [16-18]. Since T_{Si} of 8 nm has been considered in this work, the impact of QEs can be ignored. To illustrate this, the impact of QEs on saturation threshold voltage (V_{TSAT}) of DSSB SOI MOSFET has been studied with and without the inclusion of QE models. Although a complete analysis of QEs is not possible with MEDICI simulator, a brief analysis incorporating the modified local density approximation (MLDA) model has been carried out. From Fig. 2 it can be seen that, below $T_{Si} = 8$ nm with turning ON and OFF of MLDA model, there is significant difference in V_{TSAT} value of the device. Further, beyond $T_{Si} = 8$ nm the V_{TSAT} value with turning ON and OFF of MLDA model is almost equal. This clearly shows that, beyond $T_{Si} = 8$ nm the impact of QEs can be ignored.

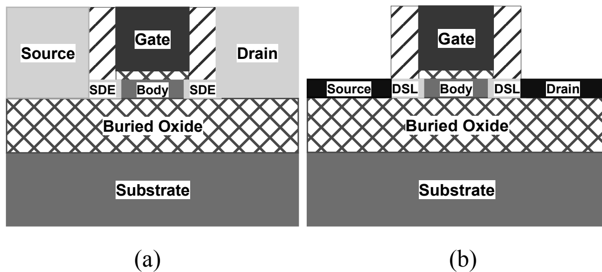


Fig. 1. (a) RSD UTB, (b) DSSB SOI MOSFET structures used in the MEDICI simulator.

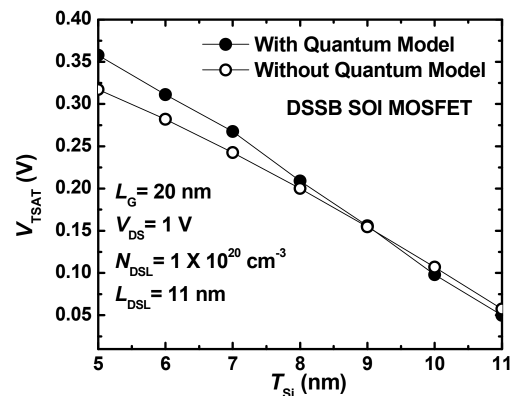


Fig. 2. Impact of quantum confinement effect on saturation threshold voltage of DSSB SOI MOSFET.

III. RESULTS AND DISCUSSION

1. Band diagrams

Fig. 3 shows the simulated band diagrams of DSSB SOI MOSFET at various N_{DSL} values. From the figure it can be seen that, with increasing N_{DSL} the Fermi-level pinning effect and the increased band bending at S/D-to-DSL interface narrows the SB width. Further, in the off-state the wider tunneling barrier for the holes at the drain reduces hole current and hence suppresses the ambipolar conduction of the device [6]. However, the narrow tunneling width for the electrons at the source increases the subthreshold leakage of the device. On the other hand, in the on-state the electrons at the source can easily tunnel through the narrow tunneling barrier and leads to an improvement in the drive current of the device. Since similar kind of behavior has been observed at L_{DSL} = 5 nm and L_{DSL} = 10 nm, the band diagrams at these lengths are not shown here.

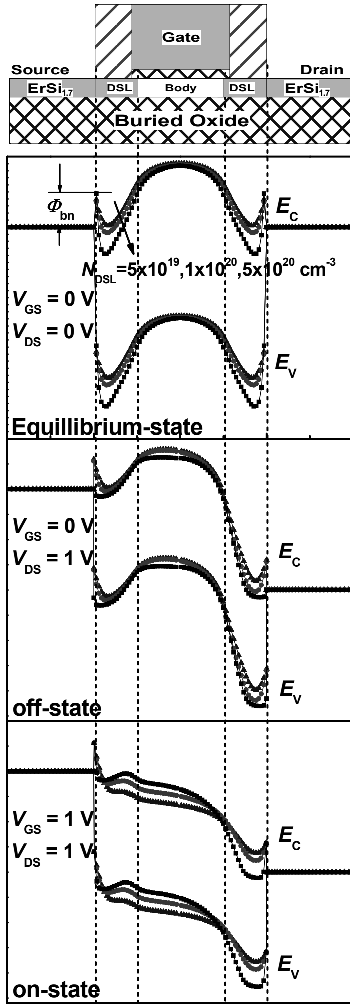


Fig. 3. Simulated band diagrams of DSSB SOI MOSFET for various N_{DSL} values at fixed L_{DSL} of 11 nm.

2. Scalability

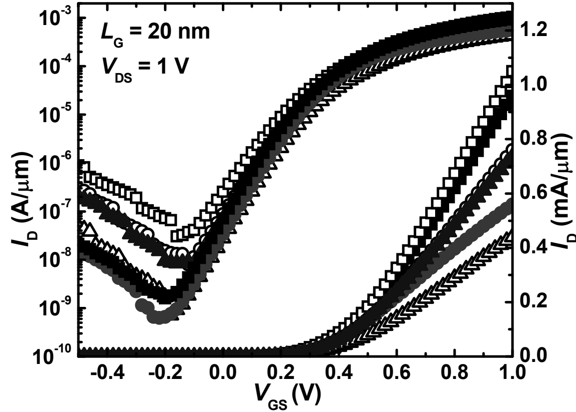
The scalability is mainly characterized by *S*, drain induced barrier lowering (DIBL), on-state drive current (I_{ON}) and the off-state leakage current (I_{OFF}) of a MOSFET [2]. The DIBL is defined as [2]

$$\text{DIBL} = \frac{V_{TLIN} - V_{TSAT}}{0.95}, \quad (1)$$

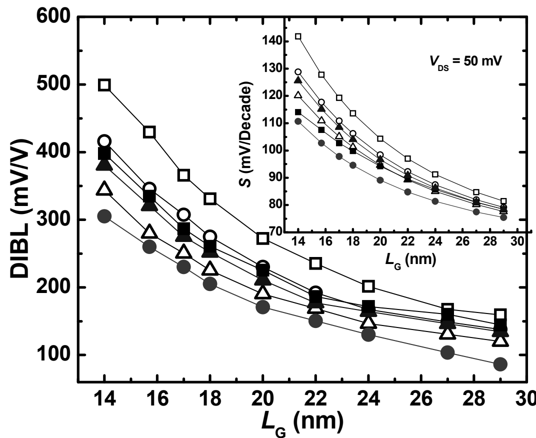
where V_{TLIN} and V_{TSAT} are the threshold voltages at V_{DS} = 50 mV and 1 V respectively and have been extracted by extrapolating the I_D vs V_{GS} and $I_D^{1/2}$ vs V_{GS} characteristics of the devices. For better comparison V_{TSAT} of all the structures has been adjusted to 0.2 V by tuning the gate work-function at V_{DS} = 1 V. Further, *S* has been extracted at V_{DS} = 50 mV whereas I_{OFF} and I_{ON} have been extracted at $V_{DS} = V_{DD}$ = 1 V; $V_{GS} = V_{GOFF}$ = 0 V and $V_{DS} = V_{DD}$; $V_{GS} = V_{GOFF} + V_{DD}$ respectively.

From I_D vs V_{GS} characteristics shown in Fig. 4(a) it can be seen that, with increasing N_{DSL} at fixed L_{DSL} of 11 nm, the reduced contact resistance at S/D-to-channel interface improves I_{ON} of DSSB SOI MOSFET. However, as can be seen from Fig. 4(a)-(b) with increasing N_{DSL} the I_{OFF}, *S* and DIBL of this device also increases. Thus, although by increasing N_{DSL} the improved I_{ON} due to narrow SB width improves high frequency performance, the increased I_{OFF}, *S* and DIBL deteriorates the scalability of the device.

On the other hand, decreasing L_{DSL} at fixed N_{DSL} of 1 × 10^{20} cm^{-3} increases the effective channel length of DSSB SOI MOSFET, due to which *S*, DIBL and GIDL of this device reduces as compared to RSD UTB. However, with decreasing L_{DSL} the increased voltage drop across the underlap lengths can reduce the effective gate voltage of DSSB SOI MOSFET [19], due to which the drive current of this device reduces as compared to RSD UTB. Thus, since increasing N_{DSL} of DSSB SOI MOSFET improves I_{ON} at the cost of increased short-channel effects and decreasing L_{DSL} reduces I_{OFF}, I_{ON} and the short-channel effects, a trade-off has been established



(a)



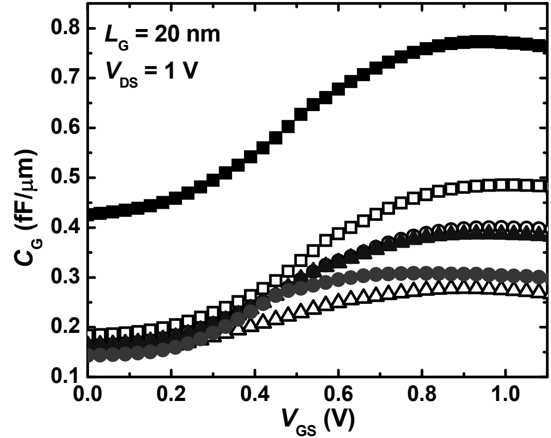
(b)

Fig. 4. (a) I_D vs V_{GS} characteristics and (b) Variation of S and DIBL with L_G for RSD UTB and DSSB SOI MOSFETs. Notations: ■-■: RSD UTB; Δ-Δ: L_{DSL} = 11 nm, N_{DSL} = 5 × 10^{19} cm^{-3}; ○-○: L_{DSL} = 11 nm, N_{DSL} = 1 × 10^{20} cm^{-3}; □-□: L_{DSL} = 11 nm, N_{DSL} = 5 × 10^{20} cm^{-3}; ●-●: L_{DSL} = 5 nm, N_{DSL} =1 × 10^{20} cm^{-3}; ▲-▲: L_{DSL}= 10 nm, N_{DSL} = 1 × 10^{20} cm^{-3}.

between high frequency performance and the scalability of this device.

3. Analog Performance

The key figures of merit which characterize the analog performance of a MOSFET are the output conductance (g_d), transconductance (g_m), intrinsic gain (g_m/g_d) and the transconductance generation factor (g_m/I_D) of the device [20, 21]. Further, the gate capacitance (C_G) which is normally defined as the sum of parasitic gate-to-source (C_{gs}) and gate-to-drain (C_{gd}) capacitances plays a vital role in analog circuits. Fig. 5 shows the variation of C_G, g_m and g_d as a function of V_{GS} for RSD UTB and DSSB SOI MOSFET with various N_{DSL} and L_{DSL} values.



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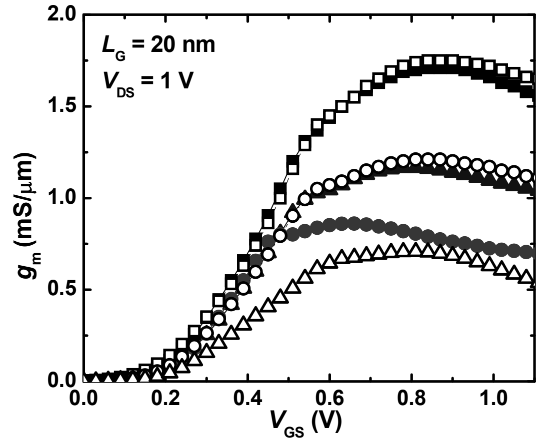

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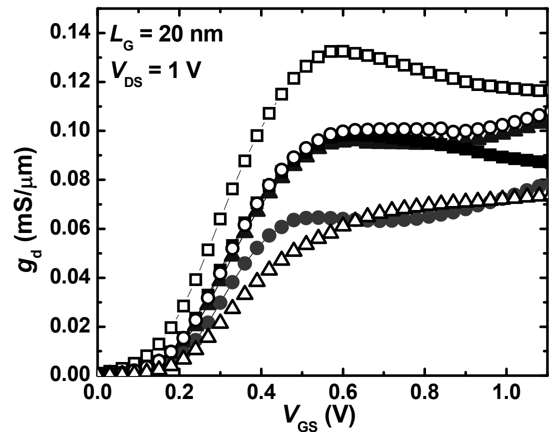


(c)

Fig. 5. Variation of (a) C_G, (b) g_m and (c) g_d with V_{GS} for RSD UTB and DSSB SOI MOSFETs. Notations: ■-■: RSD UTB; Δ-Δ: L_{DSL} = 11 nm, N_{DSL} = 5 × 10^{19} cm^{-3}; ○-○: L_{DSL}= 11 nm, N_{DSL} = 1 × 10^{20} cm^{-3}; □-□: L_{DSL} = 11 nm, N_{DSL} = 5 × 10^{20} cm^{-3}; ●-●: L_{DSL} = 5 nm, N_{DSL} = 1 × 10^{20} cm^{-3}; ▲-▲: L_{DSL} = 10 nm, N_{DSL} = 1 × 10^{20} cm^{-3}.

From Fig. 5(a) it can be seen that, although increasing N_{DSL} and L_{DSL} of DSSB SOI MOSFET leads to an increase in C_G, in comparison to RSD UTB the increase in C_G is significantly low. This is mainly because of the planar structure of DSSB SOI MOSFET. Further, since an overlap channel of length 1 nm and an underlap channel of length 5 nm is present at L_{DSL} = 11 nm and L_{DSL} = 5 nm respectively, C_G at L_{DSL} = 11 nm is larger as compared L_{DSL} = 5 nm.

Further, from Fig. 5(b) it can be seen that, increasing N_{DSL} at L_{DSL} = 11 nm, the reduced S/D-to-channel contact resistance improves g_m of DSSB SOI MOSFET [11]. However, as can be seen from Fig. 5(c), the increased channel length modulation (CLM) effect also increases g_d of the device. On the other hand, at L_{DSL} = 5 nm both g_m and g_d of the device are lower and with increasing L_{DSL} at fixed N_{DSL} of 1×10^{20} cm^{-3} both the parameters are increasing. Since increasing L_{DSL} reduces the underlap channel length, the voltage drop across the underlap lengths also reduces, due to which the series resistance across the underlap lengths reduces and hence improves g_m of the device. Further, with increasing L_{DSL} the reduced effective channel length increases CLM effect and hence increases g_d of the device.

Fig. 6 shows the impact of L_{DSL} and N_{DSL} on g_m/g_d and g_m/I_D of DSSB SOI MOSFET. From Fig 6(a) it can be seen that, with increasing N_{DSL} at fixed L_{DSL} of 11 nm, g_m/g_d in strong inversion region improves whereas in weak inversion region it reduces. Further, although by increasing N_{DSL} in DSSB SOI MOSFET g_m of this device improves as compared to RSD UTB, the increased g_d with increasing N_{DSL} reduces g_m/g_d of the device. On the other hand, despite reducing L_{DSL} of DSSB SOI MOSFET reduces g_m of this device, in weak inversion region the significant reduction in g_d improves g_m/g_d of the device.

Further, from Fig. 6(b) it can be seen that by increasing N_{DSL} at fixed L_{DSL} = 11 nm g_m/I_D of DSSB SOI MOSFET reduces in weak inversion region whereas in strong inversion region it improves. On the other hand, by reducing L_{DSL} at fixed N_{DSL} of 1×10^{20} cm^{-3}, g_m/I_D of DSSB SOI MOSFET improves in weak inversion region whereas in strong inversion region it reduces. Thus, reducing L_{DSL} of DSSB SOI MOSFET increases the suitability of this device for low-power analog circuits whereas increasing N_{DSL} makes it suitable for high frequency analog circuit applications.

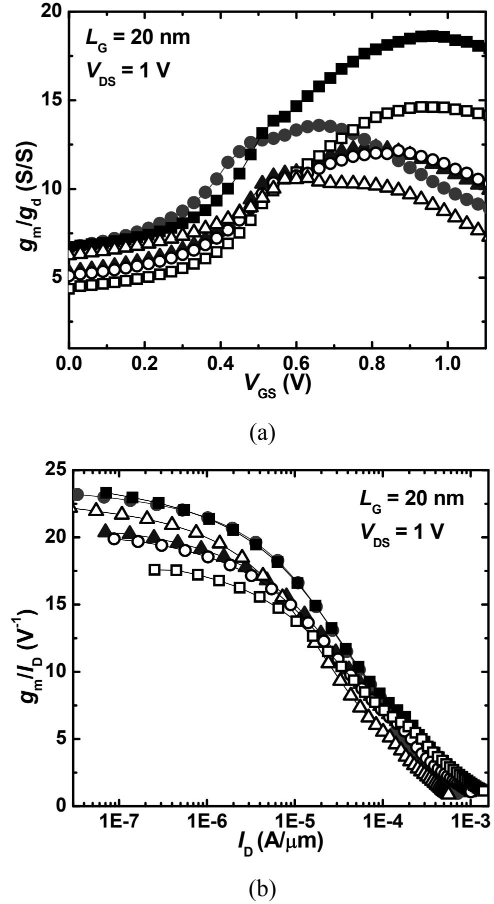


Fig. 6. Variation of (a) g_m/g_d with V_{GS} and (b) g_m/I_D with I_D for RSD UTB and DSSB SOI MOSFETs. Notations: ■-■: RSD UTB; Δ-Δ: L_{DSL} = 11 nm, N_{DSL} = 5×10^{19} cm^{-3}; ○-○: L_{DSL} = 11 nm, N_{DSL} = 1×10^{20} cm^{-3}; □-□: L_{DSL} = 11 nm, N_{DSL} = 5×10^{20} cm^{-3}; ●-●: L_{DSL} = 5 nm, N_{DSL} = 1×10^{20} cm^{-3}; ▲-▲: L_{DSL} = 10 nm, N_{DSL} = 1×10^{20} cm^{-3}.

4. RF Performance

The RF performance is mainly characterized by unity-gain frequency (F_t), maximum power gain frequency (F_{max}), short-circuit current gain (A_{ishort}) and unilateral power gain (U) of a MOSFET [21, 22]. The A_{ishort} and U interms of Y-parameters can be expressed as [22, 23]

$$A_{ishort} = \frac{Y_{21}}{Y_{11}}, \tag{2}$$

$$U = \frac{|Y_{21} - Y_{12}|^2}{4[\mathrm{Re}(Y_{11})\,\mathrm{Re}(Y_{22}) - \mathrm{Re}(Y_{12})\,\mathrm{Re}(Y_{21})]}. \tag{3}$$

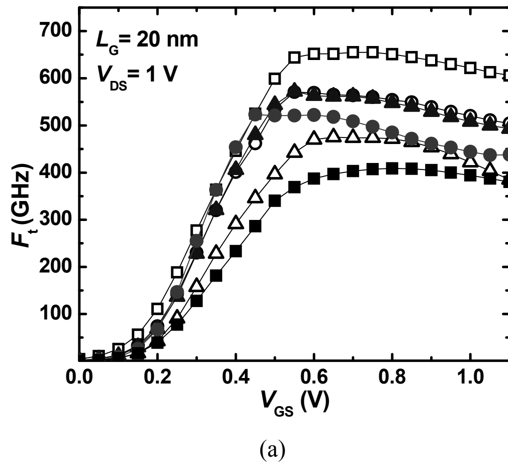
From these equations F_t and F_{max} can be approximated by considering the small-signal equivalent circuit model of a long-channel MOSFET. Fig. 7 shows the variation of F_t and F_{max} as a function of V_{GS} for RSD UTB and DSSB SOI MOSFETs at various N_{DSL} and L_{DSL} values. Here, instead of using approximated F_t and F_{max} equations, Y-parameter matrix generated by performing the small-signal ac analysis has been used to get the exact values of F_t and F_{max}. The equations used for extracting F_t and F_{max} are [21]

$$F_t = f_0 \times |A_{ishort}|, \quad (4)$$

$$F_{Max} = f_0 \times \sqrt{\frac{|Y_{21} - Y_{12}|^2}{4[\mathrm{Re}(Y_{11})\,\mathrm{Re}(Y_{22}) - \mathrm{Re}(Y_{12})\,\mathrm{Re}(Y_{21})]}}, \quad (5)$$

where f_0 is the small-signal frequency. From these equations, F_t and F_{max} have been extracted by varying f_0 from 1 MHz to 1 THz and recorded when A_{ishort} and U rolls-off to unity.

From Fig. 7 it can be seen that, by increasing N_{DSL} at L_{DSL} = 11 nm both F_t and F_{max} of DSSB SOI MOSFET improves as compared to RSD UTB. This is mainly due to improvement in g_m of DSSB SOI MOSFET. Further, in spite of having reduced g_m at L_{DSL} = 5 nm, the significant reduction in parasitic capacitances improves both F_t and F_{max} of DSSB SOI MOSFET. In addition to this, from Fig. 8 it can be seen that, with increasing N_{DSL} of DSSB SOI MOSFET both A_{ishort} and U of this device improves as compared to RSD UTB. This is also attributed to improvement in g_m of DSSB SOI MOSFET.



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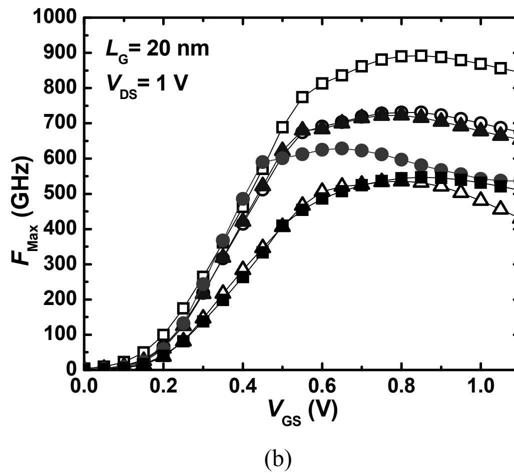
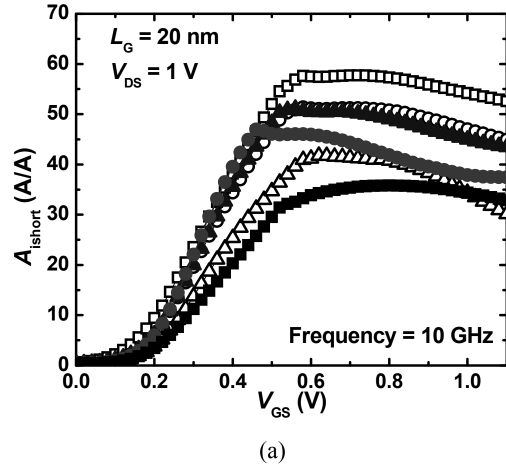


(b)

Fig. 7. Variation of (a) F_t and (b) F_{Max} with V_{GS} for RSD UTB and DSSB SOI MOSFETs. Notations: ■-■: RSD UTB; Δ-Δ: L_{DSL} = 11 nm, N_{DSL} = 5 × 10^{19} cm^{-3}; ○-○: L_{DSL} = 11 nm, N_{DSL} = 1 × 10^{20} cm^{-3}; □-□: L_{DSL} = 11 nm, N_{DSL} = 5 × 10^{20} cm^{-3}; ●-●: L_{DSL} = 5 nm, N_{DSL} = 1 × 10^{20} cm^{-3}; ▲-▲: L_{DSL} = 10 nm, N_{DSL} = 1 × 10^{20} cm^{-3}.



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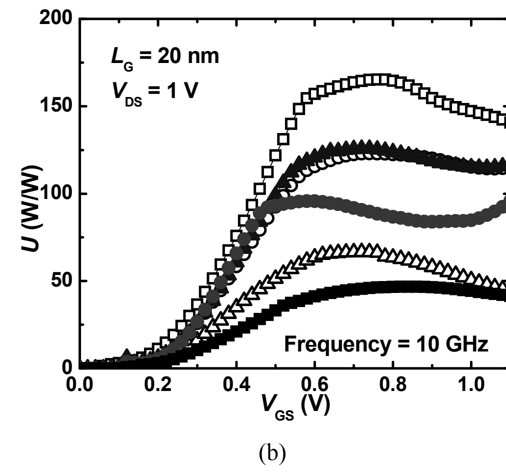


(b)

Fig. 8. Variation of (a) A_{ishort} and (b) U with V_{GS} for RSD UTB and DSSB SOI MOSFETs. Notations: ■-■: RSD UTB; Δ-Δ: L_{DSL} = 11 nm, N_{DSL} = 5 × 10^{19} cm^{-3}; ○-○: L_{DSL} = 11 nm, N_{DSL} = 1 × 10^{20} cm^{-3}; □-□: L_{DSL} = 11 nm, N_{DSL} = 5 × 10^{20} cm^{-3}; ●-●: L_{DSL} = 5 nm, N_{DSL} = 1 × 10^{20} cm^{-3}; ▲-▲: L_{DSL} = 10 nm, N_{DSL} = 1 × 10^{20} cm^{-3}.

Thus, optimizing N_{DSL} and L_{DSL} of DSSB SOI MOSFET leads to significant improvement in RF performance of this device even when compared with RSD UTB.

Since the gate oxide thickness of 1 nm has been considered, the direct tunneling through the thin oxide can lead to an increase in the gate leakage current [17], which may lead to marginal variations in the values of I_{ON}, I_{OFF} and the analog/RF figures of merit of the devices. However, since the focus of this work is to study the significance of N_{DSL} and L_{DSL} on DSSB SOI device design and optimization, even with such a thin gate oxide the overall conclusions of this work would remain unchanged.

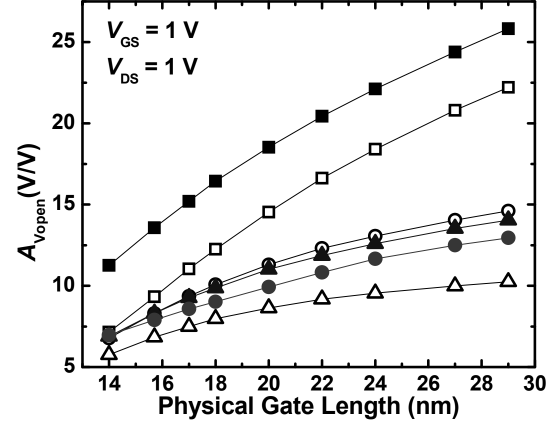
5. Analog Circuit Performance

In order to evaluate the impact of N_{DSL} and L_{DSL} on analog circuit performance of DSSB SOI MOSFET a common-source (CS) amplifier based on this device has been analyzed. The Y-parameter matrix obtained during small-signal ac analysis has been further used to extract the intrinsic open-circuit voltage gain (A_{Vopen}) and 3-dB bandwidth (F_{3dB}) of the devices. The A_{Vopen} interms of Y-parameters can be expressed as [22]

$$A_{vopen} = \frac{Y_{21}}{Y_{22}}. \tag{6}$$

By using this expression the frequency response of CS amplifier has been obtained at various L_G values from which F_{3dB} of all the devices has been extracted. Fig. 9 shows the variation of F_{3dB}, A_{Vopen}, and the gain-bandwidth product (GBP) as a function of L_G for RSD UTB and DSSB SOI MOSFET with various N_{DSL} and L_{DSL} values.

From Fig. 9(a) it can be seen that, although increasing N_{DSL} and L_{DSL} of DSSB SOI MOSFET improves A_{Vopen} of DSSB SOI amplifier, this improvement in A_{Vopen} is significantly low as compared to RSD UTB amplifier. However, as can be seen from Fig. 9(b), with increasing N_{DSL} and L_{DSL} of DSSB SOI MOSFET, F_{3dB} of DSSB SOI amplifier improves as compared to RSD UTB amplifier. Further, from Fig. 9(c) it can be seen that, despite having reduced A_{Vopen} in N_{DSL} and L_{DSL} optimized DSSB SOI amplifier, GBP of this amplifier is ~40% higher over the RSD UTB amplifier. Thus, optimizing N_{DSL} and L_{DSL} of DSSB SOI MOSFET improves the analog/RF circuit performance of this device.



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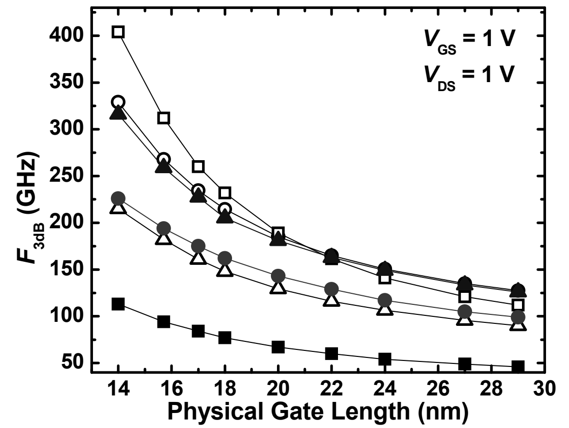

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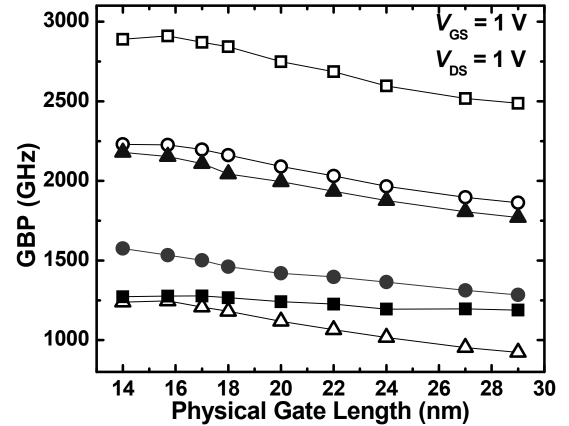

(c)

Fig. 9. Variation of (a) A_{vopen} (b) F_{3dB} and (c) GBP with L_G for RSD UTB and DSSB SOI MOSFETs. Notations: ■-■: RSD UTB; Δ-Δ: L_{DSL}=11 nm, N_{DSL}=5 × 10^{19} cm^{-3}; ○-○: L_{DSL}= 11 nm, N_{DSL} = 1 × 10^{20} cm^{-3}; □-□: L_{DSL} = 11 nm, N_{DSL} = 5 × 10^{20} cm^{-3}; ●-●: L_{DSL}= 5 nm, N_{DSL} = 1 × 10^{20} cm^{-3}; ▲-▲: L_{DSL} = 10 nm, N_{DSL} = 1 × 10^{20} cm^{-3}.

IV. CONCLUSIONS

The impact of N_{DSL} and L_{DSL} on scalability and analog/RF performance of DSSB SOI MOSFET has been investigated by using the numerical simulations. The results show that increasing N_{DSL} at fixed L_{DSL} the narrowed SB width at S/D-to-channel interface leads to significant improvement in the analog/RF figures of merit of this device even when compared with RSD UTB. However, in comparison to RSD UTB, the increased short-channel effects and the off-state leakage limits the scalability of this device. On the other hand, reducing L_{DSL} at fixed N_{DSL}, the increased effective channel length improves the scalability of DSSB SOI MOSFET. However, at lower L_{DSL} the voltage drop across the underlap lengths at S/D deteriorates the analog/RF performance of this device. Thus, a trade-off between scalability and the analog/RF performance of DSSB SOI MOSFET has been established in sub-30 nm regime.

Further, the results of small-signal ac analysis of CS amplifier show that, GBP in the case of N_{DSL} and L_{DSL} optimized DSSB SOI amplifier has significantly improved over an amplifier based on RSD UTB. In addition to this, with scaling L_G beyond sub-30 nm regime the improvement in GBP is almost constant. This clearly shows that, optimizing N_{DSL} and L_{DSL} of DSSB SOI MOSFET makes it a better choice for future analog/RF technology nodes.

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