A Study on the Electrical Characteristic Analysis of c-Si Solar Cell Diodes

Pyungho Choi, Hyojung Kim, Dohyun Baek, and Byoungdeog Choi

Abstract—**A study on the electrical characteristic analysis of solar cell diodes under experimental conditions of varying temperature and frequency has been conducted. From the current-voltage (I-V) measurements, at the room temperature, we obtained the ideality factor (n) for Space Charge Region (SCR) and Quasi-Neutral Region (QNR) of 3.02 and 1.76, respectively. Characteristics showed that the value of n (at SCR) decreases with rising temperature and n (at QNR) increases with the same conditions. These are due to not only the sharply increased SCR current flow but the activated carrier recombination in the bulk region caused by defects such as contamination, dangling bonds. In addition, from the I-V measurements implemented to confirm the junction uniformity of cells, the average current dispersion was 40.87% and 10.59% at the region of SCR and QNR, respectively. These phenomena were caused by the pyramidal textured junction structure formed to improve the light absorption on the device's front surface, and these affect to the total diode current flow. These defect and textured junction structure will be causes that solar cell diodes have non-ideal electrical characteristics compared with general p-n junction diodes. Also, through the capacitance-voltage (C-V) measurements under the frequency of 180 kHz, we confirmed that the value of built-in potential is 0.63 V.**

Index Terms—**Solar cell diodes, junction uniformity, non-ideal characteristic, I-V, C-V**

I. INTRODUCTION

Analysis of diode parameters extracted from the I-V curve of solar cell diodes is a well-known technique for determining device behavior. Analysis methods of I-V characteristics have been introduced in precursory studies [1-7]. Defects such as metal contamination, dislocation and dangling bonds, which should be responsible for carrier movement, are expected to lead to non-ideal I-V characteristics under applied bias voltages [8]. Further, traditionally, solar cell diodes have pyramidal textured junction structures to improve the light absorption on the front surface of the device [9-11]. However, from the viewpoint of electrical properties, these result in adverse effects on total current, especially, junction current flow. In this report, to confirm these non-ideal characteristics, the ideality factor which is a crucial criterion that determines device performance was investigated with varying temperature, and then computed values were obtained using conventional calculation methods. Also, we have qualitatively analyzed the current flow at the region of SCR and QNR. Especially, we investigated an analysis of junction uniformity through the conventional I-V measurement and calculation method.

The series resistance (R_S) of the diode is also an important parameter that has been found to depend on bias voltages and frequencies [12, 13]. This can be acquired from C-V and conductance-voltage (G-V) measurements [13]. In this study, we analyzed R_S characteristic in order to determine an important diode

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parameter V_{bi}, for the frequency range of 20 kHz - 180 kHz.

II. EXPERIMENTAL DETAILS

In this study, we manufactured single-crystalline silicon solar cells. Previously, p-type bare wafers that have (100) directions were dipped in alkaline solution for Saw Damage Removal (SDR) and pyramidal texturing. And then n-type doping using phosphorus diffusion in a thermal furnace was implemented. A SiNx Anti-Reflection Coating (ARC) layer with a thickness of ~ 75 nm and a refractive index of ~ 2.0 was deposited on a doped surface by the Plasma Enhanced Chemical Vapor Deposition (PECVD) method. Then metal contacts (~ 20 μm thickness) were formed on the rear surface with aluminum paste and on the front with silver paste, by the conventional screen printing technique. Finally, the samples have been co-fired in a conveyer belt for the Back Surface Fields (BSF) formation.

In order to investigate the electrical characteristics of solar cell diodes, I-V measurement was performed using an Agilent semiconductor analyzer in the dark condition. Forward bias was applied from 0 V to 0.8 V with a temperature range of 300 K - 500 K. We obtained values for the ideality factor and saturation current density of solar cell diodes in the SCR and QNR, respectively. Further, a number of samples which have been manufactured in a batch process were measured to confirm the junction uniformity of the device.

And then C-V and G-V measurements were implemented with a frequency range of 20 kHz - 180 kHz using a LCR meter. Also, we have investigated the R_S-V characteristic from the measured values of capacitance and conductance using the calculation method. And the value of V_{bi} was obtained by extrapolating the C^{-2}-V plot to the voltage axis. Finally, we extracted the substrate doping profile from the equation solutions.

III. RESULTS AND DISCUSSION

1. I-V characteristics

Fig. 1 shows the forward bias semi-logarithmic J-V plot measured for varying temperatures. We confirmed that the diode current increases with applied voltage and the plot has two different slopes. Generally, the diode characteristics are explained by Eqs. (1-5),

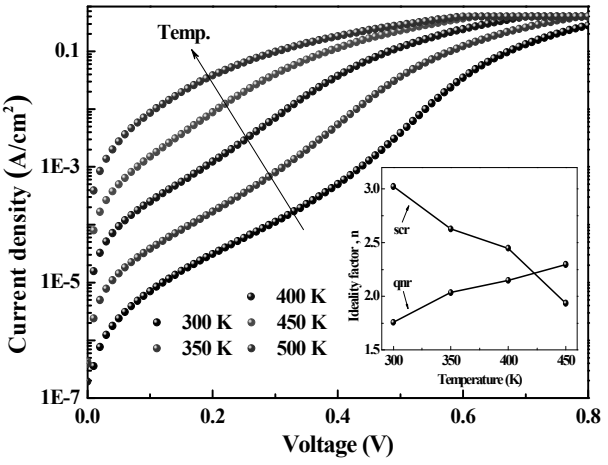

Fig. 1. Forward bias log J-V curves and ideality factors with varying temperature.

$$J = J_{sat}(e^{qV/nkT} - 1) \tag{1}$$

$$J_{sat} = qn_i^2(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}) \tag{2}$$

$$n_i = (9.15\times10^{19})(\frac{T}{300})^2 e^{-0.5928/kT} \tag{3}$$

$$J_{R-G} = \frac{qn_i}{2\tau_0} W \frac{(e^{qV_A/nkT} - 1)}{(1 + \frac{V_{bi} - V_A}{kT/q}\frac{\sqrt{\tau_n \tau_p}}{2\tau_0} e^{qV_A/2nkT})} \tag{4}$$

$$J_{Diff.} = qn_i^2(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A})(e^{qV_A/nkT} - 1) \tag{5}$$

where $\boldsymbol{J_{sat}}$ is the saturation current density, $\boldsymbol{q}$ is the electrical charge, $\boldsymbol{n}$ is the ideality factor, $\boldsymbol{k}$ is the Boltzmann constant, $\boldsymbol{T}$ is the Kelvin temperature, $\boldsymbol{n_i}$ is the intrinsic carrier density, $\boldsymbol{D}$ is the diffusion coefficient, $\boldsymbol{L}$ is the diffusion length, $\boldsymbol{N}$ is the carrier doping density, $\boldsymbol{J_{R\text{-}G}}$ is the recombination-generation current density in the depletion region, $\boldsymbol{J_{Diff.}}$ is the diffusion current density in bulk, and τ is the carrier life-time.

We used the above diode equations in order to determine the ideality factor n and saturation current

Table 1. Calculated values of characteristic parameters of solar cell diodes

	Temp. (K)	Slope (dJ/dV)	n	J_{sat} (A/cm^2)
SCR	300	5.55	3.02	2.43×10^{-6}
	350	6.39	2.63	9.04×10^{-6}
	400	6.86	2.45	5.23×10^{-5}
	450	8.67	1.94	1.85×10^{-4}
QNR	300	9.60	1.76	6.52×10^{-8}
	350	8.25	2.04	2.73×10^{-6}
	400	7.81	2.15	3.21×10^{-5}
	450	7.31	2.30	2.97×10^{-4}

density J_{sat}. Calculated values are presented in Table. 1. In the ideal case, the ideality factors of general p-n junction diodes have been presented with values of ~ 2 and ~ 1 in the SCR and QNR regions, respectively, under room temperature [1, 2]. In this study we obtained values for n_{scr}, n_{qnr} of 3.02 and 1.76, respectively, and we obtained values for saturation current density of 2.43 × 10^{-6} A/cm^2 and 6.52 × 10^{-8} A/cm^2 , respectively, under 300 K dark conditions. Compared with general p-n junction diodes, solar cell devices have been manufactured under a large-scale process, so there should be several defects, not only in the space-charge region but also in the bulk substrate. These defects are caused by contamination, dangling bonds and pyramidal textured junction structure. So the characteristics of the ideality factor and saturation current density were revealed with larger values. Based on Fig. 1, we can infer that the total diode current is increased with increasing temperature. According to Eq. (3) n_i is proportional to the square of temperature. So the total diode current, sum of Eqs. (4, 5), underwent an absolute increase in the SCR and QNR regions. However, as can be seen in Fig. 1 and Table 1, the curve slopes in the QNR decrease with increasing temperature, while the slopes in the SCR are increased. This can be explained by thermally generated trapping sites to cause carrier recombination in the bulk region, which increase with rising temperature. So the value of n_{qnr} increases. In opposite, the depletion width becomes narrowing with increasing temperature. Therefore at the low applied forward bias region, the value of n_{scr} decreases.

As can be seen in Fig. 2, solar cell diodes have pyramidal textured junction features with varying dimensions. In case of solar cells, the process of junction texturing is a very important factor for improving light absorption on the front surface. However in the description

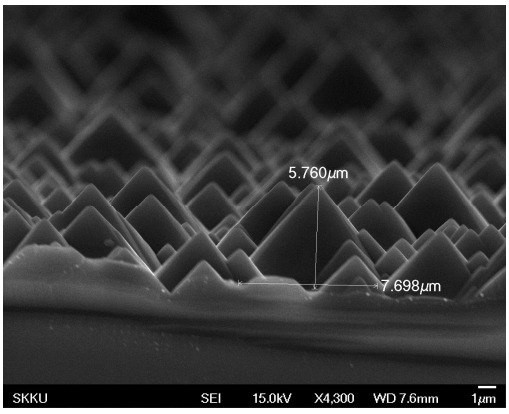

Fig. 2. SEM image of pyramidal textured junction structure.

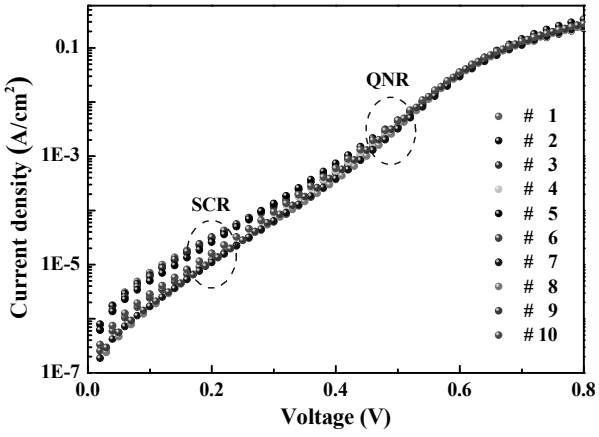

Fig. 3. Log J-V plots of a number of samples.

of diode characteristics, the electrical parameters (n, J_{sat}) of the solar device exhibit poor performance. These influence the diode current flow, especially in the low applied voltage region. Fig. 3 presents the forward bias J-V plots of a number of solar devices manufactured in an equivalent fabrication process and Fig. 4 shows current dispersion in the region of SCR and QNR, respectively. In Fig. 3, we can see that SCR current dispersion at 0.2 V is larger than QNR current dispersion at 0.5 V and this can be confirmed by Fig. 4. In Fig. 4, compare with average current flow in the regions of SCR and QNR, the SCR current shows the range of dispersion from 18.83% to 63.17% and QNR current shows the range of dispersion from 1.17% to 18.90%. Current dispersion affect to the total diode's current flow that has been presented by sum of Eqs. (4, 5). Especially the SCR current dispersion affect to the R-G current flow explained in Eq. (4). So SCR current dispersion caused by junction textured structure would vary the total

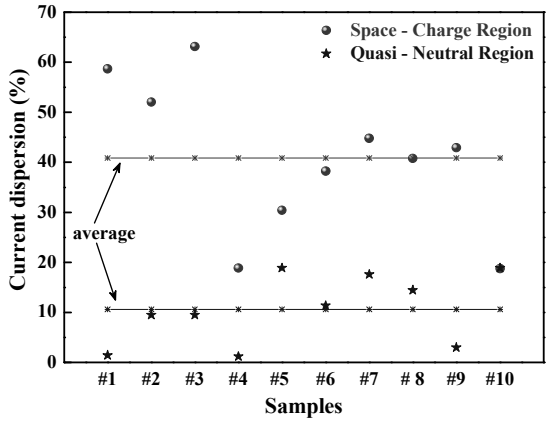

Fig. 4. The comparison of current dispersion in SCR and QNR regions.

diode's current flow that is related with short circuit current density, J_{sc}.

2. C-V characteristics

In order to analyze the electrical behavior of solar cell diodes, analysis of capacitance, conductance and series resistance vs. voltage characteristics has been investigated. Fig. 5 shows the experimental results of C-V measured in a frequency range of 20 kHz to 180 kHz in reverse and forward bias conditions. The depletion width (W) and capacitance depend on bias conditions, as explained by Eqs. (6, 7),

$$C = A\sqrt{\frac{qk_s\varepsilon_0 N_A}{2(V_{bi}-V)}} \tag{6}$$

$$W = \sqrt{\frac{2k_s\varepsilon_0(V_{bi}-V)}{qN_A}} \tag{7}$$

where $\boldsymbol{W}$ is the depletion width, $\boldsymbol{k_s}$ is the dielectric constant of silicon, $\boldsymbol{\varepsilon_o}$ is the vacuum permittivity, $\boldsymbol{V_{bi}}$ is the built-in potential, $\boldsymbol{N_A}$ is the substrate doping density, and $\boldsymbol{A}$ is the diode area.

As can be seen in Fig. 5, the capacitance increases with forward bias and it does not depend on frequencies in reverse bias conditions, on the other hand, it decreases with increasing frequencies in forward bias conditions. If the depletion region was formed by sufficient reverse bias, then the variation of depletion width by the Alternating Current (AC) signal will be negligible. In case of forward bias conditions at lower frequencies, carriers can easily follow the AC signal. However in high frequency conditions, carriers cannot easily react to the AC signal. So we can recognize the frequency dependence of this device from the Fig. 5.

Figs. 6 and 7 show G-V and Rs-V plots with varying frequencies. And these figures are explained by the following Eqs. (8-10),

$$Z = R + 1/\,j\omega C \tag{8}$$

$$Y = G + j\omega C \tag{9}$$

$$R_S = \frac{1}{G[1+(\omega C/G)^2]} \tag{10}$$

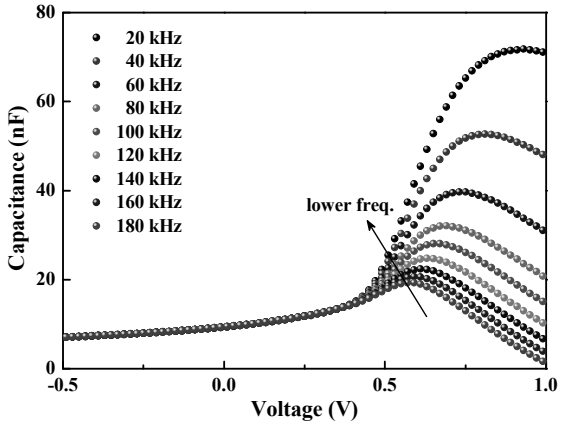

Fig. 5. C-V plots measured with frequency range of 20 kHz to 180 kHz.

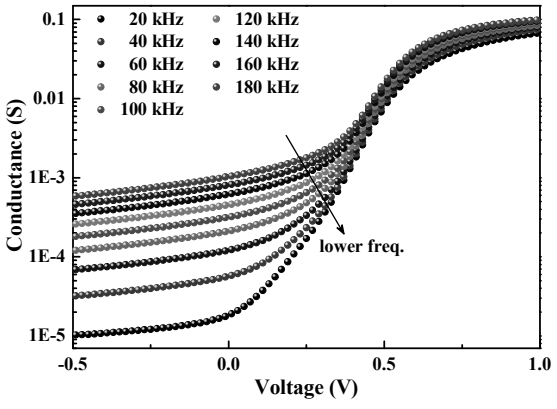

Fig. 6. Log scaled G-V plots measured with frequency range of 20 kHz to 180 kHz.

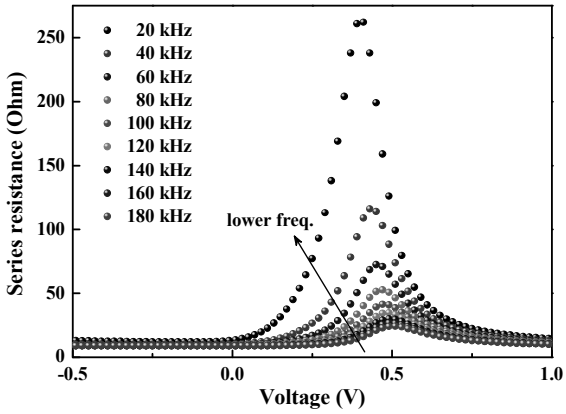

Fig. 7. RS-V plots characterized from measured C-V, G-V values.

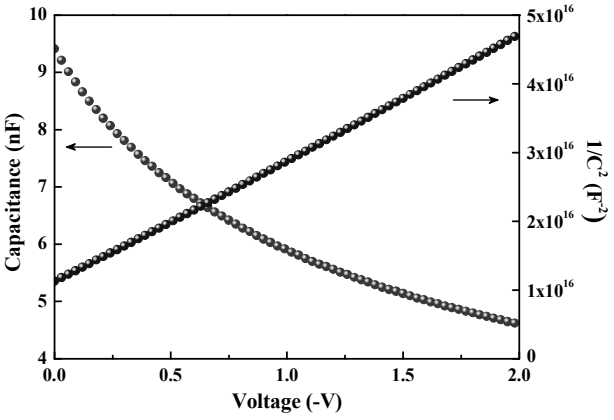

Fig. 8. C-V and C-2-V characteristics measured at the frequency of 180 kHz.

$$N_A(W) = \frac{2}{qk_s\varepsilon_0 A^2\, d(1/C^2)/dV} \tag{11}$$

where ***Z*** is the impedance, ***ω(=2πf)*** is the angular frequency, ***1/ jωC*** is the reactance, ***Y*** is the admittance, and ***jωC*** is the susceptance, ***$N_A(W)$*** is the substrate doping density.

Fig. 6 presents lower conductance values at lower frequencies. According to Eqs. (8, 9), Direct Current (DC) signals (*frequency* = 0) namely, signals which have lower frequencies, have been blocked by the capacitor. So the impedance (*Z*, stated as resistance in figs.) increases with decreasing frequency as opposed to reduced admittance (*Y*, stated as conductance in figs.). And in reverse bias conditions, because of the increased series resistance affected by the expansion of depletion width, the conductance has lower values than in forward conditions. Based on the measured values of C and G, using the calculation method (Eq. (10)), we obtained R_S-V plots and these have been presented in Fig. 7. At the frequency of 180 kHz, we confirmed the minimum value of R_S. We can infer that the impedance factor interpreted by Eq. (8) decreases with higher frequencies according to the degradation of the reactance factor. So extraction of the V_{bi} parameter was conducted at the frequency of 180 kHz. Based on the calculation method in this study, V_{bi}, was obtained by extrapolating the C^{-2}-V plot to the voltage axis, and these plots have been presented in Fig. 8. We confirmed the V_{bi} value of 0.63 V. And we also extracted the substrate doping profile from the measured C-V characteristics using the calculation method in Eq. (11). Fig. 9 shows that substrate doping density has the

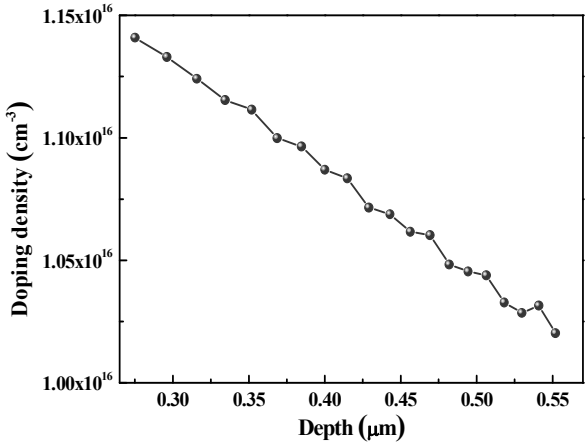

Fig. 9. Substrate doping profiles extracted using calculation method.

range of 1.15×10^{16} cm^{-3} to 1.0×10^{16} cm^{-3} with respect to substrate doping depth.

IV. CONCLUSIONS

The ideality factor is an important parameter for device performance. In this study, we analyzed the solar cell diode's electrical characteristics. Due to defective factors caused by contamination, dangling bonds and textured junction features, the ideality factor investigated in this study showed poor characteristics compared with precursory studies. In case of the measurement for the junction uniformity analysis of junction textured structure, current dispersion was more prominent in the low forward bias region than the high applied bias region. We can consider that the pyramidal textured junction structure which was formed to increase the light

absorption on the front surface affects to the total diode's current flow, especially for the R-G current flow. Also based on the C-V analysis, we confirmed that R_S has a reasonable value at the high frequency of 180 kHz for determining V_{bi}.

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