A "Thru-Short-Open" De-embedding Method for Accurate On-Wafer RF Measurements of Nano-Scale MOSFETs

Ju-Young Kim, Min-Kwon Choi, and Seonghearn Lee

***Abstract*—A new on-wafer de-embedding method using thru, short and open patterns sequentially is proposed to eliminate the errors of conventional methods. This "thru-short-open" method is based on the removal of the coupling admittance between input and output interconnect dangling legs. The increase of the de-embedding effect of the lossy coupling capacitance on the cutoff frequency in MOSFETs is observed as the gate length is scaled down to 45 nm. This method will be very useful for accurate RF measurements of nano-scale MOSFETs.**

***Index Terms*—MOSFET, nano-scale CMOS, de-embedding, coupling capacitance, RF, on-wafer measurement, S-parameter measurement**

I. INTRODUCTION

With the rapid growth of personal wireless communication markets, low-cost silicon RF integrated circuits have emerged. In order to design the RF ICs successfully, designers require accurate and reliable RF device models for simulation. S-parameter data measured from on-wafer test patterns are required to extract RF model parameters. The influence of surrounding parasitic elements in on-wafer test patterns on the S-parameter measurements has become increasingly important because the intrinsic MOS capacitance is substantially reduced with the continuous down-scaling of gate length dimensions to a nano-scale regime. As shown in Fig. 1(a), an on-wafer test pattern consists of not only an actual device-under-test (DUT) but also RF probe pads and interconnections. Accurate intrinsic device model parameter extraction is prevented because the pads and interconnections contain parasitic elements such as capacitance, resistance, and inductance. In order to obtain the actual nano-scale MOSFET characteristics without the influence of the pads and interconnections, an accurate de-embedding procedure must be performed.

Several de-embedding approaches based on a lumped equivalent circuit-model [1-5] with parasitic impedances and admittances for representing the probe pads and interconnects on silicon substrate have been reported previously. The lumped equivalent circuit-model-based techniques using short and open de-embedding patterns in Fig. 1(b) may not work well in the high frequency region, because these techniques neglect the distributed lossy transmission line effect in the metallic interconnects on silicon substrate. In order to overcome the drawbacks of the lumped equivalent circuit-model-based techniques, cascade-based techniques that model the input/output adapters (the pads and interconnects) and the DUT as a cascade connection of two-port networks in Fig. 2(a) have been proposed. However, the cascade-based techniques that use only one thru de-embedding pattern in Fig. 1(b), so called, a thru-only method [6-8] based on the equivalent circuit of Fig. 2(a) neglect parasitics of a source interconnect. In order to consider this effect, a thru-short method [9] considering the source interconnect

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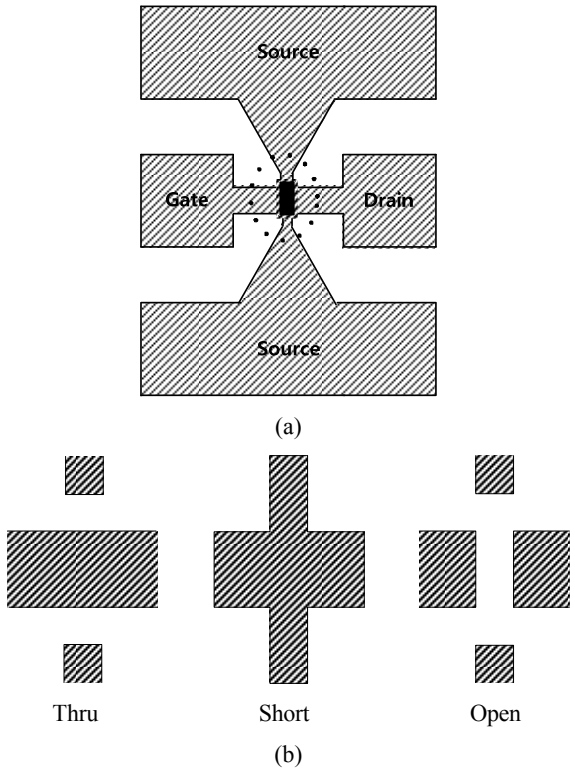


Fig. 1. (a) Layout of the on-wafer test pattern containing DUT in the area enclosed by the dotted circle, (b) Magnified view of three de-embedding patterns.

impedance Z_s of Fig. 2(b) using a short pattern has been proposed. However, this method neglects the coupling admittance between the dangling legs of gate and drain interconnects. It is very important to eliminate the coupling admittance in nano-scale MOSFETs, because the de-embedding effect of the lossy coupling capacitance increases with decreasing gate length and width due to the reduction of intrinsic device capacitances.

Therefore, in this paper, we propose a new thru-short-open de-embedding method based on the equivalent circuit of Fig. 2(c) to eliminate the coupling admittance using an open pattern in Fig. 1.

II. DE-EMBEDDING PROCEDURE

S-parameters of the pads and interconnects referred as adapters in Fig. 2 are extracted from the following equations using the measured ones of the thru pattern [6]:

$$S_{11}{}^{adapter} = S_{22}{}^{adapter} = (S_{11}{}^{thru} + S_{22}{}^{thru})/(2 + S_{21}{}^{thru} + S_{12}{}^{thru}) \quad (1)$$

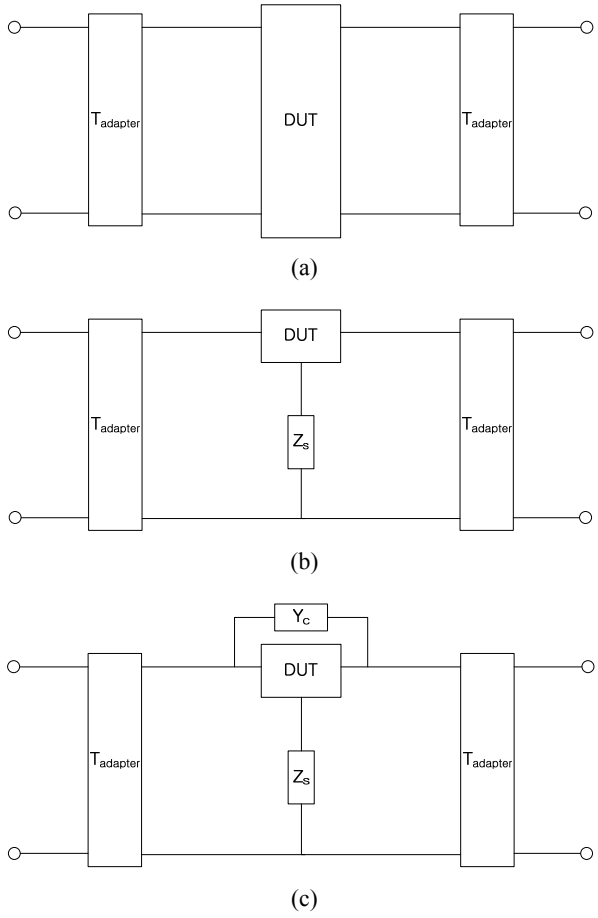


Fig. 2. An equivalent circuit representation for RF probe pads and interconnects in (a) Thru-only method, (b) Thru-short method and (c) Thru-short-open method.

$$S_{12}{}^{adapter} = S_{21}{}^{adapter} = \sqrt{0.5(S_{12}{}^{thru} + S_{21}{}^{thru})[1-(S_{11}{}^{adapter})^2]} \quad (2)$$

where the input and output adapters are assumed to be identical. Then the adapters are removed from measured DUT data as follows:

$$[T^{DA}] = [T^{adapter}]^{-1}[T^{DUT}][T^{adapter}]^{-1} \quad (3)$$

where $[T^{adapter}]$ and $[T^{DUT}]$ are the chain matrices of the adapter and DUT, respectively. However, the de-embedded S-parameters $[S^{dem}]$ converted from $[T^{DA}]$ using the conventional thru-only method [6-8] contain Z_s in Fig. 2(b). Thus, the thru-short method [9] has been applied to remove Z_s as follows:

The source interconnect chain matrix $[T^{SA}]$ can be extracted as :

$$[T^{SA}] = [T^{adapter}]^{-1}[T^{short}][T^{adapter}]^{-1} \quad (4)$$

where $[T^{short}]$ is the chain matrix of the short pattern. The source interconnect impedance Z_S is obtained by $[Z^{SA}]$ converted from $[T^{SA}]$:

$$Z_S = Z_{12}^{SA} \quad (5)$$

Then, Z_S is subtracted from the impedance matrix $[Z^{DA}]$ converted from $[T^{DA}]$:

$$[Z^{DAS}] = [Z^{DA}] - \begin{bmatrix} Z_S & Z_S \\ Z_S & Z_S \end{bmatrix} \quad (6)$$

However, the de-embedded S-parameters $[S^{dem}]$ converted from $[Z^{DAS}]$ using the thru-short method still include the coupling admittance Y_C in Fig. 2(c). In order to eliminate the coupling admittance, a thru-short-open method is newly proposed by the following procedures:

1) The input and output adapters are removed from the chain matrix $[T^{open}]$ of the open pattern:

$$[T^{OA}] = [T^{adapter}]^{-1}[T^{open}][T^{adapter}]^{-1} \quad (7)$$

2) $[T^{OA}]$ is converted to the impedance matrix $[Z^{OA}]$.

3) Z_S is subtracted from $[Z^{OA}]$:

$$[Z^{OAS}] = [Z^{OA}] - \begin{bmatrix} Z_S & Z_S \\ Z_S & Z_S \end{bmatrix} \quad (8)$$

4) Y_C is obtained by $[Y^{OAS}]$ converted from $[Z^{OAS}]$:

$$Y_C = -Y_{12}^{OAS} \quad (9)$$

5) Y_C is subtracted from $[Y^{DAS}]$ converted from $[Z^{DAS}]$:

$$[Y^{DASO}] = [Y^{DAS}] - \begin{bmatrix} Y_C & -Y_C \\ -Y_C & Y_C \end{bmatrix} \quad (10)$$

6) $[Y^{DASO}]$ is converted to $[S^{dem}]$.

III. RESULTS AND ANALYSIS

In order to investigate the de-embedding effect on the cutoff frequency f_T, S-parameters of NMOSFET of multi-finger type with different gate length L_g, the unit gate finger width W_u and the number of gate finger N_f are measured and de-embedded by three different methods described in the previous chapter.

Fig. 3 shows the current gain $|h_{21}|$ converted from the de-embedded S-parameters at L_g = 45 nm and 165 nm using the thru-only, thru-short and thru-short-open methods. The f_T values are extracted by extrapolating frequency response data of $|h_{21}|$ to 0 dB. As shown in Fig. 3, a f_T value of 180.6 GHz at L_g=45 nm using the new thru-short-open method is larger than those using the conventional thru-only and thru-short methods, because the lossy coupling capacitance between gate and drain interconnect dangling legs are eliminated after open de-embedding. However, the much smaller increase of f_T for the thru-short-open method compared to other methods is observed at L_g = 165 nm. The new thru-short-open method improves the accuracy in the high frequency range compared to a conventional three-step technique

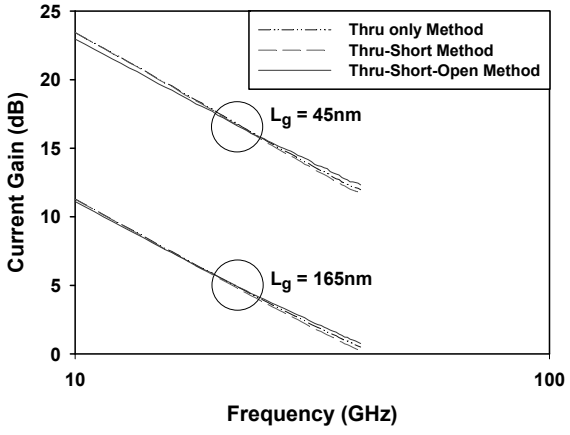


Fig. 3. The frequency response of the current gain at L_g=45 and 165 nm.

using a simple lumped equivalent circuit model [3, 4]. This is because the distributed effect of the pads and interconnections on a lossy silicon substrate is considered in the two-port network model in the new method.

Tables 1 and 2 show the f_T values of MOSFETs with various L_g and a total gate width W_t using three de-embedding methods, respectively. The percentage difference of f_T between the thru-short and thru-short-open methods increases with decreasing L_g and W_t, and reaches about 9.8% at L_g=45 nm. This indicates that the open de-embedding effect on the increase of f_T becomes larger at smaller L_g and W_t. However, f_T results for the thru-short method show smaller values than those for the thru-only one, because of the more negative slope of Fig. 3 in the high frequency range. This short de-embedding effect on f_T is due to the elimination of the source interconnect inductance.

In order to analyze the open de-embedding effect on f_T with decreasing L_g and W_t, the following equation is used:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd} + C_C)} \tag{11}$$

where g_m is the transconductance, C_{gs} is the gate-source capacitance, and C_{gd} is the gate-drain capacitance in MOSFETs. On the other hand, C_C is the coupling capacitance between gate and drain interconnect dangling legs in Fig. 2(c).

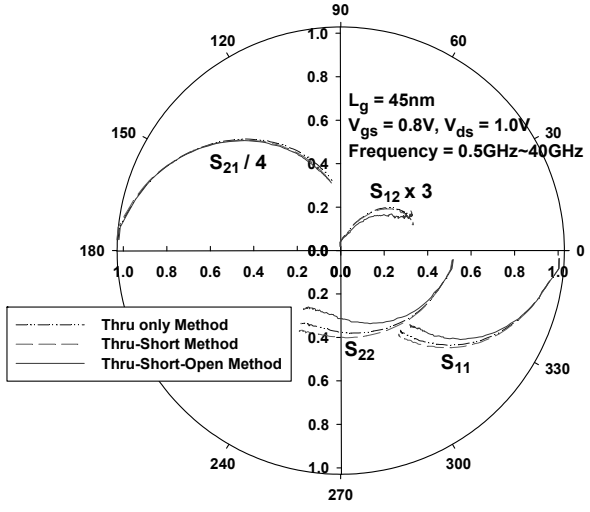
In Table 2, the wide-width effect that f_T decreases at wider W_t is observed. This effect can be explained using the g_m degradation at wider W_t due to the N_f-independent source resistance [10]. The increase of the open de-embedding effect on f_T with decreasing L_g and W_t is owing to the reduction of the gate capacitances (C_{gs}, C_{gd}) in (11). Thus, the new thru-short-open method improves the accuracy in the high frequency range compared to the conventional thru-only and thru-short methods, because the lossy coupling capacitance is eliminated. Fig. 4 shows de-embedded S-parameters of the MOSFETs at L_g = 45 nm and 165 nm in the frequency range up to 40

Table 1. Comparison of the f_T values obtained for devices (W_u = 5 μm, N_f = 10) using three de-embedding methods

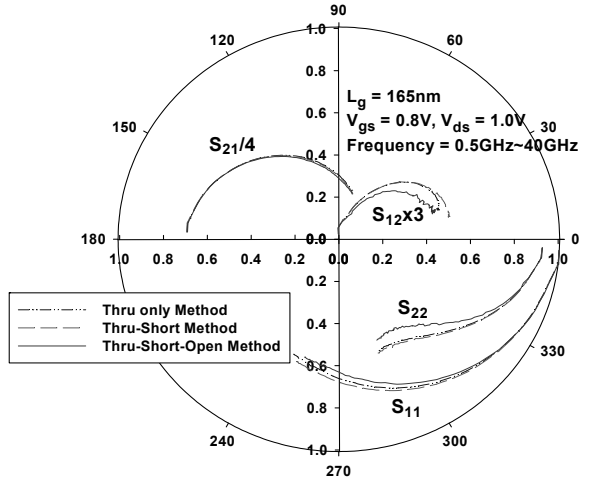
Polysilicon Gate Length (L_g)	f_T, GHz			$\frac{f_T(3)-f_T(2)}{f_T(2)}$ (%)
	Thru only (1)	Thru-Short (2)	Thru-Short-Open (3)	
45 nm	171.5	164.5	180.6	9.8
65 nm	142.3	136.5	148.3	8.6
95 nm	83.8	82.1	86.5	5.4
165 nm	40.1	39.4	41	4.1
215 nm	29.4	29.3	29.4	0.3

Table 2. Comparison of the f_T values obtained for devices (L_g = 45 nm) using three de-embedding methods

W_t=W_u x N_f (μm)		f_T, GHz			$\frac{f_T(3)-f_T(2)}{f_T(2)}$ (%)
W_u (μm)	N_f	Thru only (1)	Thru-Short (2)	Thru-Short-Open (3)	
2.5	20	154.6	148.3	161.1	8.6
2.5	40	148.3	142.3	153	7.5
2.5	60	88.3	84.7	90.1	6.4



(a)



(b)

Fig. 4. Comparison of de-embedded S-parameters at (a) L_g=45 nm, (b) L_g=165 nm.

GHz. The obvious difference between the thru-short and thru-short-open methods is observed in the high-frequency region of the de-embedded S-parameters.

These comparative results indicate that the lossy coupling capacitance between gate and drain interconnection dangling legs plays an important role in the de-embedding process for nano-scale MOSFETs. Therefore, the new thru-short-open method should be used for improving the de-embedding accuracy on nano-scale MOSFETs.

IV. CONCLUSIONS

A new thru-short-open de-embedding method is proposed to eliminate the effect of the lossy coupling capacitance between input and output interconnect dangling legs and its de-embedding effect on f_T with reducing L_g and W_t is compared with those of the conventional thru-only and thru-short methods. As L_g is shortened to 45 nm, it is observed that the effect of the coupling capacitance on f_T after open de-embedding is increased. Thus, the new thru-short-open de-embedding method based on the removal of the coupling admittance is very important to measure on-wafer RF characteristics of nano-scale MOSFETs accurately.

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REFERENCES

[1] M. C. A. M. Koolen, J. A. M. Geelen and M. P. J. G. Versleijen, "An improved de-embedidng technique for on-wafer high-frequency characterization," *in Proc. IEEE Bipolar Circuits Tech. Meet.,* pp.188-191, Sep., 1991.

[2] S. Lee, "Effects of pad and interconnection parasitics on forward transit time in HBTs," *IEEE Trans. Electron Devices*, Vol.46, No.2, pp.275-280, Feb., 1999.

[3] H. Cho and D. Burk, "A three step method for the de-embedding of high frequency S-parameter measurements," *IEEE Trans. Electron Devices*, Vol.38, No.6, pp.1371-1375, June, 1991.

[4] E. P. Vandamme, D. M. M. P. Schreurs and C. V. Dinther, "Improved three-step de-embedding method to accurately account for the influence of pad parasitics in silicon on-wafer RF test-structures," *IEEE Trans. Electron Devices*, Vol.48, No.4, pp.737-742, Apr., 2001.

[5] J. Cha, J. Cha and S. Lee, "Uncertainty analysis of two-step and three-step methods for deembedding on-wafer RF transistor measurements," *IEEE Trans. Electron Devices,* Vol.55, No.8, pp.2195-2201, Aug., 2008.

[6] T. E. Kolding, "On-wafer calibration techniques for giga-hertz CMOS measurements," *in Proc. IEEE Int. Microelectronic Test Structures Conf.*, pp.105-110, Mar., 1999.

[7] J. Song, F. Ling, G. Flynn, W. Blood and E. Demircan, "A de-embedding technique for interconnects," *in Proc. Electrical Perfomance of Electonic Packaging*, pp.129-132, Oct., 2001.

[8] H. Ito and K. Masu, "A simple through-only de-embedding method for on-wafer S-parameter measurements up to 110 GHz," *in IEEE MTT-S Int. Microwave Symposium Digest,* pp.383-386, Jun., 2008.

[9] A. Issaoun, Y. Z. Xiong, J. Shi, J. Brinkhoff and F. Lin, "On the deembedding issue of CMOS multigigahertz measurements," *IEEE Trans. Microwave Theory and Techniques,* Vol.55, No.9, pp.1813-1823, Sep., 2007.

[10] J.-Y. Cha, J.-Y. Cha, and S. Lee, "Scalable BSIM3v3 RF Modeling for CMOS IC Simulation," *in Proc. of International SoC Design Conf.*, pp.529-530, Oct., 2007.

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