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Fluorine Effects on NMOS Characteristics and DRAM Refresh

Deuk-Sung Choi

***Abstract*—We observed that in chemical vapor deposition (CVD) tungsten silicide (WSix) poly gate scheme, the gate oxide thickness decreases as gate length is reduced, and it intensifies the roll-off properties of transistor. This is because the fluorine diffuses laterally from WSix to the gate sidewall oxide in addition to its vertical diffusion to the gate oxide during gate re-oxidation process. When the channel length is very small, the gate oxide thickness is further reduced due to a relative increase of the lateral diffusion than the vertical diffusion. In DRAM cells where the channel length is extremely small, we found the thinned gate oxide is a main cause of poor retention time.**

***Index Terms*—Tungsten silicide, NMOSFET, fluorine, lateral diffusion, DRAM Refresh**

I. INTRODUCTION

The CVD WSix on doped Si (polycide) has been widely used for a gate electrode of CMOS technology because of its low resistivity and good thermal stability. For the commonly used polycide process, fluorine is inadvertently introduced into the gate oxide from WSix deposition using WF_6 gas. The effects of fluorine have been studied intensively such as reliability issues [1-3], device performance [4, 5], and the physical properties of gate oxide [6]. However, few studies have focused on the fluorine effect as the function of the channel length. Lin et al. [7] studied the effect of fluorine incorporation on the transistor channel length using ion implantation after lightly doped drain (LDD) implantation. They improved the short channel effect of transistor by fluorine retarding influence of the phosphorus lateral diffusion.

In this paper, we investigate the fluorine effect on threshold voltage roll-off characteristics of NMOS transistor as a function of the channel length in the CVD WSix polycide scheme. As the channel length of the transistor is decreased, we expect the lateral diffusion of fluorine to gate sidewall is intensified and affects the device characteristics. To compare the fluorine concentration effect, we employed dichlorosilane-based WSix (DCS WSix) and monosilane-based WSix (MS WSix) for low and high fluorine incorporation, respectively. In addition, as a case of the extremely short channel transistor, we examined DRAM refresh characteristics with two different gate materials - WSix polycide that contains fluorine, and W that is fluorine-free.

II. EXPERIMENTS AND DISCUSSION

The devices were fabricated using 80nm DRAM CMOS process [8] with CVD WSix on doped gate polysilicon. After shallow trench isolation formation, CMOS well was formed and followed by a gate module process. The gate oxide was formed with two processes, which are thermal gate oxidation and plasma nitridation for the prevention of boron penetration. The undoped polysilicon gate was deposited and followed by Ph/B implantation for doping and annealing for dopant activation. After both CVD WSix deposition and Hardmask on gate polysilicon, the gate patterning and

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etching were executed and followed by gate re-oxidation at 800 °C. The gate re-oxidation is both the first thermal treatment and the first oxidation process after gate formation. By this process, the sidewall of both of gate polysilicon and WSix film was oxidized. Gate spacer formation and source/drain implantation were processed and followed by RTA annealing for dopant activation at 1000 °C for 20 seconds and metallization process. For the investigation of the fluorine concentration effect, we used DCS and MS WSix for different fluorine concentration. We also used the W gate film for verifying the DRAM refresh characteristics.

Fig. 1 shows the V_{TH} roll-off characteristics of NMOS for the deposition conditions of DCS and MS WSix. Note that the gate oxide thickness and the following processes in both cases are the same except for the WSix deposition split with MS and DCS. When the channel length is 10um, the V_{TH} of MS WSix is higher than that of DCS WSix. Otherwise, the V_{TH}'s of both are very close. The cause of V_{TH} difference by long channel transistors is well-known due to the increase of gate oxide thickness by the fluorine effect, and MS WSix film contains higher fluorine concentration than DCS WSix film.

In our previous work [8], the fluorine concentration has the range of $4 \times 10^{20} \sim 2 \times 10^{21}$ (cm^{-3}) in MS WSix film (The fluorine concentration in depth direction is not uniform.), which is higher by 1.0~2 order than that of DCS film. Converting the concentration to dosage is about the range of $4 \times 10^{15} \sim 2 \times 10^{16}$ (cm^{-2}). As a higher fluorine concentration induces a thicker gate oxide [2], the V_{TH} becomes higher. However, this model cannot be applied to the short channel transistors because the values of V_{TH} are the same. We need an additional model to explain the experimental results.

In order to investigate the short channel behaviour further, we measured the current characteristics of the short channel transistor for both cases. The results show that both have the same current drivability as shown in Fig. 2. This indicates that the gate oxide thicknesses of the two cases could be the same.

To estimate this proposition, we measured the capacitance-equivalent thickness (CET) as the function of gate length by using Miller edge pattern as shown in Fig. 3. In the long channel devices, CET of MS WSix has a higher value and larger variation than that of DCS WSix. The higher fluorine concentration is responsible for the higher oxide thickness as discussed earlier. This is a result of an actual increase in oxide thickness but not a change in the oxide dielectric constant. It has been proposed that fluorine catalyzes the movement of excess

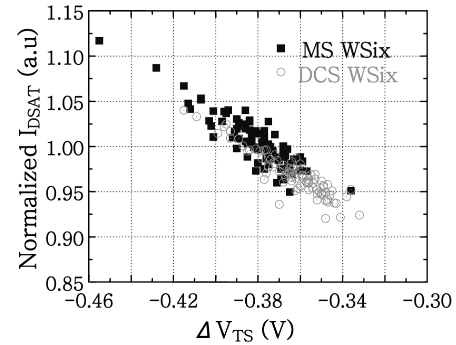

Fig. 2. Threshold voltage vs saturation current (@VDD=1.6 V) as the function of WSix deposition condition.

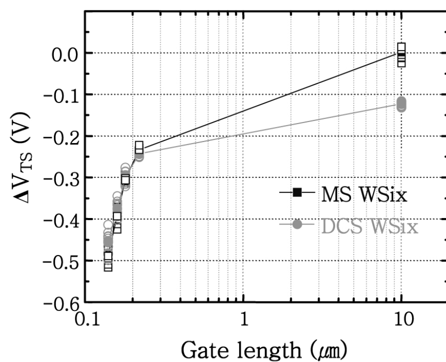

Fig. 1. NMOS threshold voltage roll-off characteristics as the function of WSix deposition condition.

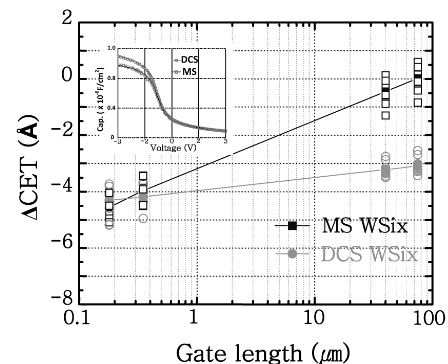

Fig. 3. NMOS CET vs gate length as the function of WSix deposition condition. ΔCET means the CET difference between long channel transistor and short channel transistor.

oxygen in the dielectric bulk, which then reacts at the interface and increases the oxide thickness [6]. In contrary to long channel devices, the short channel devices make no differences in CET between MS WSix and DCS WSix. In fact, we find the CET of MS WSix has been drastically decreased about 4.5 Å as the channel length is reduced from 75 um to 0.18 um. Based on these results, we propose a model to explain the channel length dependency for MS WSix film. As the channel length is reduced, the amount of fluorine in the oxide decreases, therefore gate oxide thickness also decreases. By the post thermal treatment, such as gate re-oxidation at 800 ^{o}C, the fluorine in WSix film diffused vertically to gate oxide and laterally to polysilicon/oxide interface as shown in the inserted cross-sectional diagram of transistor of Fig. 4. The net fluorine concentration, which is responsible for the increase of the gate oxide thickness, decreased due to the lateral out-diffusion of fluorine. As the channel length is decreased, this effect is amplified because the distance of lateral fluorine out-diffusion is shorter and the lateral polysilicon/oxide interface is an important source of fluorine file-up as shown in Fig. 4.

Thus, the above results demonstrate that the lateral fluorine diffusion to gate edge is the main root cause of the reduction of gate oxide thickness in the short channel devices. The phenomenon is more prominent in the MS WSix, which contained greater concentration of fluorine. To evaluate this model, we have examined the TEM images for gate oxide thickness of MS WSix as the function of gate length as shown in Fig. 5. We find that the gate oxide thickness of long channel device is larger by about 6 Å than that of short channel device. The

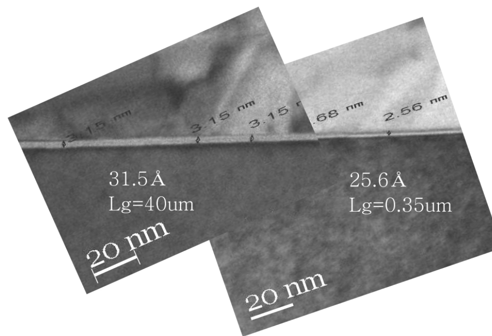

Fig. 5. TEM image of gate oxide thickness for 40 μm/0.35 μm channel length in the MS WSix condition.

physical thickness measured by TEM images is equivalent to the electrical thickness measured by capacitance. The result is the evidence to support the Wright's model [6], which is an actual increase in oxide thickness.

In DRAM, cell transistor is formed by NMOS transistor with extremely short channel and we can apply the above results to DRAM cell transistor. The gate oxide thickness of DRAM cell transistor is to be also decreased below designed thickness. So, the thinner gate oxide thickness induces the large electric field near the drain junction and DRAM's retention characteristic is decreased. To verify the hypothesis, we studied the retention time of DRAM cell by a function of relative CET measured at peripheral region as shown in Fig. 6. Relative CET means the CET difference between long channel transistor and short channel transistor.

The experiment is executed in three groups: (i) MS WSix gate film, (ii) W gate film for reference 1 (same

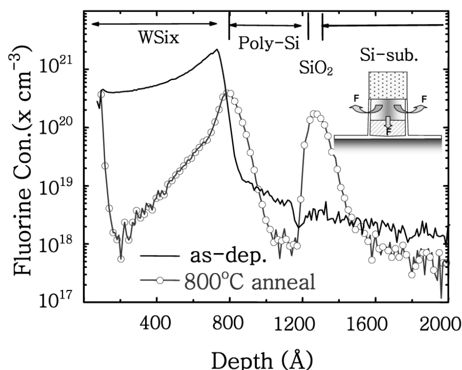

Fig. 4. Vertical SIMS profile of fluorine concentration before/ after gate re-oxidation at 800 ^{o}C in the MS WSix/Poly-Si/Si-Sub layers.

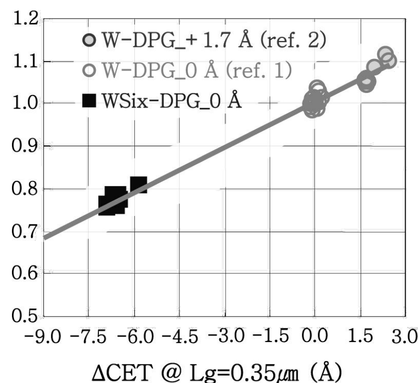

Fig. 6. Normalized DRAM Retention time vs relative CET. Relative CET means the CET difference between long channel transistor and short channel transistor.

thickness of gate oxidation as group 1) and (iii) W gate film for reference 2 (1.7 Å higher thickness of gate oxidation than group 1). W film has the many problems such as higher resistivity, conformability and abnormal high gate oxide leakage. In our previous work [8], we had improved these problems. The W gate module process has to adopt the diffusion barrier such as Ti/WN or WSix/WN for preventing the diffusion of excess Si which is the cause of conformability. The relatively high resistivity of W gate is due to increase of the interfacial resistance between W and poly-Si. Ti/WN diffusion barrier is more suitable for the W-DPG application, but the tungsten film deposited on Ti/WN barrier shows a higher electrical resistivity than that of WSix/WN barrier. We had developed low resistive CVD W process with B_2H_6-based nucleation layer. Amorphous or metastable beta-phase tungsten nucleation layer can cause large grain growth of tungsten. It is lead to low resistive W. Because W gate film does not contain fluorine, there is no effect on increasing gate oxide thickness. In the case of using the W gate film, the gate oxide thickness of transistor is the same for both large and short channel lengths. As shown in Fig. 6, the MS WSix film has a poorer retention time (about 23% decrease) than that of reference 1 with W film due to thinner gate oxide and the elevated electric field in drain junction of cell transistor. Thus, the above results demonstrate that the DRAM retention characteristic with MS W Six film is seriously affected by fluorine out-diffusion to lateral direction of channel length. In the viewpoint of process design, gate oxide thickness is very important parameter at both peripheral transistor and DRAM cell transistor with extremely short channel length. However, fluorine effect induces different gate oxide thicknesses for those transistors due to different channel length. To overcome this problem, we need to design the process parameter carefully or also use W gate film as the gate material.

III. Conclusions

We have analyzed the fluorine effect on gate oxide thickness for varying the channel length in NMOS transistor. As the channel length is decreased, the amount of fluorine out-diffusion to lateral direction of gate in the fluorine-rich film increases and the gate oxide thickness decreases. The effects have been verified by experiments. The phenomenon is caused by post thermal treatment such as poly oxidation. The mechanism is also applied to DRAM retention characteristics with extremely short channel length transistor and the cause of poor retention time is due to reducing the gate oxide thickness and increasing the electric field of channel edge. The method to overcome the problem is to design process carefully and use W gate film.

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