A Clock Regenerator using Two 2nd Order Sigma-Delta Modulators for Wide Range of Dividing Ratio

Seung-Wuk Oh*, Sang-Ho Kim, Sang-Soon Im*, Yong-Sung Ahn**, and Jin-Ku Kang***

Abstract—**This paper presents a clock regenerator using two 2nd order Σ-Δ (sigma-delta) modulators for wide range of dividing ratio as defined in HDMI standard. The proposed circuit adopts a fractional-N frequency synthesis architecture for PLL-based clock regeneration. By converting the integer and decimal part of the N and CTS values in HDMI format and processing separately at two different Σ-Δ modulators, the proposed circuit covers a very wide range of the dividing ratio as HDMI standard. The circuit is fabricated using 0.18 μm CMOS and shows 13 mW power consumption with an on-chip loop filter implementation.**

Index Terms— **High-Definition Multimedia Interface (HDMI), Transition Minimized Differential Signaling (TMDS), Cycle Time Stamp (CTS), Sigma-Delta Modulator (SDM), Multi-Modulus Divider (MMD), audio clock regenerator, phase locked loop (PLL)**

I. INTRODUCTION

High-Definition Multimedia Interface (HDMI) is one of high-speed digital multimedia interface standards to transmit and receive video and audio data with a high quality [1]. In HDMI, when transmitting the data, the audio clock is not transmitted separately. Therefore the audio clock should be recovered in the receiver side from TMDS clock (video data timing clock) coming from the transmitter. HDMI recommended seven different audio sampling clocks, which are 32 KHz, 44.4 KHz, 88.2 KHz, 176.4 KHz, 48 KHz, 96 KHz, and 192 KHz. Frequency range between 25.2 MHz to 148.5 MHz is used for TMDS clocks. With various combinations with TMDS clock frequency, N (Dividing ratio of video clock to TMDS clock), and Cycle Time Stamp (CTS), the recommended sampling audio clocks are generated. Since the output is 128*fs, the final output frequency varies from 4.096 MHz to 24.576 MHz.

In HDMI system, the source device transmits N and CTS to the sink device with TMDS clock in order to regenerate the audio clock. By using received N and CTS values, the clock regenerator of the sink device regenerates the audio clock. Therefore, the sink device requires 2 dividers receiving N and CTS. However, in HDMI specifications, the range of N (4096 ~ 46592: 16-bit)) and CTS (25200 ~ 421875 : 19-bit) value is very wide for various device applications. In order to cover very wide range of the N and CTS values, conventional integer-N type PLL design approaches consume a large chip area. And its locking time is higher due to a narrow loop bandwidth limited by a low frequency input clock to the PLL. Therefore, the difficulty in the design of the audio clock regeneration in HDMI is to cover this wide range of dividing values.

This paper proposes an architecture that regenerates clock covering a very wide range of dividing ratio [2, 3]. In the proposed approach the dividing values of N and CTS are separated in to integer part and fractional part, and the integer parts are provided to a MMD (Multi-Modulus Divider) block and the fractional parts are provided to two different 2nd Σ-Δ modulators. The proposed architecture can reduce the dividing range of

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MMD by the maximum of 6 bits and still covers whole range of the dividing ratio. Section II describes the proposed architecture, and circuit design is given in section III. Measured results are presented in section IV followed by the conclusion.

II. PROPOSED ARCHITECTURE

1. Conventional Atchitecture

Fig. 1 shows a conventional structure (integer-N type frequency synthesis) of an audio clock regenerator in HDMI. The output is represented as 128*fs with an audio sampling clock (fs) times 128. At the source device, first, the audio clock (128*fs) is divided by N, then CTS value is decided by counting the TMDS clock in one period of (128*fs)/N clock. The TMDS clock, N, and CTS are transmitted to the sink device for the clock generation. Then the sink device regenerates the clock through the PLL (Phase-Locked Loop) with N and CTS. The relationship between the output clock (128*fs) and TMDS clock is given in Eq. (1) :

$$128 * \mathrm{fs} = (\mathrm{f_{TMDS}} * \mathrm{N}) / \mathrm{CTS} \qquad (1).$$

In a conventional approach, in order to satisfy a very wide dividing range of dividing values, the circuit blocks for the dividers become larger. Besides, since the reference clock ($\mathrm{f_{TMDS}} / \mathrm{CTS} = 1$ KHz) to the PLL loop is low, the loop bandwidth of the PLL is also reduced. As a result the locking time is increased. A very narrow loop bandwidth means large values of R and C in loop filter are required, which makes it difficult to integrate on a single chip [4, 5].

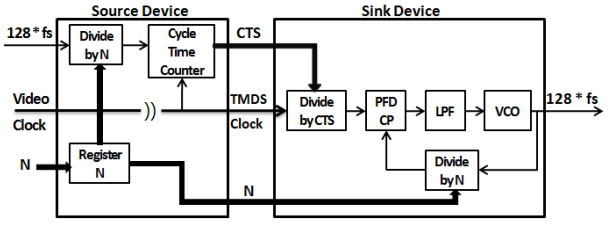


Fig. 1. The block diagram of a conventional audio clock regenerator in HDMI.

2. The Proposed Architecture

This paper proposes a circuit to regenerate the audio clock using a fractional-N PLL structure. The proposed circuit uses two 2^{nd} order Σ-Δ modulators for proper dividing of the TDMS clock from the source. We chose a fractional-N type frequency synthesis design approach. In order to do that, the N and CTS values are separated into integer and fractional parts and the integer value (*k*) are provided to the MMD and the fractional values are provided to the 2^{nd} Σ-Δ modulator. This means each dividing block is converted to a fractional-N divider with Σ-Δ modulator.

In order to facilitate the design procedure with the proposed scheme, the whole range of the N and CTS values are converted to an integer and fractional part by dividing them with 2^{10} and 2^{13}, respectively. Table 1 shows that the range of N and CTS for HDMI specification and $N/2^{10}$ and $CTS/2^{13}$ values. The reason why N is divided by 2^{10} is to utilize the 2^{nd} Σ-Δ modulator more efficiently. Since the dividing variation of the MMD is *k-1, k, k+1, k+2*, the *k* value should be more than 3 [6]. If N is divided by 2^{11} instead of 2^{10}, the minimum value of *k* becomes 2. This means dividing by 1 occurs in the MMD, which is not allowed in the fractional-N frequency synthesis. For this reason, N is divided by 2^{10} and CTS is divided by 2^{13}, respectively.

Table 1. The range of N and CTS value in HDMI specification and their binary values separated into integer part (k) and fractional parts by dividing 2^{10} (10 digits fractional) and 2^{13} (13 digits fractional), respectively

N value	MMD Integer Input (k)	SDM Fractional Input	CTS value	MMD Integer Input (k)	SDM Fractional Input
4096	100 (4)	0000000000	25200	11 (3)	0001001110000
4576	100 (4)	0111100000	27000	11 (3)	0100101111000
5824	101 (5)	1011000000	27027	11 (3)	0100110010011
6144	110 (6)	0000000000	28000	11 (3)	0110101100000
6272	110 (6)	0010000000	28125	11 (3)	0110111011101
6864	110 (6)	1011010000	30000	11 (3)	1010100110000
7007	110 (6)	1101011111	30030	11 (3)	1010101001110
8918	1000 (8)	1011010110	31250	11 (3)	1101000010010
11648	1011 (11)	0110000000	54000	110 (6)	1001011110000
12288	1100 (12)	0000000000	54054	110 (6)	1001100100110
12544	1100 (12)	0100000000	60000	111 (7)	0101001100000
13728	1101 (13)	0110100000	60060	111 (7)	0101001100000
14014	1101 (13)	1010111110	74250	1001 (9)	0001000001000
17836	10001 (17)	0110101100	82500	1010 (10)	0001001000100
23296	10110 (22)	1100000000	140625	10001 (15)	0010101010000
24576	11000 (24)	0000000000	148500	10010 (18)	0010000010000
27456	11010 (26)	1101000000	165000	10100 (20)	0010010001000
35672	100010 (34)	1101011000	210937	11001 (25)	1011111111000
46592	101101 (45)	1000000000	210938	11001 (25)	1011111111000
			234375	11100 (28)	1001110000000
			421875	110011 (51)	0111111110000

Thus, we can separate the N and CTS values into integer and fractional parts. As a result, the maximum 6 binary digits of integer part (k) are provided to the MMD, and fractional bits (10 bits for N and 13 bits for CTS, respectively) are for the 2nd Σ-Δ modulator's input. Using this approach N can be reduced from 4096 ~ 46592 (decimal) to 4 ~ 45 (decimal, binary 6 bits), and CTS from 25200 ~ 421875 (decimal) to 3 ~ 51 (decimal, binary 6 bits). Therefore the circuit architecture can be simplified while covering very wide range of dividing values.

Based on the proposed scheme two different circuit design approaches can be devised. The first one is a fractional-N PLL using an off-chip loop filter and the second one is using an on-chip loop filter. If the proposed scheme is implemented with an off-chip loop filter, the frequency resolution is could be higher with a large capacitor. Fig. 2 shows the structure of the audio clock regenerator with an off-chip loop filter. The divider design for covering the very wide dividing ratio can be simplified as Table 1. In HDMI specification, the reference clock to PFD is made by dividing the TMDS clock by the CTS value. The reference clock rate to PFD is fixed at 1 KHz with a combination of CTS value and TMDS clock rate. Since this reference clock is very low, the loop bandwidth of PLL must be set below 100 Hz. Therefore very large capacitor is needed in the loop filter and it takes a long time to lock.

As explained before, the integer part (MSB 6bits) of CTS value is provided to the fractional divider (MMD) and fractional part (LSB 13 bits) is provided to the 2nd order Σ-Δ modulator. The final output (128*fs) can be derived from Eq. (2), which is the same as Eq. (1). It represents the operation of the clock generator given in Fig. 2.

$$128 * \mathrm{fs} = \mathrm{f_{TMDS}} * \left(\frac{\mathrm{N}}{2^{10}} * 2^{10}\right) * \frac{1}{\left(\frac{\mathrm{CTS}}{2^{13}} * 2^{13}\right)} \qquad (2).$$

In order to realize the proposed scheme with on-chip implementation, the other architecture is devised as shown in Fig. 3. Fig. 3 presents the proposed audio clock regenerator with an on-chip loop filter implementation. The proposed structure increases the loop bandwidth by 2^{10} times and the values of R and C in the loop filter can be reduced. Thus R-C values in the loop filter are realizable on a chip, and the locking time is also reduced. The circuit takes an increased reference clock frequency to the PFD by 2^{10} by dividing the output of the MMD in the first Σ-Δ modulator by 2^3 instead 2^{13}. Therefore the clock frequency to PFD is increased to 1.024 MHz. The CTS and N dividers operate as a fraction-N type divider, so the whole loop operates with a fractional-N type PLL. As the reference clock to PFD increases, an accuracy of output frequency resolution could be degraded because the fraction dividing process is executed from the inflated input frequency to PFD compared to the off-chip filter solution. The locking time is inversely proportional to the loop bandwidth, represented as Eq. (3)

$$T_L = \frac{-\ln\left(\frac{w_{tol}}{\Delta w}\right)}{w_c} \qquad (3)$$

where Δw is the frequency step, w_n is the natural frequency, ξ is the damping factor, w_c is the loop bandwidth, and w_{tol} corresponds to the maxim um tolerance of the frequency at which the PLL is considered to be locked. As shown, the lock time is

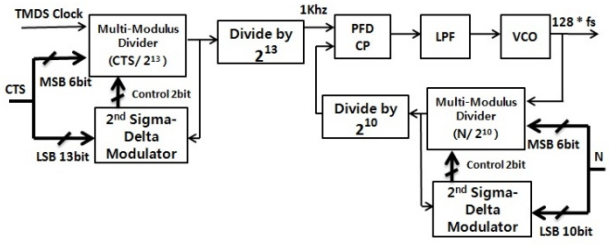


Fig. 2. The block diagram of proposed audio clock generator with an off-chip loop filter implementation.

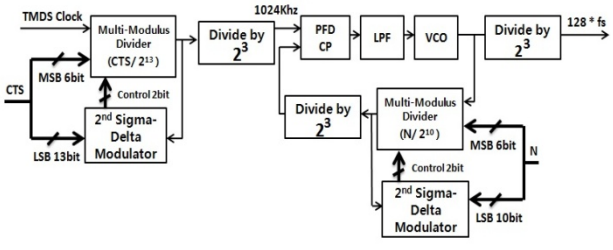


Fig. 3. The block diagram of proposed audio clock regenerator with an on-chip loop filter implementation.

largely determined by the loop bandwidth, w_c . Thus the loop bandwidth of the circuit with on-chip loop filter is 1,024 (2^{10}) times larger than that with off-chip loop filter. Therefore, the lock time of the on-chip can be reduced compared to the off-chip loop filter approach.

Eq. (4) represents the output of the proposed clock generator with the on-chip loop filter, in which the final output frequency is the same as Eq. (1)

$$128 * fs = f_{TMDS} * (\frac{N}{2^{10}} * 2^3) * \frac{1}{(\frac{CTS}{2^{13}} * 2^3)} * \frac{1}{2^3} \quad (4)$$

III. CIRCUIT DESIGN

While the sigma-delta modulators play the key role in realizing the audio clock generator, design of a fractional-N PLL circuit is another task. In this section, we describe circuit components for the proposed audio clock generator. Additional circuit design technique to reduce spurious tones by dithering is also applied in the fractional-N PLL design, such as in reference [7]. In this work a 3rd order loop filter was used.

1. 2nd order Σ-Δ Modulator

In this paper, a fractional-N PLL with Σ-Δ modulator is used for frequency synthesis. Using Σ-Δ modulators, the number of control bits can be reduced while the quantization noise is pushed into the high frequency band [8]. There is a trade-off between the order and the stability of the Σ-Δ modulator. In this work the MASH (multi-stage noise shaping) type Σ-Δ modulator is used to keep the stability regardless of the order. Fig. 4 shows the block diagram of the 2nd order MASH 1-1 sigma-delta modulator used in the proposed clock generator. It is formed by cascading two 1st order sigma-delta modulators. When the input value of Σ-Δ modulator is constant, the MASH Σ-Δ modulator generates periodical sequence of output, which generates spurs on spectr um [7, 9]. A max-sequence length dithering method to the Σ-Δ modulator is added for reducing the spurs [7].

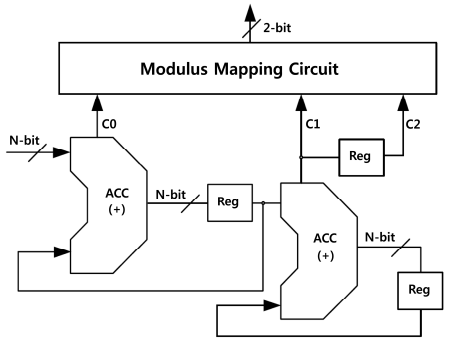


Fig. 4. Structure of the 2nd order MASH 1-1 Σ-Δ modulator.

2. PLL Components

The VCO has a tuning range from 10 MHz to 250 MHz. Since the final output (128*fs) is obtained by dividing the VCO output by 8, the final output frequency is from 1.25 MHz to 31.25 MHz. Since the desired final output should be placed between 4.096 MHz to 24.576 MHz, the VCO covers the operating range. Fig. 5(a) shows the schematic of the VCO which consists of a 4-stage ring oscillator. The replica bias circuit can adjust Vbn dynamically by its own negative feedback loop to compensate the PVT variation. The self-biased technique can provide a wide frequency range and minimized supply/substrate noise. The delay cell of the VCO shown in Fig. 5(b) is a source-coupled pair with symmetric active loads for the better linearity of the VCO gain and wider swing [10]. Fig. 6 shows the simulated VCO

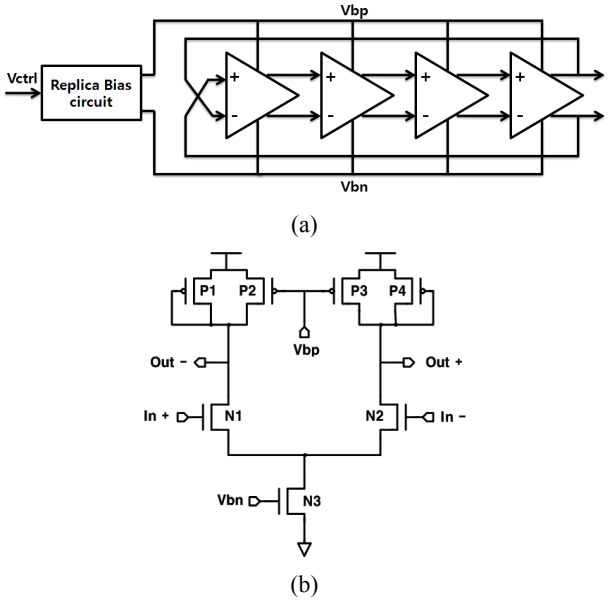


Fig. 5. (a) Block diagram of the Voltage Controlled Oscillator and (b) Its delay cell.

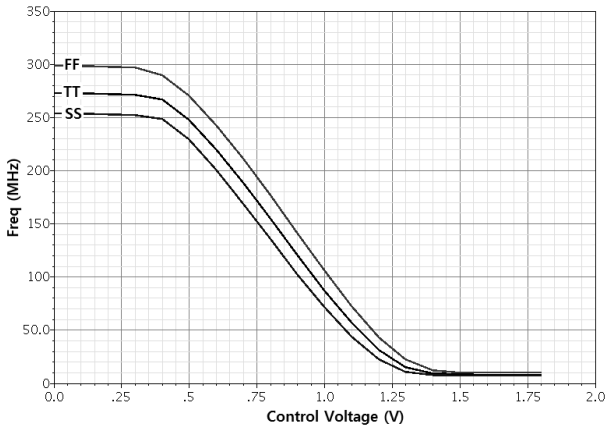


Fig. 6. Simulated VCO frequency vs Vctrl voltage.

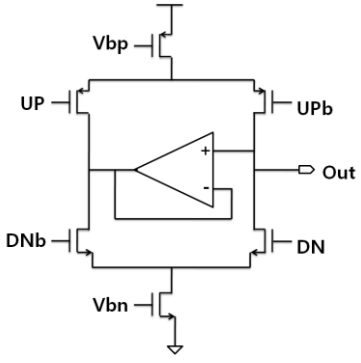


Fig. 7. Charge pump schematic.

frequency as a function of the control voltage (Vctrl). The VCO circuit covers the operating frequency range under all process corners (FF, TT, SS) between 0.4 V and 1.3 V of the control voltage.

Fig. 7 shows the schematic of the charge pump with current steering switches and unity gain buffer. The unity-gain buffer is used to clamp the terminal voltages of current sources during the zero-current pumping period. In this way, voltage glitches on the loop filter due to charge sharing can be eliminated [11, 12]. Both the up and the down current can be either connected to the output or drained to a dummy reference voltage by the four switches. The relative timing of the charge pump switches is optimized to avoid glitches at the output node.

The LPF used in audio clock regenerator is a third order on-chip filter, as shown in Fig. 8. The values of LPF are determined by the loop bandwidth, VCO gain, PFD reference clock, charge pump current, phase margin and effective dividing factor. The loop bandwidth is set about 100 KHz and the damping factor is about 0.9. The design parameters for the on-chip loop filter are as

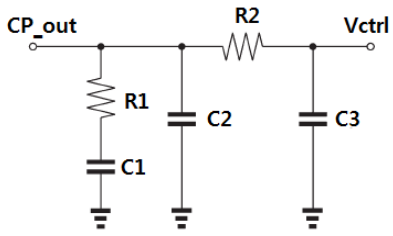


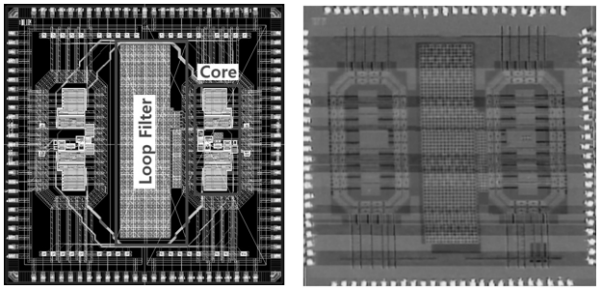
Fig. 8. Loop filter schematic.

follows: C1=703 pF; C2=33 pF; C3=3.3 pF; R1=15 kΩ; R2=143 kΩ.

IV. MEASUREMENT RESULTS

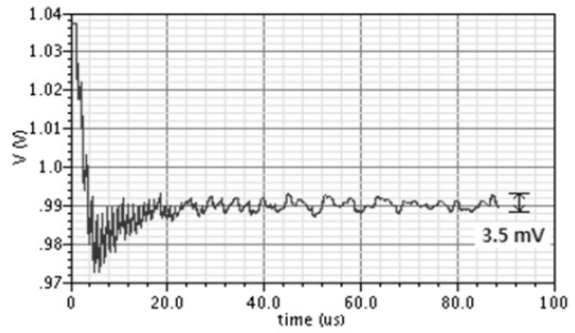
The proposed circuit has been designed and fabricated using 0.18 μm CMOS technology. Fig. 9 shows the layout and chip photo of the proposed audio clock regenerator with an on-chip loop filter. The input values for test are chosen as specified in specification. In our simulation example, TMDS clock, N and CTS value are 54 MHz, 12544 and 60000, respectively. Then the VCO output is 90.32 MHz and the generated audio clock frequency is 11.2896 MHz. The control voltage presents about variation of 3.5 mV changes is locked at 0.99 V of the VCO control voltage as shown in Fig. 8. Fig. 10(a) shows the simulated VCO output when locked at 90.32 MHz (That is 8 times of 11.2896 MHz). Simulations show the maximum peak-to-peak variation of the output frequency after lock is about 150 KHz locked at 90.32 MHz, which is about 0.17% of the recovered clock.

Fig. 11 shows the measured phase noise at 24.576 MHz. The measured phase noise is -80.21 dBc/HZ@1 KHz, -79.50 dBc/Hz@10 KHz, -78.86 dBc/Hz@100 KHz and -102.77 dBc/Hz@1 MHz, respectively. Fig.12 shows the measured output signals (128*fs) at 4.096 MHz,

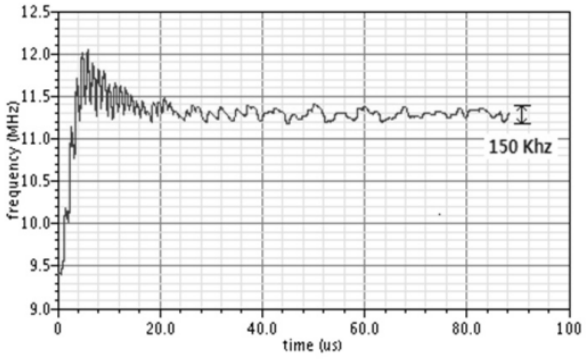


(a) (b)

Fig. 9. (a) Layout, (b) Chip photo.



(a)



(b)

Fig. 10. Simulated results on the circuit with an on-chip filter (a) VCO control voltage and (b) Final output at 11.29 MHz.

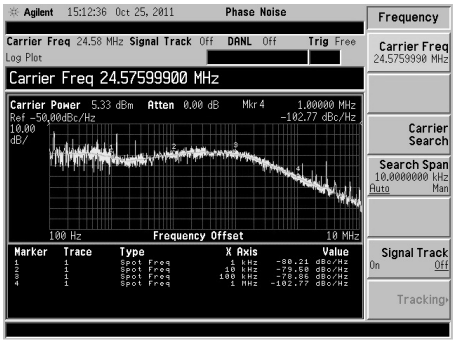
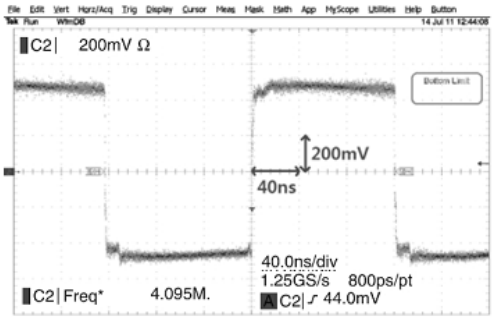


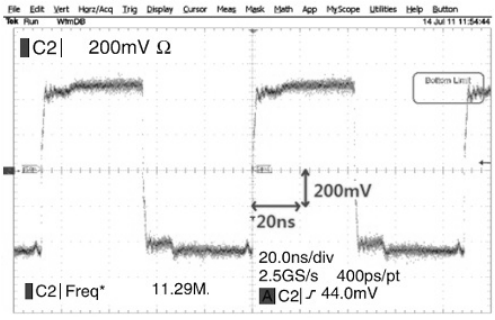
Fig. 11. Measured output phase noise at 24.576 MHz.

Table 2. Performance summary

Technology	0.18 μm CMOS
Supply voltage	1.8 V
Power consumption	13 mW
Chip area(core)	0.5 mm^2
Dividing Ratio Range	4096 ~ 46592 (N) 25200 ~ 421875(CTS)
Loop BW	100 KHz
Output clock range	2.5 MHz ~ 62.5 MHz
Phase noise (@ 24.576MHz clock)	-80.21 dBc/HZ@1 KHz -79.50 dBc/Hz@10 KHz -78.86 dBc/Hz@100 KHz -102.77 dBc/Hz@1 MHz



(a)



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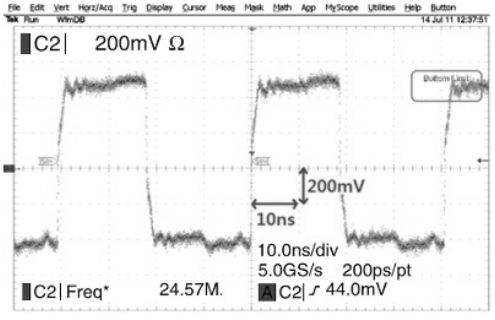

(c)

Fig. 12. Measured output signals (128*fs) of (a) 4.096 MHz, (b) 11.2896 MHz, (c) 24.576 MHz and frequency spectrum.

11.2896 MHz, and 24.576 MHz, respectively. Table 2 s ummarizes the measurement result of the circuit.

V. CONCLUSIONS

This paper presents a clock regenerator using two 2nd order sigma-delta modulators for covering wide range of dividing ratio as defined in HDMI. The proposed circuit adopts a fractional-N frequency synthesis for PLL-based clock regeneration using two Σ-Δ modulators. By converting the integer and decimal part of the N and CTS values in HDMI format and processing separately at two different Σ-Δ modulators, the proposed structure covers a

very wide range of the dividing ratio. The circuit is fabricated using 0.18 μm CMOS and shows 13 mW power consumption with an on-chip loop filter

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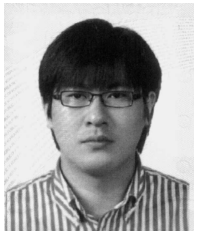

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