A 10-b 500 MS/s CMOS Folding A/D Converter with a Hybrid Calibration and a Novel Digital Error Correction Logic

Joongwon Jun, Daeyun Kim, and Minkyu Song

Abstract—**A 10-b 500 MS/s A/D converter (ADC) with a hybrid calibration and error correction logic is described. The ADC employs a single-channel cascaded folding-interpolating architecture whose folding rate (FR) is 25 and interpolation rate (IR) is 8. To overcome the disadvantage of an offset error, we propose a hybrid self-calibration circuit at the open-loop amplifier. Further, a novel prevision digital error correction logic (DCL) for the folding ADC is also proposed. The ADC prototype using a 130 nm 1P6M CMOS has a DNL of ±0.8 LSB and an INL of ±1.0 LSB. The measured SNDR is 52.34-dB and SFDR is 62.04-dBc when the input frequency is 78.15 MHz at 500 MS/s conversion rate. The SNDR of the ADC is 7-dB higher than the same circuit without the proposed calibration. The effective chip area is 1.55 mm^2, and the power dissipates 300 mW including peripheral circuits, at a 1.2/1.5 V power supply.**

Index Terms—**Analog digital converter, folding, interpolation, digital correction logic, calibration**

I. INTRODUCTION

The demand for analog-to-digital converters (ADCs) to convert natural analog signals into mechanical digital codes is rapidly increasing due to the development of CMOS technology and the improvement of digital appliances. In addition, the application of ADCs is being extended to the area of communications such as mobile appliances and wideband modems; the area of image signal processing such as HDTVs, camcorders, and set-top boxes; the area of medical appliances such as MRI, CT, and wireless endoscopy; the area of computer science such as voice recognition, and video graphic processors; and etc. Among them, an ADC beyond 10-b resolution and a 500 MS/s conversion rate is needed in the field of digital testing equipment like digital oscilloscopes; in the field of communication systems such as wideband 4G, LTE-Advanced, and software defined radio(SDR) [1]. To satisfy the new requirements, ADC architectures such as SAR, pipelining, and multi-step are now widely used [2, 3]. Fig. 1 shows the popular ADC architectures. For high resolution ADC, the pipelining scheme is the best choice. However, the conversion rate is poor, compared to the other architectures. In contrast, the flash architecture has the highest conversion rate, although it has poor resolution (e.g. 6-bit).

Recently, in order to raise the conversion rate to the giga-Hz, multi-channel ADC with time interleaving scheme has been studied [1, 4]. Since the time interleaving architecture has a few ADC cores in parallel, the conversion rate can be improved. However, the chip area and power consumption increase in proportion to the number of ADC cores. Therefore, the time interleaving architecture cannot be the best candidate for next generation communication system chips because of the requirement for a huge chip area and high power consumption. Instead of time interleaving architecture, a

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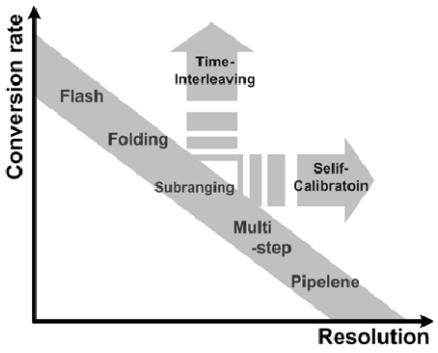

Fig. 1. Conceptual representation of resolution vs. conversion rate (Nyquist rate ADC).

folding architecture with 10-bits resolution and a 500 MS/s conversion rate has been developed [5-8]. Normally, it is difficult to implement high resolution ADC beyond 10-bits with folding architecture, because the folding architecture encounters many problems such as a narrow band input frequency, large offset errors at the folding amplifiers, and asynchronous delay between the coarse block and the fine block. Some researchers have published to overcome these drawbacks [9-13]. In this paper, we propose a 10-b 500 MS/s folding ADC with new techniques. The folding scheme satisfies the high performance specifications of LTE-advanced and SDR with low power consumption and a small chip area. The paper is organized as follows. In section II, the block diagram and circuit diagrams of the proposed ADC are described. Hybrid calibration and a prevision error correction logic is discussed in section III. Our measurement results and our conclusions are described in section IV and V, respectively.

II. ARCHITECTURE

Fig. 2 shows the architecture of the proposed 10-bit ADC. It is composed of an analog input block, an analog signal pre-processing block, a 4-bit coarse flash ADC block, a 6-bit fine cascaded folding ADC block, a digital processing block with a prevision error correction circuit, and a hybrid offset self calibration block.

In general, when we design a folding ADC, the most important issue is the determination of folding factors such as the folding rate (FR), interpolation rate (IR), and number of folding block (NFB). Based on the folding factors, we select the analog input bandwidth, conversion rate, power consumption, and chip area. Table 1 shows the folding factors, according to the architecture schemes. Normally, 3+7 (3-bit coarse block and 7-bit fine block) or 4+6 schemes are used when designing a 10-b folding ADC. In the 3+7 scheme, the analog input bandwidth is wide, because of a low FR. However, there are many offset errors at the preamplifier block, since it must handle 128 parallel signals at the fine 7-bit ADC.

Thus, the power consumption and the chip area are large. In the 4+6 scheme, the analog bandwidth is narrower than that of 3+7, because FR is 25. However, the problem can be solved with a mixed track-and-hold amplifier(THA) and a cascaded folding architecture [12].

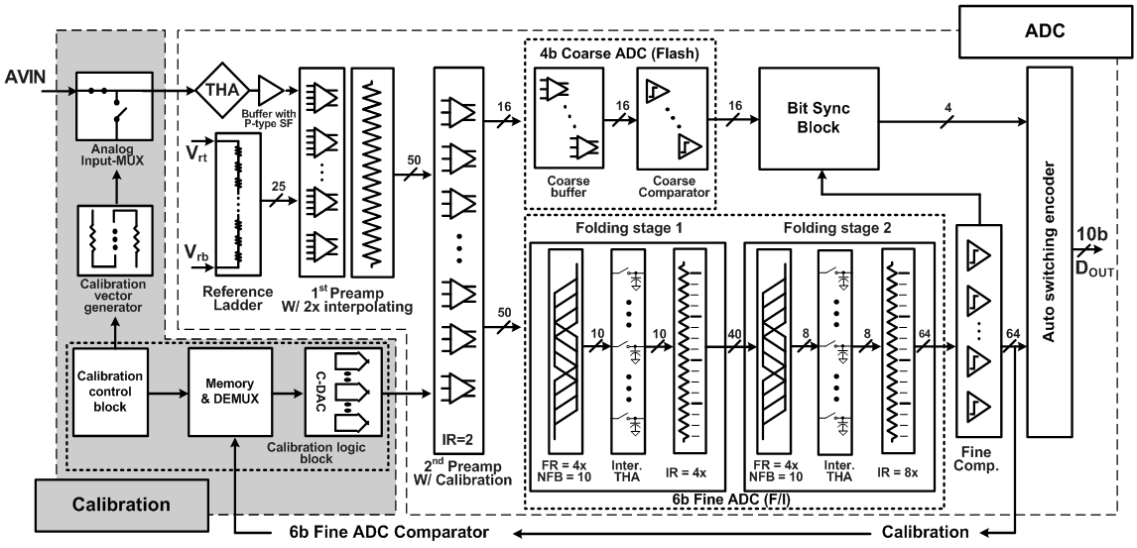

Fig. 2. Block diagram of proposed 10-b F/I ADC.

Table 1. Folding-Interpolating factors of the 10b ADCs

Architecture	1st preamp	1st FR	1st IR	2nd FR	2nd IR	No. of Comparator
3+7	36ea	3	4	3	8	8+128 =136ea
3+7	48ea	3	3	3	8	8+128 =136ea
4+6 (Proposed)	50ea	5	4	5	8	16+64 =80ea
4+6	80ea	5	4	3	4	16+64 =80ea

In this paper, we propose a 4+6 scheme, hybrid calibration and a prevision error correction logic to satisfy a small chip area and a high conversion rate. We now explain the operation of proposed circuits.

III. CIRCUIT DESCRIPTION

1. Analog Input Block

Fig. 3 shows a circuit diagram for the analog input block. The block is composed of a THA and a source follower to drive the preamplifiers. In order to satisfy the 10-bit resolution, the input stage must have at least 70-dBc SFDR [7]. Thus a gain bootstrapping technique to keep the linearity of the THA, and a super source follower with a low total harmonic distortion (THD), are adopted [1, 8]. Since the super source follower has an input trans-conductance value beyond 75 mS, a wide input bandwidth of 100 MHz is obtained in spite of the large 3.5 pF output load. The input range is 0~850 mV. The simulated SFDR of the input stage is about 75-dBc

2. Cascaded Folding-Interpolation

In the 4+6 scheme, since the coarse ADC has a 4-bit resolution, the fine 6-bit ADC must handle 25 folding signals. In this case, however, the gain of folding amplifiers decreases. This is because the bandwidth of the pre-amplifier has a limitation and the long metal bus lines among folding amplifiers cause huge parasitic capacitances [5]. To solve these problems, a cascade technique to distribute the high FR is proposed. As shown in Fig. 2, the first stage of the folding-interpolation block is composed of FR=5, NFB=10, and IR=4. The second stage of the folding-interpolation block is composed of FR=5, NFB=8, and IR=8. To overcome the high FR, a new folding amplifier is proposed. Fig. 4 shows the circuit diagram of the folding amplifies which is composed of a folded cascade output stage, an intermediate THA, and a level shifter. The folded cascade output stage increases the voltage gain of the folding amplifier, decreases the degradation of parasitic capacitances caused by large folding bus lines, and reduces the kickback noise of a switch at the intermediate THA. The role of an intermediate THA is improving the settling time of the folding amplifier. The role of level shifter, namely, the source follower, is determining the DC level of the second folding amplifiers or the DC level of the comparators. It is important to design an optimized level shifter, since the output impedance of the folding amplifier must be carefully determined using Eq. (1) [5].

$$R_L = \frac{1}{2\pi \cdot BW \cdot C_L} \tag{1}$$

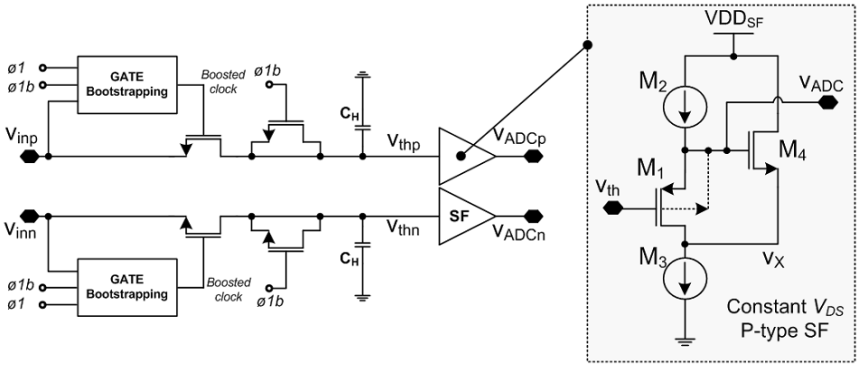

Fig. 3. ADC input stage with a THA and a super SF.

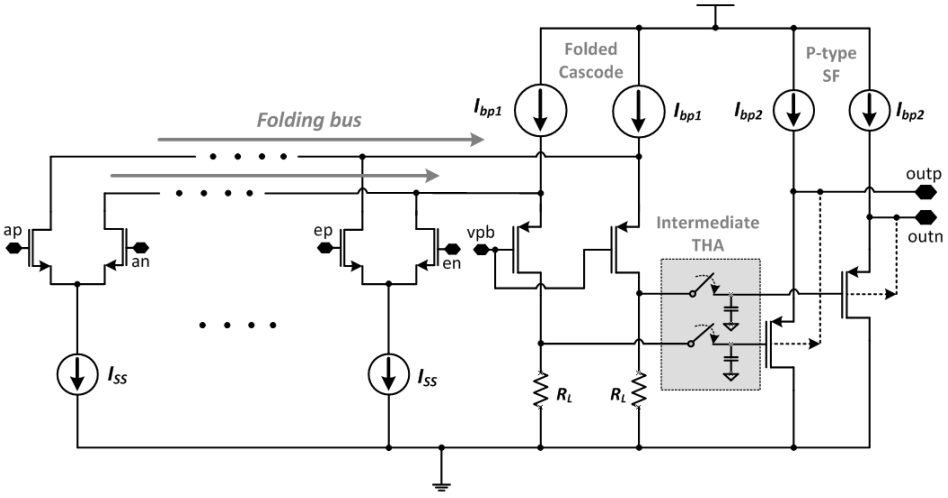

Fig. 4. Folding amplifier with a folded-cascade output stage, an intermediate THA, and a level-shifter (FR=5).

In Eq. (1), R_L means the output impedance of the folding amplifier, BW is the bandwidth of the folding amplifier, and C_L is the total output load capacitances of the folding amplifier. To extend bandwidth, the output impedance must be small. Therefore, a source follower with a very low output impedance is designed.

3. Sequential Settling by THA

The settled DC level signals at the first stage THA may have mismatching errors or disappear in the worst case at the comparator block, after the end of multistage analog signal processing in the fine 6-bit cascaded folding interpolation ADC. Thus, the settling time of amplifiers is one of the major problems in the design of the ADC, and it is a major problem to generate a missing code at the block of comparators. To solve those problems, a technique that uses a preset switch at the output stage of analog amplifiers has been studied [9, 10]. However, due to the preset switch, the output impedance of the amplifiers has a large variation. In this paper, we propose a multiple stage THA with a multiple phase clock. Fig. 5 shows the circuit diagram of the proposed technique. It consists of an input THA, two intermediate THAs, and multiple phase clocks(THA: ϕ1-3, comparator: ϕ3b). Based on this technique, a stable settling time can be obtained without a change of output impedance. Further, the operating speed is improved, because the settling time of the amplifiers is much faster.

4. Hybrid Calibration Technique

In general, it is difficult to implement a folding ADC beyond 10-b resolution without calibrations. Hence, we propose a hybrid calibration that has an analog calibration technique and a digital calibration technique such as Fig. 6.

At first, the DC level input signal of ADC is stored at input MUX and THA with a calibration vector generator. Then, the offset error from multiple pre-amplifiers is transported to an input of a calibration comparator. The

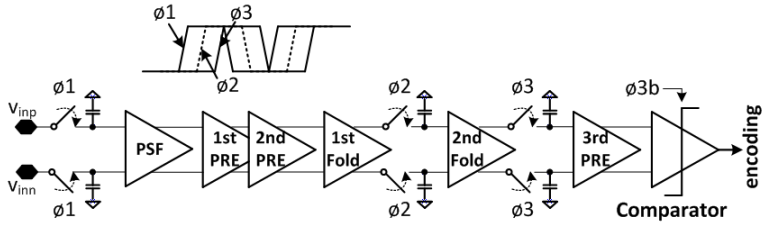

Fig. 5. Sequential settling by input THA and intermediate THA.

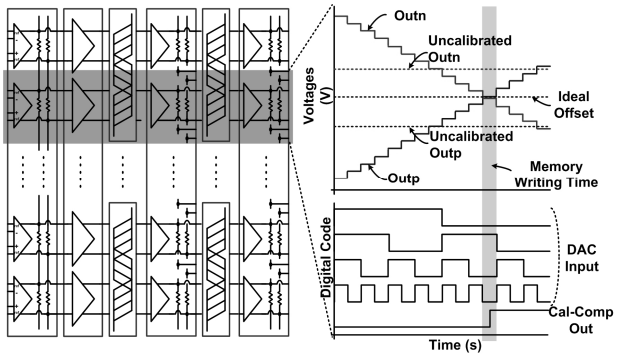

Fig. 6. The proposed hybrid calibration technique.

other input of the calibration comparator comes from a calibration 4-bit current DAC. In case of the DAC, the switching condition of the current DAC is selected by the digital codes stored in the memory block, according to the digital output of the main ADC. Finally, the output offset voltage of the folding block can be reduced, since the current of the second pre-amplifier is controlled by the current DAC. This procedure is repeated until the desired calibration is obtained. The number of iterations is determined by the calibration control block. After completing all of the calibrations, the ADC automatically begins normal operation. With the proposed calibration technique, we can reduce the offset errors substantially. Therefore, this approach is called hybrid calibration, since there are an analog calibration such as 4-bit DAC and a digital calibration such as calibration memory.

Fig. 7 shows the setting procedure of the calibration vector generator. The zero-crossing of the analog block is determined by the pre-amplifier block, and the input signal of the pre-amplifier is different as shown Fig. 7(a).

Thus, the appropriate detection signals should be configured to the respective inputs of the pre-amplifiers. To generate an appropriate detection signal, a calibration vector generator is proposed. Fig. 7(b) shows the calibration vector generator, which is composed of a resistance ladder. The desired detection signal is transferred to the 6-bit fine ADC throughout MUX.

Fig. 8 shows the algorithm flow chart of the proposed hybrid calibration and a Monte-Carlo simulation of offset error range using the number of iterations. Fig. 8(a) shows a flow chart of the hybrid calibration. It is similar to an iterative self-calibration with an analog technique and a digital technique. As shown in Fig. 8(b) the error range has a maximum of ±81 mV without calibration

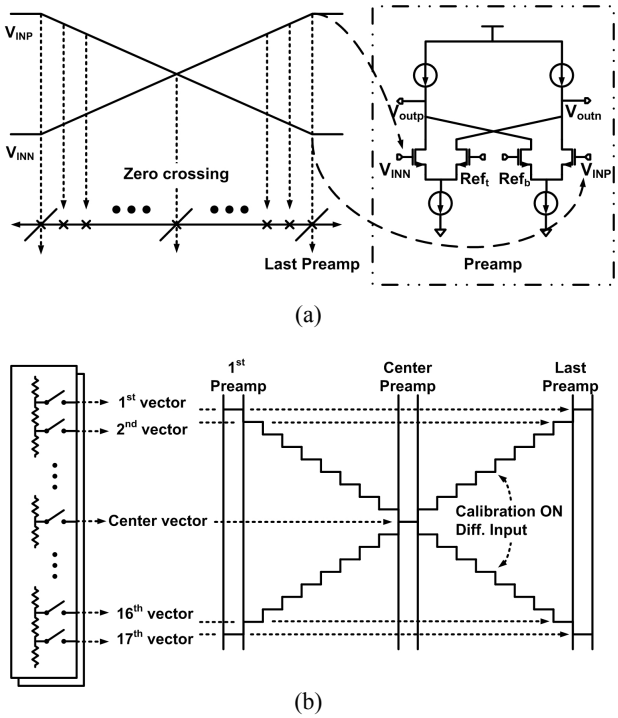

Fig. 7. Setting of the calibration vector (a) Diff input signal as preamp, (b) Calibration vector generator.

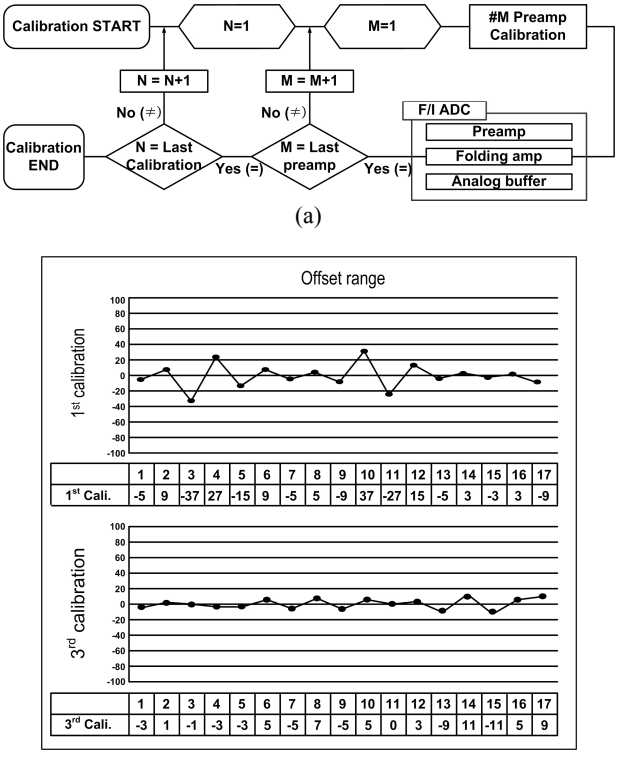

Fig. 8. Hybrid calibration (a) Algorithm of the iterative self-calibration, (b) Offset error variation by the number of iterations.

circuits. However, it is about ±37 mV with a first iterative calibration. After three iterations, the offset error range is reduced by ±11 mV. In the proposed ADC, we repeat the iterative hybrid self-calibration until a sufficient 10-bit resolution is obtained. Normally, the desired resolution is obtained, after 6 or 7 iterations.

5. New Prevision Error Correction Logic

The F/I ADCs have significant error between the coarse ADC and the fine ADC, since there are time differences and offset errors. Fig. 9 shows the reason for the missing code error between the coarse ADC and the fine ADC. Since the coarse ADC is 4-bit and the fine ADC is 6-bit, the zero-crossing time of the coarse ADC is normally faster than that of the fine ADC. Thus a time difference and a delay occur as shown in Fig. 9(a). Finally, the digital output code has a missing code as shown in Fig. 9(b). To solve this problem, a new prevision error correction logic is proposed. Fig. 10 shows the block diagram of the proposed error correction logic. The logic calibrates the error of the first fine binary code with the superposition of the last coarse binary code and the first fine thermometer code. With the combination of codes, uncorrected fine binary codes are corrected. To control the corrected signal, as well as the first fine binary code is drives the switch block, the last coarse binary code and the fine thermometer code are nested in the XOR-gate to determine the error of the fine ADC codes. At this time, if an error occurs, the output is replaced by corrected signals. Otherwise the original fine binary codes are passed throughout the digital error correction block. Therefore, the proposed prevision error correction logic ensures stable performance of the high speed folding ADC.

IV. Measurement Results

The prototype ADC was fabricated using a Samsung 130 nm 1P6M CMOS process, and it occupied 1.55 mm^2 of effective area as shown in Fig. 11. (ADC core : 1.05 mm^2, Calibration Block : 0.5 mm^2) The chip was tested at a 500 MS/s conversion rate. However, to measure the high speed parallel digital code, a decimation scheme was used at the ADC output buffer. The decimation block reduced the frequency of the output digital code from

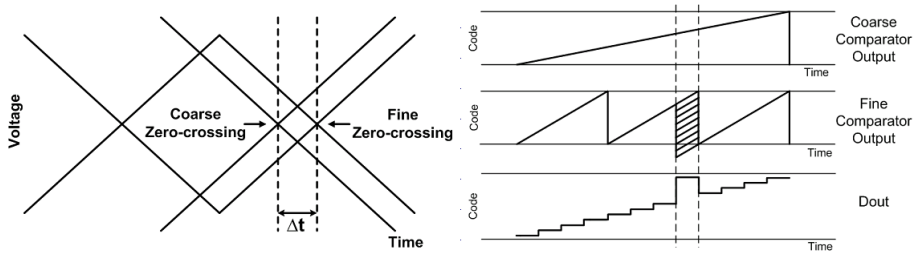

Fig. 9. Missing codes error (a) Fine and coarse comparator input signal, (b) Digital output signal.

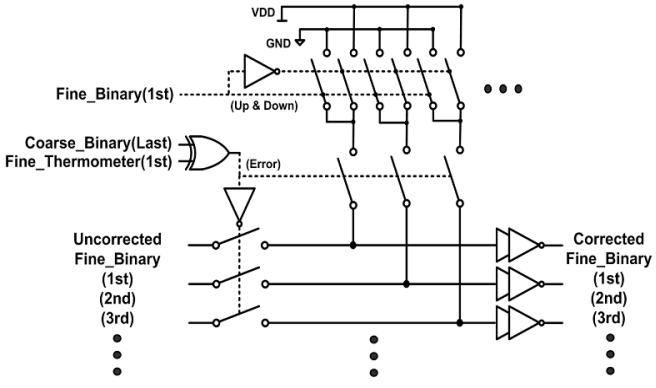

Fig. 10. A new prevision error correction logic.

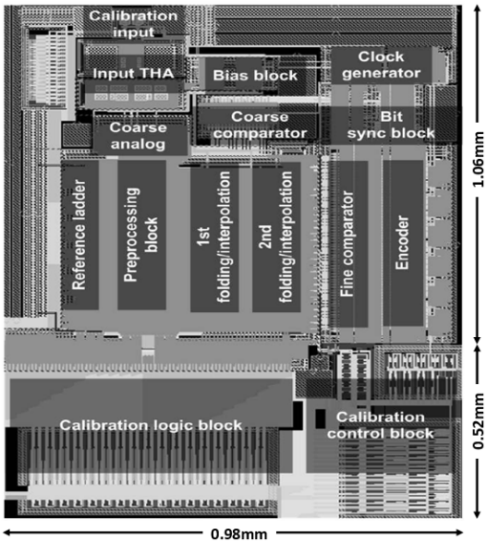

Fig. 11. Die photo for the prototype ADC.

500 MHz to 62.5 MHz.

Fig. 12 shows the measured results for differential nonlinearity (DNL) and integral nonlinearity (INL) with a 5.0659 MHz sinusoidal input. From Fig. 12(a), the maximum DNL and INL with the proposed hybrid calibration are +0.8/-0.6 LSB and +1.00/-0.8 LSB, respectively. The DNL and INL without calibration are typically + 1.5/-0.7 LSB and +4/-3.5 LSB, respectively. Fig. 13 shows the SNDR and SFDR performance versus

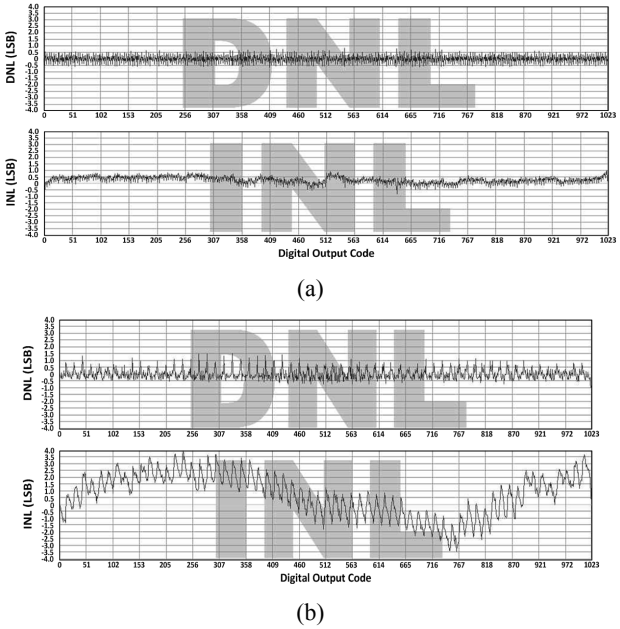

Fig. 12. Measured DNL & INL (a) With calibration (b) Without calibration.

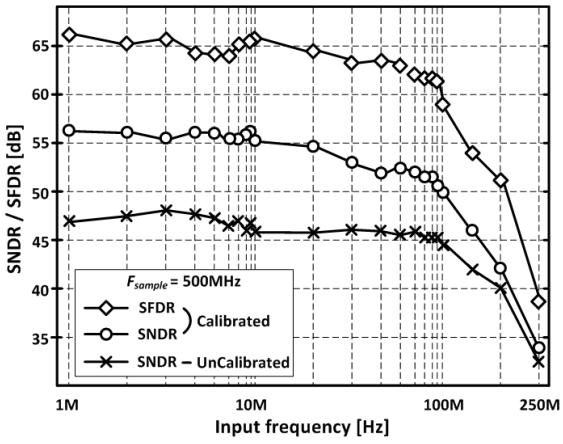

Fig. 13. Measured SNDR and SFDR versus input frequency at 500 MS/s.

analog input frequency at 500 MS/s. The SNDR and SFDR kept the low frequency value beyond 50-dB and 62-dBc up to 90 MHz, respectively. However, the performance rapidly degraded at an input frequency of 100 MHz.

This performance degradation at high input frequency can be estimated due to the poor clock jitter. Table 2 shows a measured performance summary at 500 MS/s with and without the calibration circuit.

Table 2. Performance Summary at 500 MS/s for Calibrated VS. UnCalibrated

	Calibrated	UnCalibrated
Resolution	10 bits	
Sampling Rate	500 MSample/s	
SNDR @ F_{IN} = 78.15 MHz	52.34 dB	45.12 dB
SFDR @ F_{IN} = 78.15 MHz	62.04 dBc (HD3)	55.08 dBc (HD2)
Max. INL	+1.00 / -0.8 LSB	+4 / -3.5 LSB
Max. DNL	+0.8 / -0.6 LSB	+ 1.5 / -0.7 LSB
Jitter @ F_S = 500 MHz	4p-sec rms	
Input Range	±400 mV differential	
Power Supply	1.5 V (Input stage) / 1.2 V (ADC & Calibration)	
Power Dissipation	300 mW (ADC W/ Peripheral Circuits)	
Figure of Merit *	FoM1 = 1.77p, FoM2 = 5.68p[J/conv.-step]	
Active Die area	1.55 mm^2 (ADC : 1.05 mm^2, Calibration : 0.5 mm^2)	
Process	Samsung 130 nm 1P6M N-well CMOS	

* : $FoM1 = \frac{Power\ Diss.}{2^{ENOB} \times F_{sampling}}$, $FoM2 = \frac{Power\ Diss.}{2^{ENOB} \times 2 \times ERBW}$

V. CONCLUSIONS

A 10-bit 500 MS/s CMOS cascaded folding ADC with hybrid calibration was designed, fabricated and completely measured. The prototype ADC with the proposed scheme was implemented using a 130 nm 1P6M CMOS process. A single-channel folding-interpolating ADC was composed of an analog input network, a pre-processing block, a 4-bit coarse ADC, and a 6-bit fine ADC. The folding amplifier with the folded cascade output stage was proposed for the block of the folding bus, to improve the bandwidth limitation and voltage gain by parasitic capacitances. To overcome the disadvantage of a high folding rate, at the fine ADC, a cascaded folding-interpolating technique was used. Furthermore, to extend the folding ADC resolution, we propose a hybrid calibration circuit with an analog calibration technique and a digital calibration technique. New prevision digital error correction logic was also proposed to reduce the digital error codes. The fabricated chip occupied 1.55 mm^2 and the power dissipated was 300 mW including peripheral circuits at the 1.2/1.5 V power supply. The measured results of DNL and INL were within 1.0 LSB and 0.8 LSB at 10-bit resolution, respectively. The SNDR was 52.34-dB and SFDR was 62.04-dBc when the input frequency was 78.15 MHz at a sampling frequency of 500 MS/s. The SNDR was approximately 7-dB higher compared to the same circuit without a calibration. Therefore, the proposed hybrid calibration and the prevision error correction logic were proved to be very complementary techniques that enhance the performance of ADC.

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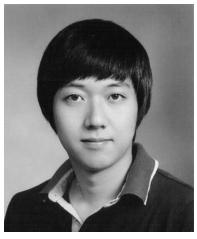

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