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Common Mode Voltage Cancellation in a Buck-Type Active Front-End Rectifier Topology

Mohd Junaidi Abdul Aziz†, Christian Klumpner*, and Jon Clare*

†Power Electronics and Drive Research Group, Faculty of Electrical Eng., Universiti Teknologi Malaysia, Johor, Malaysia

*Power Electronics, Machine and Control Group, The University of Nottingham, Nottingham, United Kingdom

Abstract

AC/AC power conversion is widely used to feed AC loads with a variable voltage and/or a variable frequency from a constant voltage constant frequency power grid or to connect critical loads to an unreliable power supply while delivering a very balanced and accurate sinusoidal voltage system of constant amplitude and frequency. The load specifications will clearly impose the requirements for the inverter stage of the power converter, while wider ranges of choices are available for the rectifier. This paper investigates the utilization of a buck-type current source rectifier as the active front-end stage of an AC/AC converter for applications that require an adjustable DC-link voltage as well as elimination of the low-frequency common mode voltage. The proposed solution is to utilize a combination of two or more zero current vectors in the Space Vector Modulation (SVM) technique for Current Sources Rectifiers (CSR).

Key words: Buck rectifier, Common mode voltage elimination, Space vector modulation

I. INTRODUCTION

The standard topologies for AC/AC power converters used in applications where sinusoidal input current and sinusoidal output voltage are required are shown in Fig. 1. They consist of a two-level back-to-back Voltage Source Inverter (VSI) topology plus the necessary input and output filters, where the rectifier stage is a boost type, as shown in Fig. 1a or 1b, depending on the load requirements: three or four wire loads with or without grounding of the neutral potential. This topology has been proven to have very good performance in [1]-[8]. However, it experiences higher switching losses which further increase with a decrease in the voltage transfer ratio (especially below 0.8) due to the fact that switching losses tend to stay constant.

In this situation, a buck-type rectifier [3], [8]-[11], which is illustrated in Fig. 2, seems a logical choice. However, when a topology equivalent to the one shown in Fig. 1(b) is desired, a few negative aspects have to be taken into account. First, it is not possible to use a third-order harmonic injection or standard Space Vector Modulation (SVM) to increase the voltage transfer ratio of the rectifier to its theoretical limit of 0.866 because large zero-sequence 3rd order current harmonics will appear due to the low impedance of the input

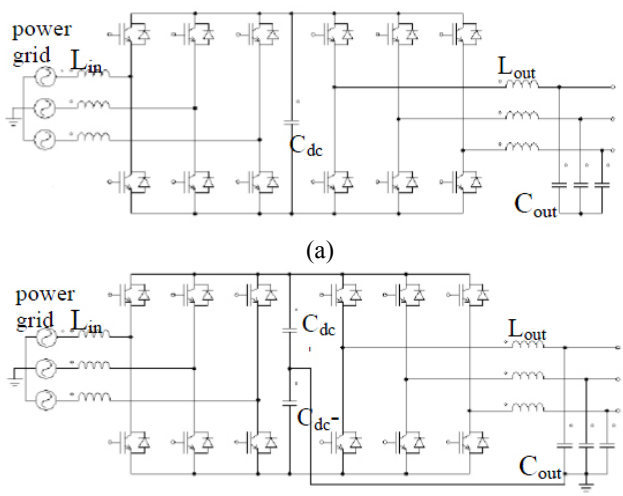

Fig. 1. Back-to-back Voltage Source Converter topologies with output filters for; (a) 3-phase/3-wire applications. (b) 3-phase/4-wire applications.

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†Corresponding Author: junaidi@fke.utm.my
Tel: +607-5535357, Fax: +607-5566272, Universiti Teknologi Malaysia
*Power Electronics, Machine and Control Group, The University of Nottingham, United Kingdom

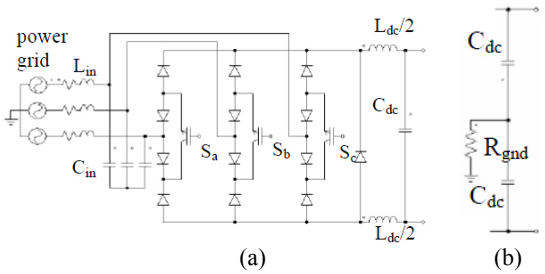

Fig. 2. The topology of a three-phase buck rectifier using 3-IGBTs (a) 3-wire (b) 4-wire.

filters that correspond to low frequency (3rd order) harmonics. Common mode chokes to limit the circulation of third-order common mode current, which is supposed to cause the most trouble due to the smallest reactance of the filter inductance, or other means for the injection of third order common-mode voltage are possible but not feasible.

This paper proposes a combination of two zero current vectors in the Space Vector Modulation (SVM) technique for three-switch current source buck rectifiers in order to cancel the low frequency (especially the 3rd order) common mode voltage present in the dc-link [12]-[15]. This converter operates in an open loop where the DC link current is not controlled.

This paper is organized as follows. The Space Vector Modulation (SVM) method for Current Source Rectifiers (CSR) is introduced in Section II. The simulation results of the three-switch current source buck rectifier and the generation of common mode voltage in the rectifier are presented and discussed in Section III. The proposed solution to reduce it is explained in Section IV. The simulation and hardware results for the proposed solution are illustrated and discussed in Section V. Some conclusions are given in Section VI.

II. Space Vector Modulation for a Current Source Rectifier

In general, the SVM strategy features full control of the frequency, amplitude and phase angle of the output voltage/current and the controllable displacement phase angle of the input line current for a back to back AC/AC converter. However, for a current source rectifier, the amplitude of the output voltage and the displacement phase angle of the input line current are vital quantities to be controlled [11]-[15]. This can be accomplished by utilizing a combination of the two adjacent active current vectors and a zero current vector to synthesize a reference vector for the variable amplitude and angle. The proportion between the duty-cycles of the two adjacent vectors gives the direction and the duty-cycle of the zero-vector determines the magnitude of the reference vector. Fig. 3 shows the reference input current vector of the rectification stage and the sectors delimited by the six active current vectors, in which a CSR has the same direction as the

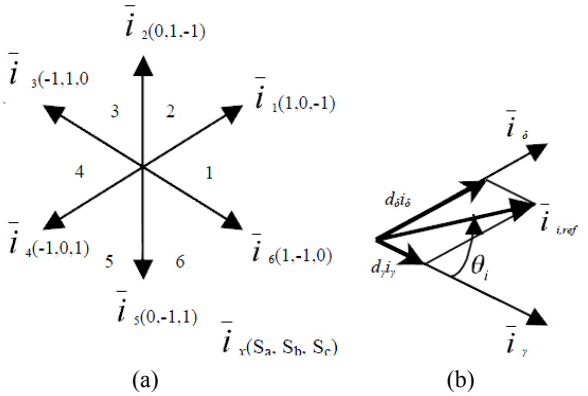

Fig 3. Generation of the reference current vector in a current source type rectifier. (a) The six active current vectors. (b) The reference current vector within the current sector.

line-to-line space vectors. The duty-cycles of the two active switching vectors I_γ and I_δ used to synthesize the reference current vector are given by:

$$d_\gamma = m_i \sin(\pi/3 - \theta_i) \qquad d_\delta = m_i \sin\theta_i$$
$$\text{and} \quad d_0 = 1 - d_\delta - d_\gamma \tag{1}$$

where m_i is the modulation rectifier index and θ_i is the angle within the sector of the reference input current vector.

These duty-cycles are multiplied with the switching period in order to determine the ON-times of the buck rectifier switches. A zero current vector is normally produced by the disconnection of one of the rectifier switches, which causes the freewheeling diode to connect the two DC-side terminals in order to provide a current path for the inductor currents.

The average voltage in the DC-link is calculated by knowing the active switching states duty-cycles and the corresponding line-to-line voltages:

$$V_{PN\text{-}avrg} = d_\gamma \cdot V_{line\text{-}\gamma} + d_\delta \cdot V_{line\text{-}\delta} \tag{2}$$

In can be seen that when $\theta_i = \pi/6$, $d_\gamma = d_\delta = 0.5$ and the two line-to-line voltages are equal to their peak value multiplied by $\cos(\pi/6)$, the average voltage over a switching period delivered by the rectifier stage reaches a minimum of 0.867 of the peak line-to-line voltage.

III. Simulation of a Three-Switch Buck Rectifier

A simulation model of a 5 kW three-switch buck rectifier that corresponds to the topology shown in Fig. 3 has been implemented in Saber® simulator.

A. Switching Sequence for a Three-Switch Buck Rectifier

High system efficiency of a three-switch buck rectifier can be achieved by employing the switching pattern proposed in [8], which results in minimum switching losses. There, within a $\pi/3$-wide interval of the mains period, the power transistor of the bridge leg that corresponds to phase *i,* where *i=a,b,c,* which has the lowest absolute value of the input phase

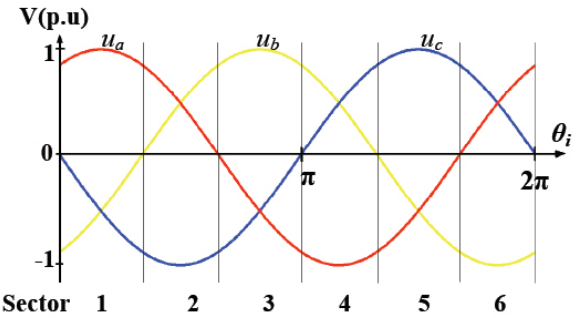

Fig 4. Mains phase voltages and interval being defined by different relations of the instantaneous main phase voltage.

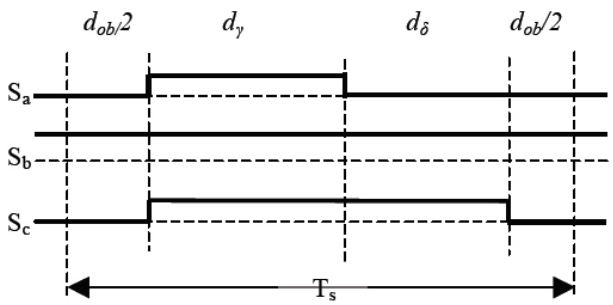

Fig 5. Switching state sequence of the three-switch buck rectifier with minimum switching losses.

voltage is continuously gated to the corresponding DC-link terminal. Considering, for example, the angle interval $\pi/3 < \theta_i < \pi/2$ in Fig. 4, the main phase voltage u_b meets the criteria $|u_b| < \{|u_a|; |u_c|\}$. Therefore the power transistor S_b is continuously turned-ON within this interval.

In order to achieve minimum switching losses, a specific sequence of the switching states has to be implemented. This sequence consists of three different switching states, two active switching states and one free-wheeling state, which are arranged symmetrically as depicted in Fig 5.

B. Simulation Results of a Three-switch/three-wire Buck Rectifier

This simulation is based upon ideal switches, ideal diodes with a 0.7 V voltage drop during the conduction state, an ideal supply and a resistive load. The value of the input filter, L_{in} is 1.9mH parallel with a 22Ω resistor per-phase and C_{in} is 6.8uF per-phase. Meanwhile at the output side, the value of L_{dc} is 6mH and C_{dc} is 0.04mF. The supply frequency is 50Hz and a $230V_{rms}$ phase voltage while the load is 50 Ω. Fig 6 shows the input and output voltages and currents of the rectifier when operating at m_i = 0.85 and a 2.7kW output power.

The quality of the input current for all three phases, I_a, I_b and I_c shown in the Fig. 6(a) is excellent where a sinusoidal current shape with an amplitude of ~5.7 A_{pk} are obtained. As depicted in Fig 6(b), only low frequency components are

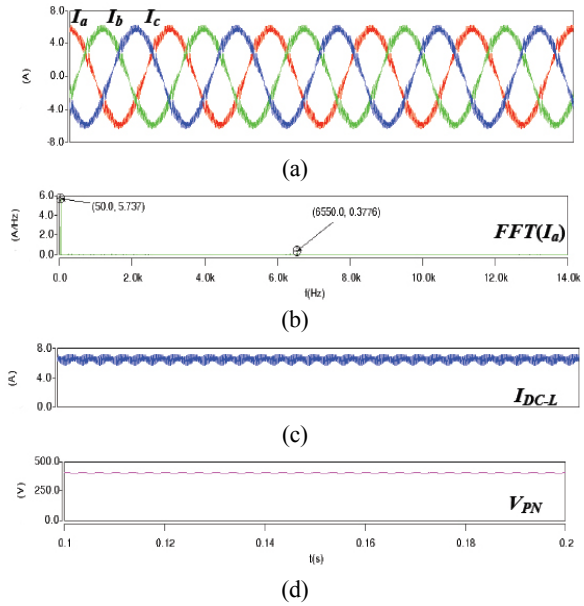

Fig. 6. Three-switch buck rectifier input line currents (a), FFT of *Ia* (b), rectifier output inductor current (c) and dc output voltage (d) for reference output voltage = 412 V_{dc} operating with the minimum switching losses switching state sequences.

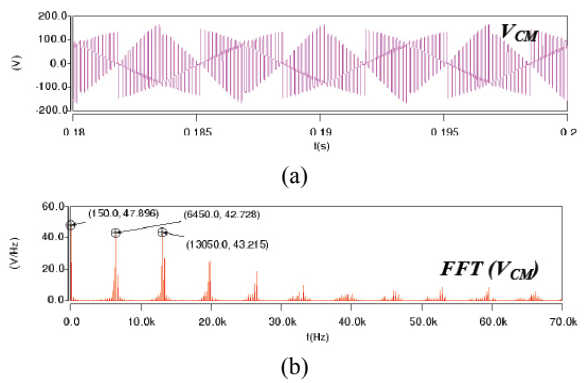

Fig. 7. (a) Common mode voltage generated by buck rectifier and (b) its corresponding FFT for reference output voltage = 412Vdc operating with the minimum switching losses switching state sequences.

allowed to pass through it while high frequency components, such as ~0.38 @ 6.6 kHz are suppressed, which verifies the function of the low pass input filter. The dc choke current I_{DC-L} and the output dc voltage V_{PN}, are presented in the Fig. 6(c) and Fig. 6(d) respectively. It can be seen that a 6 A_{pk} dc choke current with a 1.5 A_{pk-pk} ripple and smooth ~ 412 V_{dc} output voltages are obtained.

The common mode voltage generated by a three-switch buck rectifier and its FFT are shown in Fig. 7(a) and 7(b) respectively. It can be seen that the large amplitude of the third order common mode voltage ~47.9 V_{pk} is generated by the buck rectifier. From a high frequency point of view, ~42.7 V_{pk} @ 6.45 kHz and ~43.2 V_{pk} @ 13.05 kHz are where the

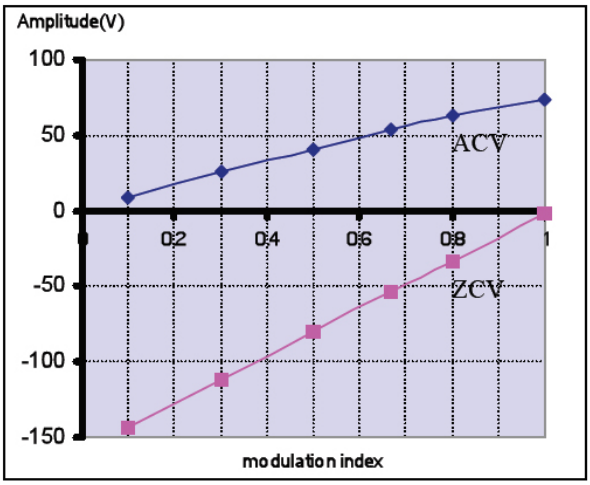

Fig. 8. Relationship between the modulation index and the amplitude of the third order common mode voltage generated by the ACV and ZCV when using switching sequence in Fig. 5.

cluster component of the switching frequency and the multiple of the switching frequency take place.

The common mode voltage shown in the figure will cause a large third order circulating current to appear when the rectifier is connected to an inverter with four wire loads and grounding of the neutral potential is desired. The low order circulating current will affect the line input currents which finally ruins the rectifier system. A deeper discussion of this issue will be presented in the next subsection.

C. Generation of Common Mode Voltage in a Current Source Buck Rectifier

A possible explanation for the unfeasibility of the implementation of standard SVM to a rectifier that is connected to an inverter with four wire loads and a grounded neutral potential can be understood by investigating the generation of the common mode voltage. By using standard SVM and the switching state sequence shown in Fig. 5, the amplitude of the common mode voltage can be calculated from:

$$V_{CM-PN} = \frac{d_\gamma . V_\gamma + d_\delta . V_\delta + d_0 . V_0}{2} \tag{3}$$

As seen from equation (3), the common mode voltage generated by a standard current source rectifier has two components: one is given by the combination of the two active current vectors (ACV) dictated by the direction of the input current reference vector which can not be changed and the other one is given by the zero current vector (ZCV) which can be changed by choosing any of the input voltage potentials.

Fig. 8 shows the association between the amplitude of the third order common mode voltage and the modulation index, m_i for $230V_{rms}$ of phase supply voltage. It can be seen that the polarity of the common mode voltage produced by the ACV is opposite the ZCV gated to the lowest absolute value of the input phase voltage. At a modulation index of 0.667, which corresponds to a 0.577 voltage transfer ratio, the magnitude of the low order common mode voltages generated by the ACV and the ZCV are equal to 54V, which illustrate that the total common mode voltage is zero. The figure also shows that the total common mode voltage becomes negative when m_i is lower than 0.666 (the ZCV is higher than the ACV).

On the other hand, the total common mode voltage is increasing with a positive amplitude when the m_i exceeds 0.666 and reaches a maximum of 81V (the common mode voltage generated by the ACV only) at a modulation index equal to 1. Fig. 8 also shows that it is possible for a three-switch buck rectifier to provide zero-average common mode voltage by using SVM techniques utilizing a chosen combination of ZCV. However this approach is limited by the margin of the ZCV, which is the only adjustable component. From this figure, it can also be seen that the margin of the ZCV is when m_i is lower than 0.666, which corresponds to a 0.577 voltage transfer ratio. This subject will be discussed in the next section.

IV. Cancellation of Common Mode Voltage in a 3-phase Current Source Buck Rectifier

In the previous section, it was revealed that the appearance of a low frequency common mode voltage component in the DC-link voltage will cause a large third order circulating current when the rectifier output is connected to an inverter feeding a four wire load and having its neutral point grounded. This low order circulating current will affect the input line currents which will finally disturb the performance of the whole rectifier system. Therefore, this section proposes and analyzes possible methods to cancel the low order component in the common mode voltage, based on software modification of the standard buck rectifier.

The zero current vector, d_0, can actually be a combination of two or multiple zero current vectors that can adjust the value and sign of the common mode voltage of the rectifier. A unique combination of zero current vectors is able to cancel any low (third) order component of the common mode voltage caused by the use of active current vectors. However, the third order common mode voltage component produced by a buck rectifier controlled by SVM can be fully eliminated by modifying the commutation pattern, but the level of the voltage delivered to the DC-link is drastically reduced from a 0.867 to a 0.578 voltage transfer ratio [12]-[15].

A. Influence of Switching on the Common Mode Voltage

By utilizing an appropriate combination of zero current vectors, zero-average common mode voltage over a switching period can be achieved. From Fig. 9, it can be seen that by using two zero current vectors: one gated at the most positive

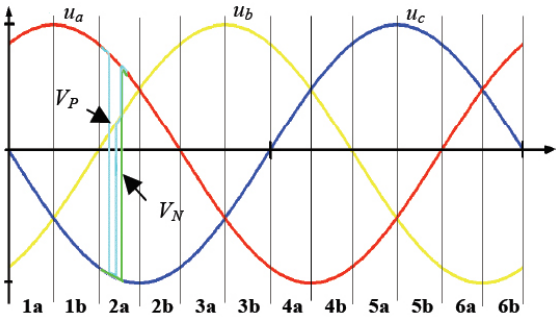

Fig. 9. Sector division of SVM to eliminate common mode voltage by gating zero current vectors to the most positive and the most negative line voltage.

absolute value of the phase voltage (V_{0+}) and the other one gated at the most negative absolute value of the phase voltage (V_{0-}) with an optimum duty cycle split will eliminate the common mode voltage. The implementation requires that, instead of the six sectors in standard SVM, the space vector plane is divided into 12 sectors from the division of each sector into two sub-sectors to realize the intervals depicted in Fig. 9. The duty cycle of both zero current vectors is derived from equation (4):

$$V_{CM-PN} = \frac{d_\gamma.V_\gamma + d_\delta.V_\delta}{2} + \sum d_0.V_0 = 0 \quad (4)$$

Recall that

$$d_0 = d_{0-} + d_{0+} = 1 - \left(d_\gamma + d_\delta\right) \quad (4a)$$

By substituting (4a) into (4) the following expression is obtained:

$$d_\gamma.V_\gamma + d_\delta.V_\delta + 2d_{0-}.V_{0-} + 2d_{0+}.V_{0+} = 0 \quad (5)$$

When (5) is solved, the optimum duty cycles to compensate the common mode voltage can be rewritten as:

$$d_{0-} = \frac{2d_0.V_{0+} + d_\gamma.V_\gamma + d_\delta.V_\delta}{2V_{0+} - 2V_{0-}} \quad \text{and}$$

$$d_{0+} = d_0 - d_{0-} \quad (6)$$

For example, in sector 2a, the most positive (V_+) and the most negative line voltages (V_-) are u_a and u_c respectively. Therefore, the optimum split duty cycle of the zero current vectors can be determined:

$$d_{0-} = \frac{2d_0.u_a + d_\gamma\left(u_a + u_c\right) + d_\delta\left(u_b + u_c\right)}{2u_a - 2u_c}$$

and $$d_{0+} = d_0 - d_{0-} \quad (7)$$

The main drawback of this is that the voltage transfer ratio of the buck rectifier has to be limited to 0.578, which in many cases disqualifies this topology from possible utilization.

B. The Switching Sequence to Eliminate Common Mode Voltage

For the purpose of eliminating the common mode voltage, it is not possible to implement a standard switching scheme, as shown in Fig. 5. This is because the two zero current vectors must be gated at the two input phase voltages highest in absolute value as described in the previous section. Taking into consideration sector 2a in Fig. 9 for example, the phase voltages u_a and u_c meet the criteria $\{|u_a|;|u_c|\} > |u_b|$. Therefore, the power transistors S_a and S_c are gated within this angle interval. In order to achieve the minimum switching losses, a unique sequence of switching states has to be implemented. This sequence consists of four different switching states (two active switching states and two zero states), which are arranged symmetrically, as shown in Fig. 10.

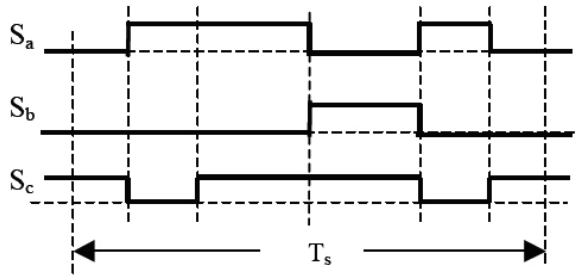

Fig 10. Switching sequence combination to eliminate common mode voltage for case of *VPN-ref* < 0.578 Vl-l(peak).

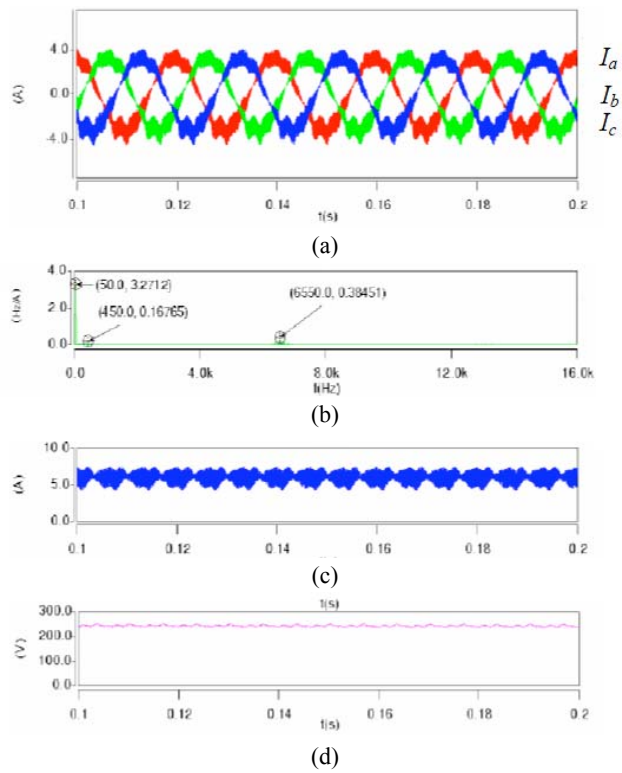

Fig. 11. Simulation results for the buck rectifier operating with combination of two zero current vectors switching state sequence (a) input line currents, (b) spectrum of *Ia*, (c) buck rectifier DC output inductor current and (d) DC output voltage when reference output voltage was set at 240Vdc.

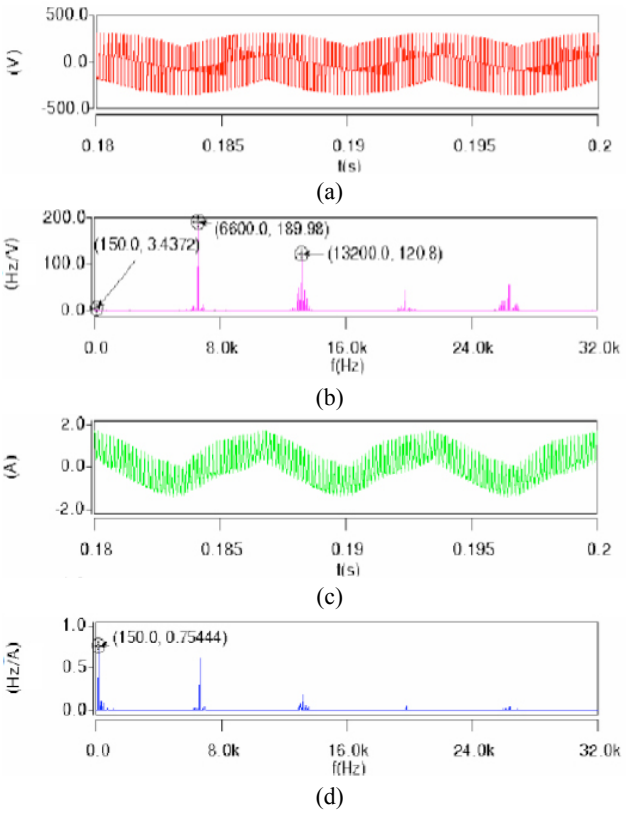

Fig. 12. Simulation results when operating with combination of two zero current vectors switching state sequence (a) Common mode voltage, *VCM* (b) spectrum of *VCM,* (c) common mode current that flows through the 5 Ohm resistor that connects the middle point of the DC-link capacitor at the supply neutral and (d) spectrum of the common mode current when reference output voltage was set at 240Vdc.

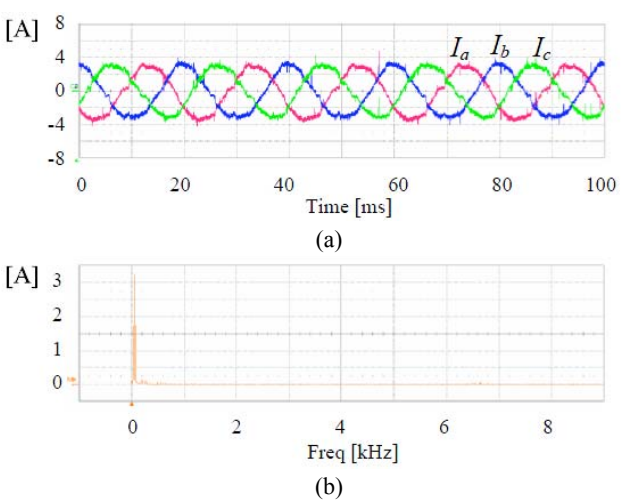

Fig. 13. Experimental result showing the operation of the buck rectifier with software modification: (a) the three phase line currents *Ia*, *Ib* and *Ic* (2 A/div) (10ms/div), (b) the spectrum of *Ia* (500mA/div) (1kHz/div).

The switching sequence provides the lowest switching losses to implement common mode voltage elimination. Only one hard turn-on switching and two hard turn-off switchings occur in the buck rectifier switches within one switching period, (T_s) with the chosen switching state sequence. It is important to note that switching between the two zero current vectors changes the DC terminals (from one phase voltage to another) without contributing any switching losses since the current through the switch is zero (because the freewheeling diode conducts the current). Thus it can be concluded that by using this switching sequence, the total switching losses of the rectifier are higher than when continuously turning-on the switch connected to the lowest absolute value of the input phase voltage during the zero current vector but lower than when continuously turning-on the switch connected to the highest absolute value of the input phase voltage during the zero current vector.

V. Simulation And Experimental Results Of The Proposed Technique

A. Simulation of a Three-switch Buck Rectifier using the Combination of Two Zero Current Vectors to Eliminate the Common Mode Voltage

This section presents the simulation results of a buck rectifier run with parameters similar to the ones given in section III (b) except that the mid point of the DC link is grounded through a 5 Ω resistor. These results were obtained by operating the buck rectifier with the combination of two zero current vectors discussed in the previous section, in order to confirm the validity of the proposed switching sequence. It is important to note here that the converter is operates in an open loop where the DC link current is not controlled.

During the simulation, the rectifier is set to operate at m_i = 0.5 to produce 240V_{dc} of output voltage and 1.44kW of output power. Fig. 11(a) illustrates the input line currents I_a, I_b and I_c, while the spectrum of i_a is shown in Fig 11(b) to reveal the overall quality of the waveforms. From both figures, it can be seen that the shapes of all of the input currents are nearly sinusoidal but with the presence of a small ninth order harmonic component.

In the low order harmonic range, the amplitude of the fundamental component is 3.27A_{peak} while the small amplitude 0.17A_{peak} of the ninth order harmonic, which corresponds to 5% of the fundamental component, appears. Fig. 11(c) and Fig. 11(d) show the 6A_{dc} average output inductor current with the presence of a low switching ripple 1.5A_{peak} current and the 240V_{dc} output DC voltage of the rectifier respectively.

Fig. 12(a) and Fig 12(b) show that the common mode voltage waveform generated by the buck rectifier and its correspondence spectrum give a good agreement with the expectations. At a low frequency, the third order common

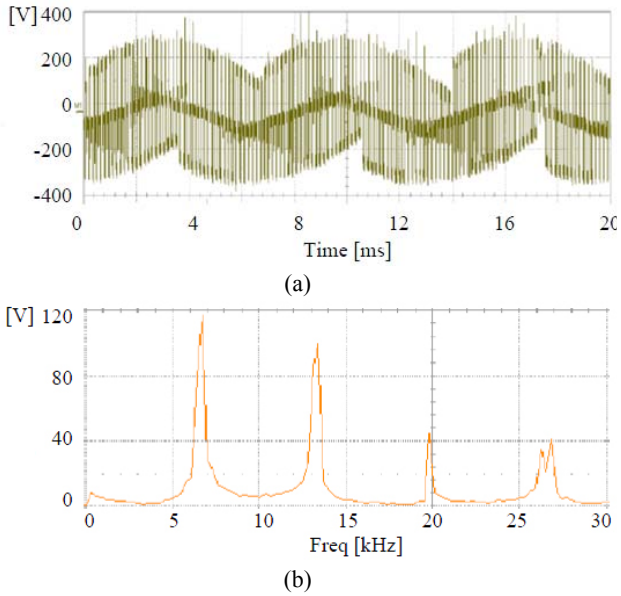

Fig. 14. Experimental result showing the operation of the buck rectifier with software modification: (a) the common mode voltage measured across the load (200V/div) (2ms/div) and (b) spectrum of (a) (40 V/div) (5kHz/div).

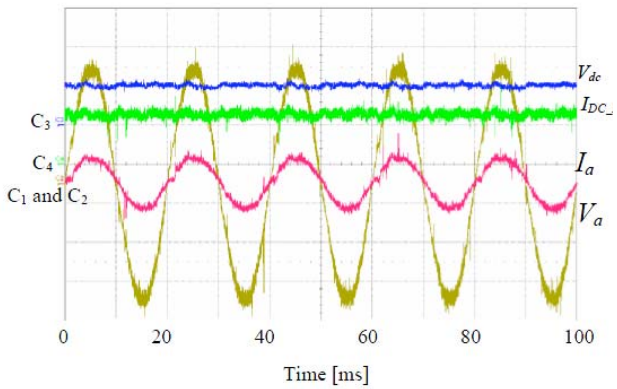

Fig. 15. Experimental result showing the operation of the buck rectifier with software modification; the waveforms of the DC output voltage *Vdc* (200V/div)(C3), the DC inductor current *IDC_L* (5 A/div) (C4), input phase voltage *Va* (100V/div) (C1) and its current *Ia* (5Adiv) (10ms/div) (C2).

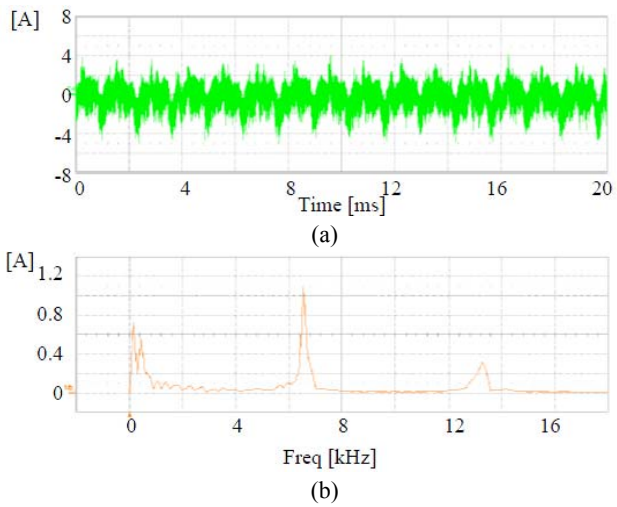

Fig. 16. Experimental result showing the operation of the buck rectifier with software modification: (a) the common mode current measured through 5Ω grounding resistor (2A/div)(10ms/div) and spectrum of (a) (200mA/div) (2 kHz/div).

mode voltage has been reduced to $3.44V_{peak}$ while at the switching frequency, common mode voltages of $189.98V_{peak}$ @ 6.6 kHz and $120.80V_{peak}$ @ 13.2 kHz are generated. However, due to the high order, a smaller size common mode filter can be used to limit the current ripple. The common mode current that flows through the 5 Ohm resistor that connects the middle point of the DC-link capacitors to the supply neutral and its corresponding spectrums are depicted in Fig. 12(c) and 12(d) respectively. As expected, the third order harmonic is kept low at $0.754A_{peak}$. In the high frequency region, approx. $0.6A_{peak}$ @ 6.6 kHz is generated. It is worth mentioning that cancellation of the common mode voltage normally causes an excessive increase in the switching losses, since commutation from an active current vector to a zero current vector normally results in high switching voltages (in addition to being gated at the highest absolute value of the phase voltage).

In general, the simulation results confirm a successful reduction of the common mode voltage and common mode current. DC and input currents with a better shape are also a result of applying this software solution. A better line current can be obtained by increasing the value of both of the DC inductors connected to the positive and negative rail of the buck rectifier (which is not investigated here). Furthermore, the amplitude of the third order common mode voltage and the current can be minimized by increasing the switching frequency. However, it is important to note that increasing the switching frequency also increases the switching loss.

The appearance of a common mode voltage with a high amplitude at the switching frequency and multiples of the switching frequency is the main weakness of this method. However, they can be effectively addressed with small size common mode filters. Although it is possible to reduce the common mode voltage by using this software solution, the level of voltage delivered to the DC-link is drastically reduced leading to a poor utilization of the power semiconductors, which means that other ways to improve the voltage transfer ratio need to be explored.

B. Experimental Evaluation of the Cancellation of the Common Mode Voltage in a Buck Rectifier

This section presents the experimental results of the proposed switching technique in order to eliminate the common mode voltage in a three-phase four wires buck rectifier. The operating behaviour of the system prototype

was investigated at $200V_{rms}$ of phase voltage and a 6.6 kHz switching frequency. This is due to the fact that by limiting the input voltage to ~87% of rated voltage ($230V_{rms}$), the amount of reactive power is limited to approximately 75%.

It is important to note that, for this experiment the middle point of the DC-link capacitor is grounded and the converter is operates in an open loop. Similar to the simulation setup, a 5Ω-grounding resistor is connected between the middle point of the DC-link capacitor and the neutral supply. The input currents I_a, I_b and I_c are shown in Fig. 13 to have a sinusoidal shape with an amplitude of approx $3.23A_{peak}$. When compared with the standard SVM previously discussed, it can be seen that clamping the zero current vectors at the most positive/most negative input phases voltage does not change the overall quality of the input currents. In comparison with the simulation result shown in Fig. 11, the experimental result show a better shape for the current waveform because a variac which has big line inductance is used to supply voltage to the rectifier. This inductance helps to filter the input current before it is fed to the rectifier.

Fig. 14 shows the common mode voltage generated by the three-switch buck rectifier and its corresponding spectrum. As expected, in the low harmonic range, the third order common mode voltage is effectively cancelled by this software modification. However, in the high frequency range, it can be noted that the cancellation of the common mode voltage at a low modulation index in a standard buck rectifier is made at the expense of excessive increases in the high frequency common mode voltage: which reaches approximately $116V_{peak}$ @ 6.6 kHz and $90V_{peak}$ @ 13.2 kHz. This experimental result also shows a good agreement with the simulation result shown in Fig. 12.

The DC output voltage V_{dc}, the DC inductor current I_{DC_L}, one of the input phase voltages and its corresponding line current are presented in the upper side of Fig. 15. It can be seen that a smooth DC inductor current of approximately $6A_{peak}$ and a DC output voltage of approximately $215V_{dc}$ are obtained. It is also clear that the line current I_a has a sinusoidal shape and is slightly leading the phase input voltage V_a because of the low output power levels of the input filter capacitor.

The common mode current that flows through the 5Ω grounding resistor that connects the middle point of the DC-link capacitors to the supply neutral and its corresponding spectrum waveforms are depicted in Fig. 16. As expected, the third order harmonic and the ninth order harmonic are kept low at approximately $0.7A_{peak}$ and $0.6A_{peak}$, respectively. In the high frequency region, a common mode component of approximately $1.1A_{peak}$ @ 6.6 kHz is generated. However, it is possible to more effectively reduce the high frequency common mode current component with a small size common mode choke. In general, the experimental results show a good agreement with the simulation results shown in Fig. 11 and Fig. 12.

VI. CONCLUSIONS

This paper shows that for a three-switch buck rectifier having the DC-link mid point grounded, it is not possible to use the standard SVM because large zero-sequence third order current harmonics will build up. The large third order circulating current that appears is caused by the common mode voltage generated by the buck rectifier. A common mode choke to limit the circulation of the third-order common mode current is possible to solve this problem but it is not feasible since the size of a common mode choke depends on 1/frequency and its cost will be prohibitive. Therefore, other active methods involving software modifications to reduce the common mode voltage/current have been proposed.

It was shown that it is possible to eliminate the common mode voltage by manipulating the zero current vectors in the SVM. However, the voltage transfer ratio of the buck rectifier was found to be limited to 0.577, which in many cases disqualifies this topology from possible utilization. However, for specific applications i.e ground power units (GPU), where the output of the AC-AC converter is $120V_{rms}$ with 400 Hz (a three-phase four-wire where the mid point of the DC link is grounded), a combination of the proposed switching technique and a buck-type active front-end rectifier topology make a suitable choice for a transformer-less GPU.

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Mohd Junaidi Abdul Aziz was born in Kuala Terengganu, Malaysia, in 1979. He received his B.S. and M.S. in Electrical Engineering from the Universiti Teknologi Malaysia (UTM), Malaysia, in 2000 and 2002, respectively, and his Ph.D. in Electrical Engineering from The University of Nottingham, U.K, in 2008. Since 2008, he has been with the Faculty of Electrical Engineering, Universiti Teknologi Malaysia (UTM), Malaysia, where he is currently a Senior Lecturer. His research interests include power electronics and electric vehicles with a special focus on battery management systems.

Christian Klumpner (S'00–A'01–M'02) was born in Resita, Romania, in 1972. He received his B.S. in Electromechanical Engineering from the University of Resita, Resita, Romania, in 1995, and his M.S. and Ph.D. in Electrical Engineering from the "Politehnica" University of Timisoara, Timisoara, Romania, in 1996 and 2001, respectively. From 1996 to 1997, he was with Bee Speed, Timisoara, Romania. Between 1998 and 2000, he was a Guest Researcher at the Institute of Energy Technology, Aalborg University, Aalborg, Denmark, working on matrix converters, under the auspices of the Danfoss Professor Program. From 2001 to 2003, he was a Research Assistant Professor at the Institute of Energy Technology, Aalborg University, continuing research into direct power conversion under the auspices of the Innovation Post-Doc Program supported by the Danish Research Agency and Danfoss Drives A/S. Since October 2003, he has been with the School of Electrical Engineering, The University of Nottingham, Nottingham, U.K., where he is currently an Associate Professor. His research interests include power electronics and ac drives, with a special focus on direct power conversion. Dr. Klumpner was the recipient of the Isao Takahashi Power Electronics Award for outstanding achievements in power electronics at the International Power Electronic Conference (IPEC2005) organized by the Institute of Electrical Engineers of Japan (IEEJ) in Niigata, Japan.

Jon Clare (M'90–SM'04) was born in Bristol, England. He received his B.S. and Ph.D. in Electrical Engineering from the University of Bristol, Bristol, U.K. From 1984 to 1990, he was a Research Assistant and a Lecturer at the University of Bristol, where he was involved in teaching and research on power electronic systems. Since 1990, he has been with the Power Electronics, Machines, and Control Group, The University of Nottingham, Nottingham, U.K., where he is currently a Professor in power electronics. His research interests include power electronic converters and modulation strategies, variable-speed drive systems, and electromagnetic compatibility. Prof. Clare is a Member of the Institution of Engineering Technology.