JPE 12-1-13

http://dx.doi.org/10.6113/JPE.2012.12.1.98

Modified Digital Pulse Width Modulator for Power Converters with a Reduced Modulation Delay

Jaber Abu Qahouq†, VaraPrasad Arikatla*, and Thanukamalam Arunachalam*

†* Dept. of Electrical and Computer Eng., The University of Alabama, Alabama, USA

Abstract

This paper presents a digital pulse width modulator (DPWM) with a reduced digital modulation delay (a transport delay of the modulator) during the transient response of power converters. During the transient response operation of a power converter, as a result of dynamic variations such as load step-up or step-down, the closed loop controller will continuously adjust the duty cycle in order to regulate the output voltage. The larger the modulation delays, the larger the undesired output voltage deviation from the reference point. The three conventional DPWM techniques exhibit significant leading-edge and/or trailing-edge modulation delays. The DPWM technique proposed in this paper, which results in modulation delay reductions, is discussed, experimentally tested and compared with conventional modulation techniques.

Key Words: Counter, Delay, Digital Control, Digital Pulse Width Modulation, Power Control, Power Converter, Transient Response

I. INTRODUCTION

Digital control is increasingly being used in power converters and power electronics systems because of the advantages it brings especially when compared to analog control [1]–[14]. These advantages include, among others, the ability to perform more advanced and sophisticated functions that potentially result in improved power conversion efficiency and/or dynamic performance of the power converter, the ease of adding digital control functions and loop upgradability (or revision), and decreased sensitivity to component variations when compared to analog controllers [7]–[12].

Digital control advantages come with several challenges and drawbacks [12]–[17]. These include, among others, additional control loop delays that impact the dynamic performance of the power converter and the additional controller power consumption in some digital control implementations. The first drawback is compensated for in some implementations by applying non-linear and predictive control schemes in order to obtain overall dynamic performance that is better than that obtained with analog controllers.

The second drawback can be alleviated or reversed by circuit design methods, such as by using digital CMOS circuit technologies with a smaller feature size and a lower power consumption, and by utilizing the ability of digital controllers to utilize adaptive control schemes that result in improving the power converter efficiency (reducing the power converter stage power losses) [13], [17].

Digital Pulse Width Modulation (DPWM) is a necessary part in digital power controller system implementation [2], [16], [17], [21]. It converts the duty cycle value generated by the closed loop compensator of a controller to ON and OFF time durations in order to control the power switches of the power converter and to regulate the output voltage (refer to Fig. 1). Unlike an Analog PWM (APWM), a DPWM has a finite resolution. The higher DPWM resolution results in better output voltage regulation and a lower possibility of limit cycle oscillation instabilities [2], [14]–[17], [21]. However, it may result in increases in DPWM circuit power consumption and size increase.

Moreover, DPWM has modulation delays. These are the time delays that the DPWM needs in order to change its output to a new duty cycle after the closed loop compensator commands a new duty cycle value. During transient response the operation of a power converter as a result of dynamic variations, such as a load step-up or step-down, the closed loop controller will continuously adjusts the duty cycle in order to regulate the output voltage. The larger the delay, the larger the undesired output voltage deviation from the reference point [16]–[19]. Therefore, there is a motivation to reduce the closed-loop delays including the DPWM modulation delays at a given switching frequency of the power converter.

This paper presents a modified DPWM scheme with a reduced digital modulation delay (DPWM transport delays) during the transient response of power converters. The three conventional DPWM techniques exhibit large leading-edge and/or trailing-edge modulation delays. The DPWM technique proposed in this paper, which results in modulation delays

Manuscript received Jul. 1, 2011; revised Oct. 27, 2011
Recommended for publication by Associate Editor Yong-Chae Jung.
† Corresponding Author: jaberq@eng.ua.edu, jaberq@ieee.org
Tel: +1-205-348-8669, Fax: +1-205-348-6959
* Dept. of Electrical and Computer Eng., The University of Alabama, USA

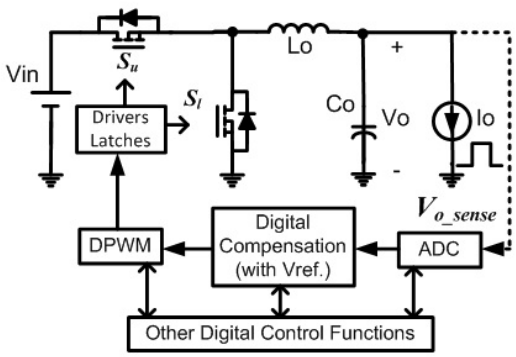


Fig. 1. Block diagram of DC-DC buck converter with digital controller.

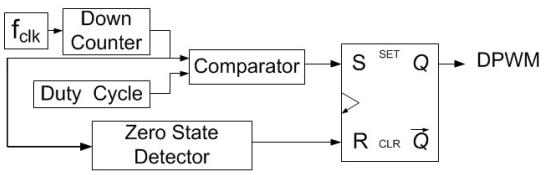


Fig. 2. An example of a counter-based leading-edge DPWM circuit block diagram.

reductions, is discussed, experimentally tested and compared with existing modulation techniques.

Section II briefly reviews the conventional DPWM schemes. Section III presents the proposed modified DPWM modulation scheme (MDPWM). Section IV presents the FPGA (Field Programmable Gate Array) implementation experimental results. Section V includes additional comments on the MDPWM while Section VI gives the conclusions.

II. Conventional DPWM Modulation Schemes

This section briefly reviews three conventional DPWM modulation schemes. They are the leading-edge modulation scheme, the trailing-edge modulation scheme, and the dual-edge modulation scheme. There are different circuit implementations for each of the digital modulation schemes, such as counter-based implementations, delay-line based implementations, and hybrid implementations, to mention a few [3], [4], [16]. Fig. 2 shows an example of a counter-based leading-edge DPWM circuit block diagram. The different DPWM modulation schemes are shown in Fig. 3(a)-(c).

During load step-down transients, the output voltage of a DC-DC buck converter (used as an example here) is expected to overshoot. As a result, the closed loop compensator will command a reduction in the duty cycle value (it will provide a new calculated value to the modulator). During load step-up transients, the output voltage of a DC-DC buck converter is expected to undershoot. As a result, the closed loop compensator will command an increase in the duty cycle value. The faster the DPWM responds to the new duty cycle command of the closed loop compensator, the smaller the output voltage deviation (overshoot/undershoot).

As illustrated in Fig. 3, the leading-edge modulation scheme exhibits a turn OFF delay, which causes a time delay in the response to load step-down transients. The trailing-edge modulation scheme exhibits a turn ON delay, which causes a time delay in the response to load step-up transients. The

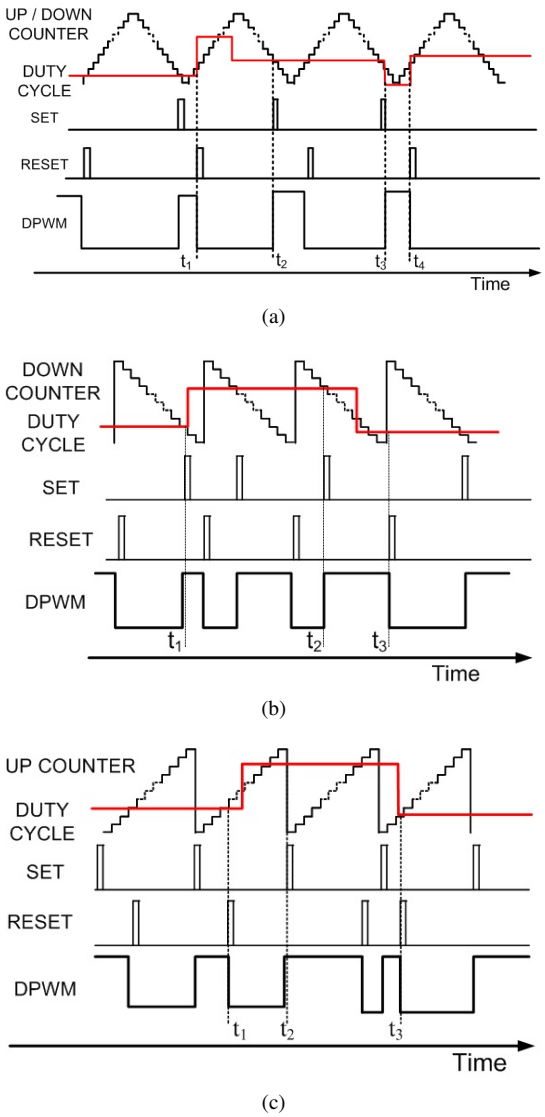


Fig. 3. (a) Conventional dual-edge DPWM scheme. (b) Conventional leading-edge DPWM scheme. (c) Conventional trailing-edge DPWM scheme.

dual-edge modulation scheme exhibits both a turn OFF delay, which is smaller than the leading-edge modulation scheme turn OFF delay, and a turn ON delay, which is smaller than the trailing-edge modulation scheme turn ON delay.

The modulation delays, which are transport delays, affect the closed loop performance and slow down the dynamic response of the power converter system.

The value of the turn OFF delay for leading-edge modulation is given by Eq. (1) and the value of the turn ON delay for trailing-edge modulation is given by Eq. (2).

$$t_{DPWM-leading} = (1 - D_a) \cdot T_{sw} \tag{1}$$

$$t_{DPWM-trailing} = D_a \cdot T_{sw} \tag{2}$$

where D_a is the steady state value of the duty cycle and T_{sw} is the switching time period.

For the dual-edge modulation scheme, the modulation delay time is given by Eq. (3) and Eq. (4).

$$t_{DPWM-dual} = 0.5 \cdot (1 - D_a) \cdot T_{sw} \tag{3}$$

(When duty cycle decreases or is at the leading edge)

$$t_{DPWM-dual} = 0.5 \cdot D_a \cdot T_{sw} \quad (4)$$

(When duty cycle increases or is at the trailing edge)

In a conventional digital controller the duty cycle command can be calculated either once (single sample) per switching cycle or multiple times (multisampling rate) [6] in order to generate a compensated error signal. However, in both cases, a conventional DPWM generates/updates only one duty cycle command per switching cycle. The modulation delay, which is associated with the update of the duty cycle, is constant for a DPWM and is equal to T_{sw}.

Next section proposes a modified DPWM modulation scheme with reduced modulation delays.

III. Proposed DPWM Modulation Scheme

Fig. 4 illustrates the proposed modified DPWM (MDPWM) with leading-edge modulation as an example. Fig. 4(a) shows a block diagram of the MDPWM while Fig. 4(b) shows the operation waveforms.

The operation of the MDPWM can be summarized as follows: When the compensator output value (duty cycle command) is larger than the main down-counter count value, the auxiliary up-counter counts up. In the case of the conventional leading-edge DPWM (refer to Fig. 2(b) and Fig. 4), the SR flip-flop is "set" high (its output is set to logic high or the DPWM is ON) when the main down-counter count down value becomes lower than the compensator duty cycle commanded value. In the conventional leading-edge modulation, the modulator output cannot be turned OFF any time after the main down-counter count down value becomes lower than the compensator duty cycle commanded value if the commanded duty cycle value is decreased. In this case, the conventional modulator output can only be turned OFF after the down-counter finishes counting to zero by re-setting the SR flip-flop with a clock (the duty cycle cannot be adjusted without transport delays), and therefore, there is a turn OFF delay. On the other hand, in the proposed MDPWM, the modulator output can also be turned OFF when the auxiliary up-counter count value is larger than the commanded duty cycle. Therefore, if the commanded duty cycle is reduced, the modulator output can be turned OFF at any time with a reduced or no turn OFF modulation delay via the auxiliary up-counter comparison circuit through the "OR" gate. The auxiliary up-counter value is reset to zero every time the main down-counter count value becomes lower than the commanded duty cycle value as can be seen from Fig. 4(b). Fig. 5 shows a delay line based implementation example for the proposed MDPWM.

The delay time for the MDPWM with leading-edge modulation is given by Eq. (5).

$$t_{MDPWM-leading} = (1 - D_a - \Delta D_1) \cdot T_{sw} \quad (5)$$

where $\Delta D_1 = D_{trans1} - D_a$ and D_{trans1} are the duty cycle values during the transient operation. These values usually deviate significantly from the steady-state value of the duty cycle and this deviation depends on the transient magnitude and type.

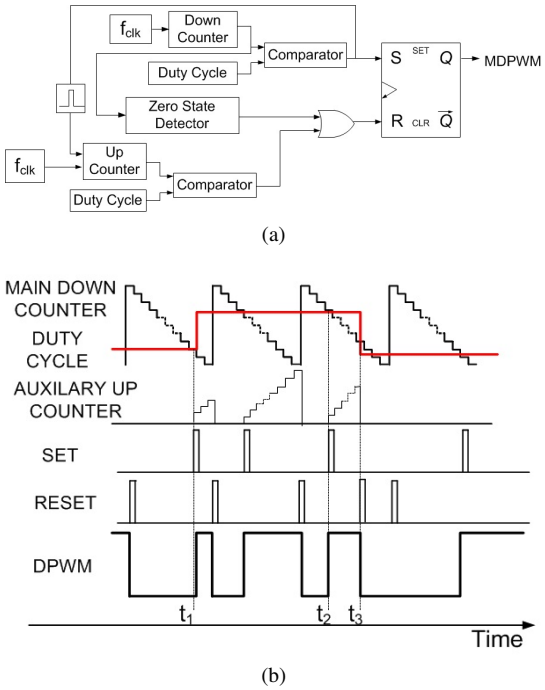


Fig. 4. The Proposed Modified DPWM with leading-edge modulation as an example. (a) Block diagram. (b) Operation Waveforms.

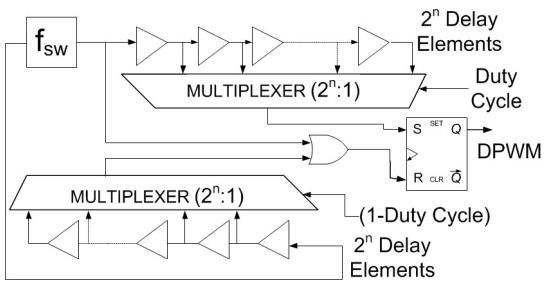


Fig. 5. Delay line based implementation example for the proposed MDPWM.

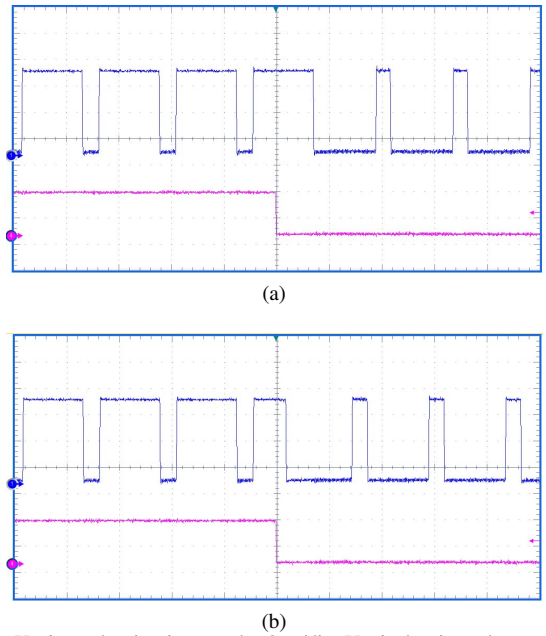
Similarly, the delay time for the MDPWM with trailing-edge modulation is given by Eq. (6).

$$t_{MDPWM-trailing} = (D_a - \Delta D_2) \cdot T_{sw} \quad (6)$$

where $\Delta D_2 = D_a - D_{trans2}$ and D_{trans2} are the duty cycle values during the transient operation.

Therefore, the modulation delay reduction with the MDPWM is proportional to the difference between the current steady-state value of the duty cycle and the new duty cycle calculated values during the transient (greater improvement is achieved under larger transients). Given certain regulation requirements and limits, reducing deviations that are the result of the worst case or large transients is more important. In order for the MDPWM to reduce the modulation delay, the compensated error signal has to be calculated multiple times (multisampling rate operation) during a switching period [6]. A multisampling rate digital controller is used for the implementation of the MDPWM as described in the next section. Again, the multisampling rate operation does not result in reductions in the conventional DPWM transport delays.

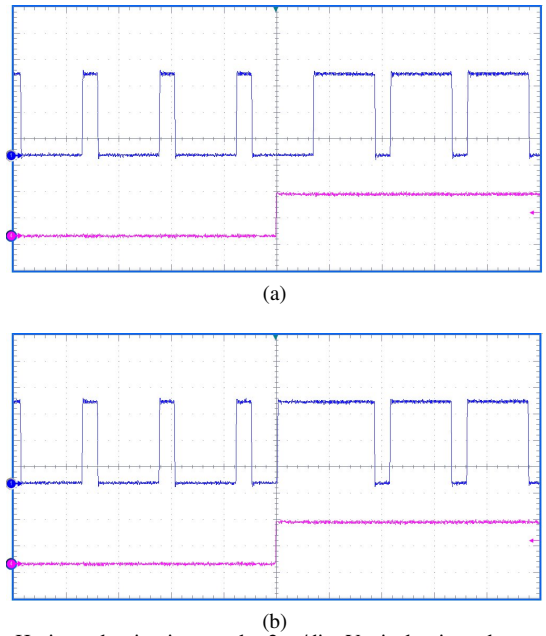
It should be noted that the switching frequency of the MDPWM is fixed during steady-state operation. The MDPWM creates a time shift in the control signal during the response



(a) (b)

Horizontal axis: time, scale: 2μs/div. Vertical axis: voltage, Top trace: DPWM, scale: 1V/div., Bottom trace: Duty Cycle Change Indication Signal, scale: 2V/div.

Fig. 6. View of several switching cycles during duty cycle Step-down from 0.8 to 0.2 for: (a) Conventional leading-edge DPWM. (b) Proposed MDPWM.



(a) (b)

Horizontal axis: time, scale: 2μs/div. Vertical axis: voltage, Top trace: DPWM, scale: 1V/div., Bottom trace: Duty Cycle Change Indication Signal, scale: 2V/div.

Fig. 7. View of several switching cycles during duty cycle Step-up from 0.2 to 0.8 for (a) Conventional trailing-edge DPWM. (b) Proposed MDPWM.

to transients in order to make the change in the duty cycle effective earlier with a reduced or no delay.

IV. Experimental Results

The experimental prototype is a single phase DC-DC buck converter with an 8V input voltage and a 1.5V output voltage. A 10-bit DPWM and a MDPWM with a switching frequency of 342 kHz are used. The power stage is achieved with an output inductor of 440nH and an output capacitance of 330μF. The conventional DPWM and the proposed MDPWM are implemented using a FPGA (Field Programmable Gate Array). An Altera Cyclone II EP2C35F672C6 chip is used. The controller calculates the compensated error signal 16 times (multisampling rate digital controller) per switching period.

Fig. 6 shows the open loop experimental results for the 10-bit conventional DPWM and for the proposed MDPWM. The duty cycle is varied between 0.8 and 0.2. The figures verify the theoretical operation described in the previous section and show that the turn OFF time delay of the conventional DPWM is significantly reduced when using the proposed MDWPM. Similar results can be obtained using the delay-line-based DPWM and the MDPWM.

In Fig. 6 the top trace is the DPWM or the MDPWM output of the modulator and the bottom trace represents the indication of the duty cycle change/transient from 0.8 to 0.2 and vice versa (a logic high of 0.8 and a logic low of 0.2). As can be seen in Fig. 6(a) and Fig. 6(b), when the duty cycle switches from 0.8 to 0.2, the conventional leading-edge modulator has a significant turn OFF delay while the proposed modulator has no or a smaller turn OFF delay. As can be seen in Fig. 7(a) and Fig. 7(b), when the duty cycle switches from 0.2 to 0.8, the conventional trailing-edge modulator has a significant turn ON delay while the proposed modulator has no or a smaller turn ON delay. The proposed MDPWM reduces the delays which results in reduced overshoot and/or undershoot in the output voltage.

Fig. 8 shows the closed loop experimental results during load step-down transients. Fig. 8(a) shows the results for the conventional leading-edge DPWM while Fig. 8(b) shows the results for the proposed DMPWM. The output voltage overshoot with the conventional leading-edge DPWM is about 90mV and with the proposed MDPWM it is 70mV. Therefore, a 20mV ($\sim$22%) output voltage deviation reduction can be observed for this design example. This is due to a significant reduction in the modulation delay when using the proposed MDPWM.

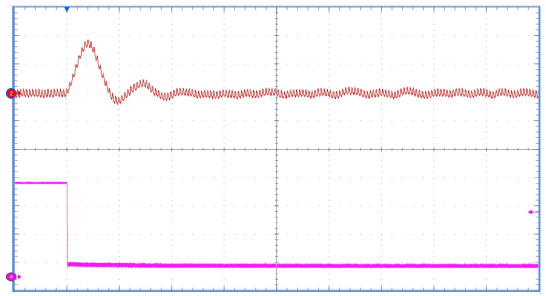
Fig. 9 shows the DPWM and MDPWM signals for two turn OFF instances during an output voltage overshoot (while the voltage is still in the process of ramping up). As can be seen, the MDPWM has a reduced turn OFF modulation delay, which resulted in a smaller output voltage overshoot. Note that the 90ns modulation delay, shown in Fig. 9, is 3.2% of the switching cycle.

During load step-up transients, the proposed MDPWM has the same results as the conventional leading-edge DPWM since both have no turn ON modulation delays as discussed earlier.

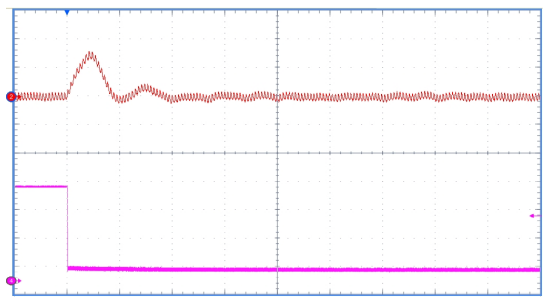
V. Additional Comments

A. Comment 1

While the following comment may seem obvious, it is important to note that increasing the conventional DPWM resolution by increasing the number of bits (resolution) will not result in solving the modulation delay issue addressed in



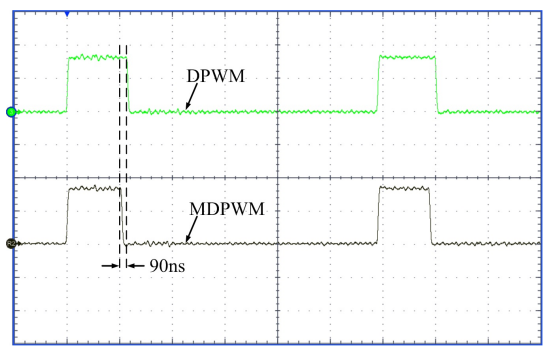
(a)



(b)

Horizontal axis: time, scale: 50μs/div. Vertical axis: voltage,
Top trace: Output voltage at 50mV/div., Bottom trace: Load current step-down transient of 6A.

Fig. 8. Closed-loop experimental results for (a) Conventional DPWM. (b) Proposed MDPWM.



Horizontal axis: time, scale: 500ns/div. Vertical axis: voltage,
Top trace: DPWM signal, Bottom trace: MDPWM signal

Fig. 9. Closed-loop experimental results comparing switching cycles for conventional DPWM and proposed MDPWM.

this paper. For example, if the number of bits in a conventional DPWM is increased from 10-bits to 20-bits, the result will be a more accurate (higher resolution) duty cycle value, but the modulation delay will still be there since the DPWM circuit has to wait until the end of the switching cycle to take the new duty cycle value from the compensator. The proposed MDPWM with a 10-bit main counter and a 10-bit auxiliary counter significantly reduces or eliminates the modulation delay while a conventional DPWM with 20-bits does not.

B. Comment 2

Since the MDPWM requires additional circuitry, there is a size and a power consumption increase when compared to a conventional DPWM. These size and power increases can be reduced by using newer integrated circuit technologies.

However, with this tradeoff, the MDPWM scheme can significantly reduce or eliminate a type of modulation delay that cannot be taken care of by increasing the digital modulator resolution. Moreover, the size increase (in terms of the digital components) is expected to be very small when compared to the option of adding additional output capacitors (analog component). In addition, the size and power increases become less significant as the power level of the power converter is increased. Note that the relatively low power converter design example used in this paper is only for demonstration purposes.

VI. Conclusion

This paper presents a modified digital pulse width modulation scheme (MDPWM) which has reduced modulation delays when compared with conventional digital modulation schemes. During the transient response operation of a power converter, as a result of dynamic variations such as load step-up or step-down changes, the closed loop controller will continuously adjusts the duty cycle to regulate the output voltage. The larger the modulation delay, the larger the undesired output voltage deviation from the reference point. Therefore, the elimination or reduction of digital modulation delays results in lower dynamic output voltage deviations in a power converter during transient conditions.

The proposed MDPWM operation is discussed, verified by experimental results and compared with conventional digital modulation schemes in this paper. The MDPWM can be used in power converters that utilize digital pulse width modulation in their controller to reduce modulation delays. These power converters can be found and used in wide range of applications.

Acknowledgment

This work is supported in part by the National Science Foundation (NSF) of the USA under Grant No. 0927104. The opinions, findings, conclusions and recommendations expressed in this paper are those of the author(s) and do not necessarily reflect the views of the National Science Foundation.

References

[1] P. J. Sun and L. W. Zhou, "Duty ratio predictive control scheme for digital control of dc-dc switching converters," *Journal of Power Electronics*, Vol. 11, No. 2, pp. 156-162, Mar. 2011.

[2] J. H. Kim, J. G Lim, and S. K. Chung, Y. J. Song, "Dsp-based digital controller for multi-phase synchronous buck converters," *Journal of Power Electronics*, Vol. 9, No. 3, pp. 410-417, May 2009.

[3] A. Prodic, D. Maksimovic, and R. W. Erickson, "Design and implementation of a digital PWM controller for a high-frequency switching DC-DC power converter," in *The 27th Annual Conference of the IEEE Industrial Electronics Society, IECON '01*, Vol. 2, pp. 893-898, 2001.

[4] A. Syed, E. Ahmed, D. Maksimovic, and E. Alarcon, "Digital pulse width modulator architectures,"in *IEEE 35th Annual Power Electronics Specialists Conference*, *PESC 04*, Vol. 6, pp. 4689- 4695, 2004.

[5] V. Yousefzadeh, and D. Maksimovic, "Sensorless optimization of dead times in DC-DC converters with synchronous rectifiers," *IEEE Trans. Power Electron.*, Vol. 21, No. 4, pp. 994-1002, Jul. 2006.

[6] L. Corradini, P. Mattavelli, E. Tedeschi, and D. Trevisan, "High-bandwidth multisampled digitally controlled DC–DC converters using ripple compensation," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 4, pp. 1501-1508, Mar. 2008.

[7] C. Sudhakarababu and M. Veerachary, "Dsp based control of interleaved boost converter," *Journal of Power Electronics*, Vol. 5, No. 3, pp. 180-189, Jul. 2005.
[8] T. Nussbaumer, M. L. Heldwein, G. Gong, S. D. Round, and J. W. Kolar, "Comparison of prediction techniques to compensate time delays caused by digital control of a three-phase buck-type PWM rectifier system," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 2, pp. 791-799, Feb. 2008.
[9] L. Peng, Y. Kang, X. Pei, and J. Chen, "A novel PWM technique in digital control," *IEEE Trans. Ind. Electron.*, Vol. 54, No. 1, pp. 338-346, Jan. 2007.
[10] Y. F. Chan, M. Moallem, and W. Wang, "Design and implementation of modular fpga-based pid controllers," *IEEE Trans. Ind. Electron.*, Vol. 54, No. 4, pp. 1898-1906, Apr. 2007.
[11] L. Guo, J. Y. Hung, and R. M. Nelms, "Evaluation of dsp-based pid and fuzzy controllers for dc–dc converters," *IEEE Trans. Ind. Electron.*, Vol. 56 , No. 6, pp. 2237-2248, Jun. 2009.
[12] J. A. A. Qahouq, and V. Arikatla, "Power converter with digital sensorless adaptive voltage positioning control scheme," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 9, pp. 4105-4116, Sep. 2011.
[13] B. Miao, R. Zane, and D. Maksimovic, "Automated digital controller design for switching converters," in *36th IEEE Power Electronics Specialists Conference*, *PESC '05,* pp. 2729-2735, 2005.
[14] A. V. Peterchev, and S. R. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters," *IEEE Trans. Power Electron.*, Vol. 18. No. 1, pp. 301-308, Jan. 2003.
[15] Z. Jianlong, M. Xikui, and D. Changqing, "Asymmetrical oscillations in digitally controlled power-factor-correction boost converters," *IEEE Trans. Circuits and Syst. II*, Vol. 56, No. 3, pp. 230-234, Mar. 2009
[16] V. Yousefzadeh, T. Takayama, and D. Maksimovi, "Hybrid dpwm with digital delay-locked loop," in *IEEE Workshop on Computers in Power Electronics*, *COMPEL '06,* pp. 142-148, 2006.
[17] W. Qiu, G. Miller, and Z. Liang, "Dual-edge pulse width modulation scheme for fast transient response of multiple-phase voltage regulators," in *IEEE Power Electronics Specialists Conference,* pp. 1563-1569, 2007.
[18] M. He, and J. Xu, "Nonlinear pid in digital controlled buck converters," in *IEEE Applied Power Electronics Conference*, Vol. 2, pp. 1461-1465, 2007.
[19] P.-L. Wong and F. C. Lee, "Switching action delays in voltage regulator modules," in *IEEE Power Electronics Specialists Conference*, Vol. 2, pp. 675-678, 2002.
[20] D. S. Sha, Z. Q. Guo, and X. Z. Liao, "Digital control strategy for input-series-output-parallel modular dc/dc converters," *Journal of Power Electronics*, Vol. 10, No. 3, pp. 245-250, May 2010.
[21] A. V. Peterchev, Jinwen Xiao, and S. R. Sanders, "Architecture and ic implementation of a digital vrm controller," *IEEE Trans. Power Electron.*, Vol. 18, No. 1, pp. 356-364, Jan. 2003.

Jaber Abu Qahouq received his B.Sc. (with first class honors) from Princess Sumaya University (PSUT)/Royal Scientific Society (RSS), Amman, Jordan, in 1998, and his M.S. and Ph.D. from the University of Central Florida (UCF), Orlando, USA, in 2000 and 2003, respectively, all in Electrical Engineering/Electronics. He is currently an Assistant Professor in the Department of Electrical and Computer Engineering, The University of Alabama, Tuscaloosa, USA. He was with Intel Corporation from August 2005 to January 2008. From January 2004 to August 2005, he was a Visiting Assistant Professor and Instructor with the School of Electrical Engineering and Computer Science, UCF, and from January 2002 to December 2003, he was an Adjunct Faculty member at UCF. He was a Research Assistant/Associate with the Florida Power Electronics Center, UCF, from 1999 to 2003. From 1998 to 1999, he was with the Royal Scientific Society (RSS), Electronic Services and Training Center (ESTC), Amman, Jordan. He led and worked on several projects funded by the NSF, USDA, Army Research Lab, NASA, Astec Power/Emerson, Intel, the University of Central Florida and the University of Alabama. His research interests include dc–dc converters, soft-switching power conversion, digital control in power electronics, adaptive power control, platform power delivery distribution architectures and related power management schemes, power factor correction ac-dc converters, and dc–ac inverters, renewable energy systems, and power devices, nanotechnology-based electronic devices, etc. Dr. Abu Qahouq is actively serving as a reviewer for several journal and conference publications including the IEEE Transactions and Conferences. He has also chaired several conference sessions over the years. He severed as a technical program committee member of the IEEE PESC 2007 conference, as a review committee member of the IEEE ISCAS 2008 conference, as a technical program committee member of the IEEE ICECS 2009, 2010, and 2011 conferences, as a technical program committee member of the IEEE ECCE 2010 and 2011 conferences, and as member of Intel's mobile platforms patent committee (when he was with Intel Corporation) among others. Dr. Abu Qahouq received the Division Recognition Award from the Systems Technology Lab, Corporate Technology Group, Intel Corporation in 2006, the IET Premium Award for Best Paper in 2009, the IEEE Outstanding Graduate Student Award in 2002, and the King of Jordan Royal Watch in 1998, among others. He has published many refereed journal and conference papers and holds several patents (thirteen US patents granted and many others pending as of September 2011). He is a Senior Member of the IEEE, a Member of Eta Kappa Nu and a Member of Phi Kappa Phi.

VaraPrasad Arikatla was born in Ongole, India. He received his B.Tech in Electronics and Communiations Engineeering from Acharya Nagarjuna University, India, in 2008. He received his M.S. in Electrical and Computer Engineering from the University of Alabama in May 2011. He is currently pursuing his Ph.D. in the Department of Electrical and Computer Engineering at the University of Alabama, Tuscaloosa, USA. His research interests include the modeling and control of power converters, high frequency power conversion, high frequency magnetics and energy harvesting. He has worked on reserch projects funded by the National Science Foundation, Department of Defense/Army Research Labs. He has served as a reviewer for the IEEE Energy Conversion Congress and Exposition Conference (ECCE 2010, ECCE 2011), the IEEE International Conference on Electronics, Circuits, and Systems (ICECS 2010, ICECS 2011) and the IEEE Applied Power Electronics Conference (APEC 2011, APEC 2012).

Thanukamalam Arunachalam was born in Rajapalayam, India. She received her B.E. in Electrical and Electronics Engineering from Anna University, India, in 2005 and her M.S. in Electrical and Computer Engineering from the University of Alabama, Tuscaloosa, USA, in 2010. Her research interests include the control of DC-DC power converters.