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Input Voltage Sharing Control for Input-Series-Output-Parallel DC-DC Converters without Input Voltage Sensors

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Abstract

Input-series-output-parallel (ISOP) modular converters consisting of multiple modular DC/DC converters can enable low voltage rating switches for use in high voltage input applications. In this paper, an input voltage sharing control strategy for input-series-output-parallel (ISOP) full-bridge (FB) DC/DC converters is proposed. By sensing the difference in the input current of two modules, the system can achieve input voltage sharing for DC-DC modules. The effectiveness of the proposed control strategy is verified by simulation and experimental results obtained with a 200w-50kHz prototype.

Key Words: DC/DC converters, Input-series-output-parallel, Input voltage sharing

I. Introduction

The input-series-output-parallel (ISOP) configuration contains multiple standardized converter modules connected in series at the input side and in parallel at the output side. This configuration has many advantages such as a modularized design, hot-swapping capability and suitability for high input voltage applications with low-voltage rating switches. To make this configuration work properly, input voltage sharing (IVS) and output current sharing (OCS) should be ensured. According to power balance, if IVS is obtained, OCS can be achieved automatically.

There are many control strategies for ISOP converters. The common duty ratio control [1], [2] is simple, but IVS and OVS can be obtained only for well-matched modules. The charge control [3] is implemented by the feedforward input voltage to improve the dynamic response, but both the input voltages and the input currents need to be sensed. Three loop control [4]–[6] is employed for ISOP converters to realize equal sharing of the input voltage and the dynamic response of the output voltage. The master/slave control [7] and the uniform voltage distribution [8] are adopted for ISOP converters to realize IVS. The neighboring input voltages sharing method [9] is implemented for ISOP converters. The strategies in [2]–[9] allow the configuration to achieve IVS, but the input voltage of each module has to be sensed. Senseless current control [10], which gives the system a good dynamic response, is implemented for ISOP converters. This control strategy can achieve a good dynamic response. By sensing the voltage over the output filter inductor, the output current is reconstructed. The cross-feedback output current control is proposed in [11]. With it power sharing can be achieve among the modules without sensing the input voltages.

Actually, these schemes [3]–[9] can be classified as input voltage control methods. The individual input voltages need to be sensed with many voltage sensors. When measuring high voltages, safely considerations are likely to demand galvanic isolation. Only high voltage sensors can be used under this condition. However, the current can be sensed by a Hall sensor, which is a kind of contact-less sensing method. This can avoid the electric isolation problem.

A control strategy, which provides a simple method for obtaining IVS by only measuring the difference in input currents between neighboring modules, is presented for ISOP DC-DC converters in this paper. A current sensor is only used for two-module ISOP systems. The number of sensors is reduced and there is no need to sense the input voltages. The principle behind the control strategy is analyzed and a $200W$ prototype is built for experimental evaluation.

II. Control Strategy for the System

A. Main Circuit of Input-series-output-parallel Converters

Fig. 1 shows a schematic of an ISOP system comprising of n high frequency isolated dc-dc converter modules. In this configuration, the total input voltage v_{in} is divided by the input capacitors C_{d1}, $C_{d2} \ldots C_{dn}$. As a result, the voltages v_{cd1}, $v_{cd2} \ldots v_{cdn}$, working as individual input voltages for each module, are obtained. If v_{cd1}=v_{cd2}=. . . =v_{cdn}, then i_{o1}=i_{o2}=. . . =i_{on} can be obtained. On the other hand, if

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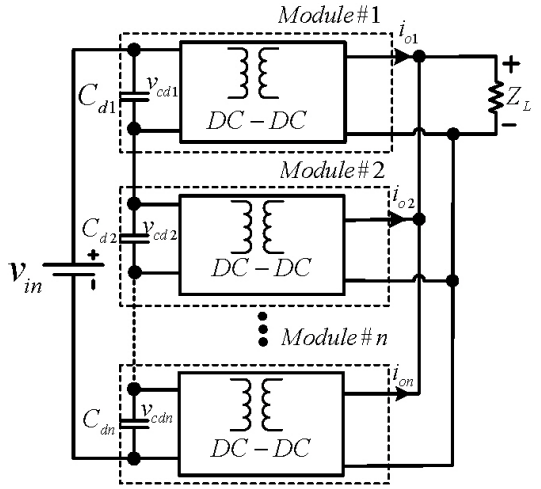

Fig. 1. ISOP connected n-high frequency isolated converter modules.

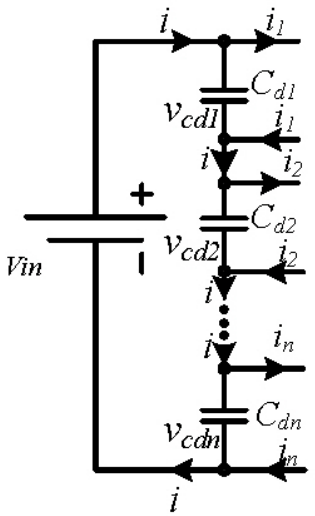

Fig. 2. the circuit of the input capacitors.

i_{o1}=i_{o2}=…=i_{on}, then v_{cd1}=v_{cd2}=…=v_{cdn} can be obtained [10]. The basic objective of an ISOP converter is to share power among the constituent converters. In order to achieve power sharing, a dedicated control is necessary for sharing the input voltage or the output current among the modules.

B. General Control Scheme

The equivalent circuit of Fig. 1 from the input side can be seen in Fig. 2. According to Kirchhoff 's law, provided that C_{d1}=C_{d2}=…=C_{dn}=C, the following is obtained:

$$\begin{cases} i = i_1 + C\dfrac{dv_{cd1}}{dt} \\ i = i_2 + C\dfrac{dv_{cd2}}{dt} \\ \cdots \\ i = i_n + C\dfrac{dv_{cdn}}{dt} \end{cases} \tag{1}$$

Therefore:

$$v_{cdj} - v_{cd(j+1)} = -\frac{1}{C}\int (i_j - i_{j+1})dt \tag{2}$$

where j corresponds to the converter number. According to (2), the difference in the input voltages between neighboring modules can be reconstructed by the difference in the input currents between them. The general control strategy for the ISOP converter is shown in Fig. 3.

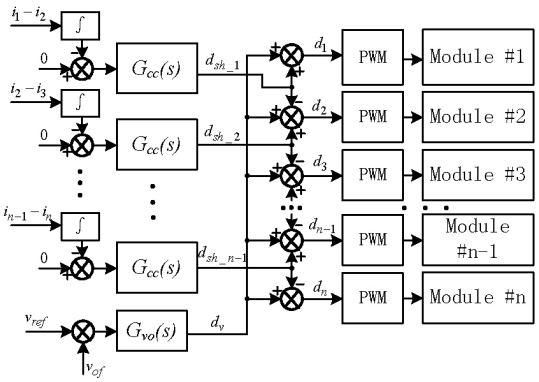

Fig. 3. the diagram of the proposed control strategy.

The general control strategy for the system is shown in Fig. 3, where v_{ref} is a reference, v_{fb} is the feedback voltage signal, and the input current over each module is denoted as i_1, i_2, …, i_{n-1}, i_n. $G_{vo}(s)$, which guarantees the output voltage tracking of the voltage reference, is the compensator network of the output control loop. $G_{cc}(s)$ is the compensator network of the input voltage sharing control loop, which causes the input voltage to be equally shared among the individual modules. Both $G_{vo}(s)$ and $G_{cc}(s)$ are PI regulators, which make the feedback of the output voltage track the output reference with zero errors. They also result in the input voltage being equally shared theoretically. From Fig. 3, the duty ratios of the individual modules can be expressed as follows:

$$\begin{cases} d_1 = d_v + d_{sh\_1} \\ d_2 = d_v + d_{sh\_2} - d_{sh\_1} \\ \cdots \\ d_j = d_v + d_{sh\_j} - d_{sh\_j-1} \\ \cdots \\ d_{n-1} = d_v + d_{sh\_n-1} - d_{sh\_n-2} \\ d_n = d_v - d_{sh\_n-1} \end{cases} \tag{3}$$

According to (2), if the input current $i_j$is smaller than i_{j+1}, the input voltage v_j becomes larger than v_{j+1}, where j is an arbitrary number of the module. Then the integration of $i_j - i_{j+1}$ is smaller than 0. The output of the input voltage sharing compensator network d_{sh_j} increases. According to (3), the duty ratio of module #j increases, whereas the duty ratio of module #j+1 decreases. As a result, the input voltage v_j decreases while v_{j+1}increases. Then the input voltages of the neighboring modules are regulated to be equal. In this way, the input voltage is shared equally among all of the converters and a power balance of the modules is obtained. As can be seen, the input voltages can be reconstructed by the input currents and the electric isolation requirement is avoided.

III. Simulation Results and Experiments for a Two-module ISOP Converter System

A. Two Module System of Proposed Control Strategy

A power circuit of the ISOP configuration is shown in Fig. 4. The schematic is made up of two full bridge dc-dc converters. In this configuration, the input voltage V_{in} is

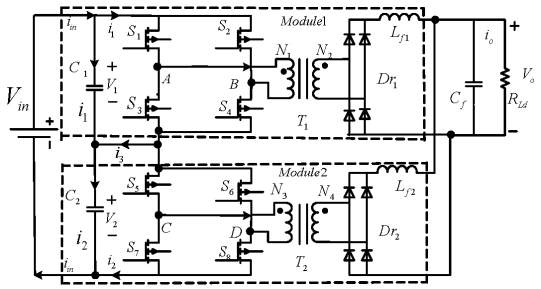

Fig. 4. ISOP connected two full bridge dc-dc converters.

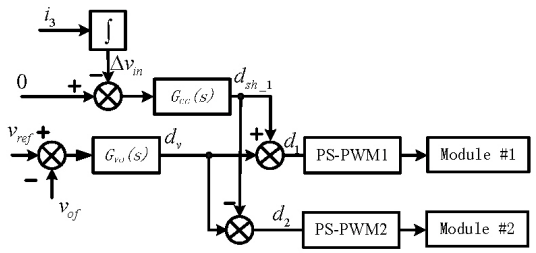

Fig. 5. Control strategy of the two modules.

divided by the input capacitors C_{d1} and C_{d2}. According to (2), the difference in the input voltage can be obtained by the integration of i_1-i_2. As can be seen from Fig. 3, the current i_3 is equal to i_1-i_2. Therefore, only one current sensor and one voltage sensor for sensing the output voltage are needed to complete the control strategy. The implementation of the control strategy for the two ISOP connected full bridge dc-dc modules can be seen in Fig. 5. It should be pointed out that the control strategy is effective only when the two input dividing capacitors have almost the same capacitive value. Otherwise, (2) cannot be satisfied and IVS cannot be ensured.

B. The Simulation Results of the Two Modules

The simulation result for the configuration is shown in Fig. 6. In order to test the effectiveness of the proposed control strategy, the turns-ratios of the two transforms are intentionally chosen to be different. The turns ratio for the transformer of module #1 is 9:1, while that for module #2 is 4.5:1. The rated input voltage V_{in} is $500V$. The output voltage of the system is $20V$. To test the effect of selecting different compensator networks, the system performance under different compensator networks can be analyzed. When the output voltage compensator and the input voltage compensator are selected as: $G_{vo}(s)$=2+30000/s and $G_{cc}(s)$=1+5000/s, the simulation results are as shown in Fig. 6 (a). As can be seen, the input voltage is not shared equally during the starting up process. However, IVS can be achieved finally and the system is stable under the steady state. When the output voltage compensator is kept unchanged and $G_{cc}(s)$=1.1+5500/s, the simulation results are as shown in Fig. 6 (b). As can be seen, the transient performance is improved, but individual input voltages begin to oscillate and the stability of the system is affected. When the output voltage compensator is kept unchanged and $G_{cc}(s)$=1.25+6250/s, the simulation results are as shown in Fig. 6 (c). As can be seen, the system is unstable. Therefore, the gain of the PI regulator for the input voltage sharing loop should be selected with appropriate proportional

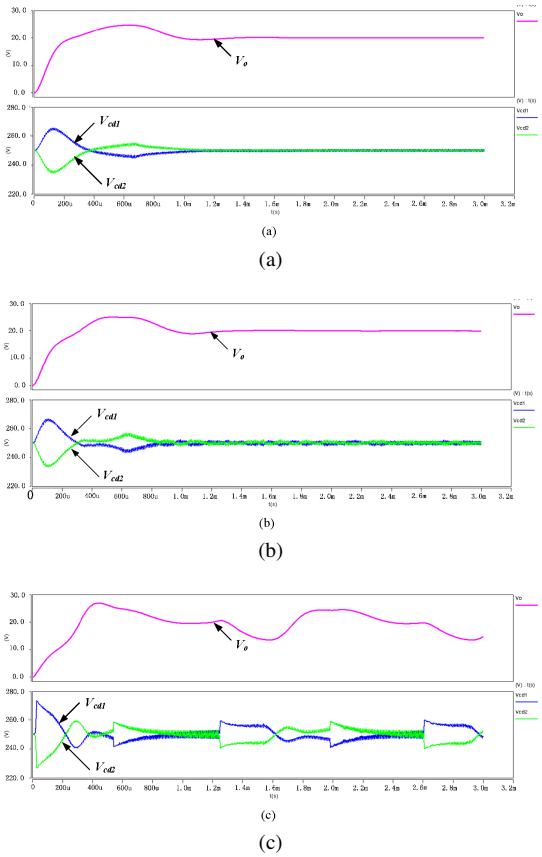

Fig. 6. Simulation result with different $G_{CC}(s)$.

and integral coefficients. The system may become unstable with larger proportional and integral coefficients.

C. Experiment Configuration for Proposed Control Strategy

The digital control is implemented in the experiment. A TMS320F2812 digital processor is chosen to generate PWM signals and control signals. In order to control the two phase-shift, the control system needs at least three pairs of complementary PWM signals. The phase-shift PWM signals are generated by the DSP. As shown in Fig. 7, $CMPR_1$, $CMPR_2$ and $CMPR_3$, which are the values of compare registers, are compared with a triangular carrier waveform to generate PWM_1 and PWM_2, PWM_3 and PWM_4, and PWM_5 and PWM_6 individually. The values of the compare registers are updated once an underflow or period interrupt occurs in the DSP.

General-Purpose Timer 1 works in up and down courting modes. When General-Purpose Timer 1 is working in up courting mode:

$$CMPR_1 = 0,\ CMPR_2 = TP1 - d_1,\ CMPR_3 = TP1 - d_2 \quad (4)$$

while General-Purpose Timer 1 is working in down courting mode:

$$CMPR_1 = TP1,\ CMPR_2 = d_1,\ CMPR_3 = d_2 \quad (5)$$

where d_1 and d_2 are the inputs for generating duty cycles, respectively, as can be seen in Fig. 5. $TP1$ is the value of Timer 1. As can be seen in Fig. 4 and Fig. 7, the switching of S1 and S5 are driven by PWM_1; the switching of S3 and S7

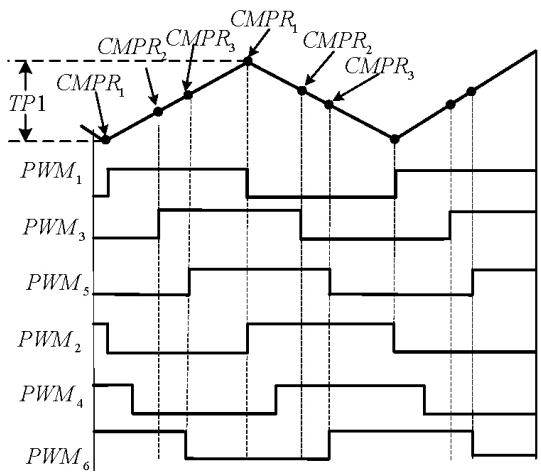

Fig. 7. Schematic of digital PWM generation.

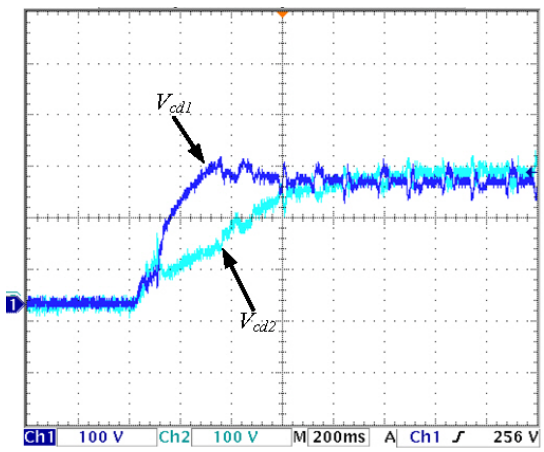

Fig. 8. Response of the input voltage when the system starts up.

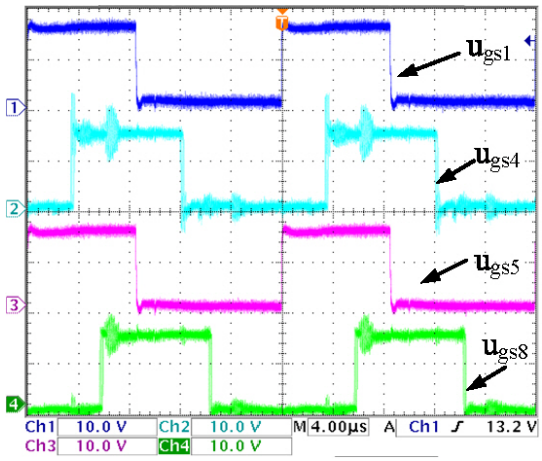

Fig. 9. PWM signals of S1, S4, S5 and S8.

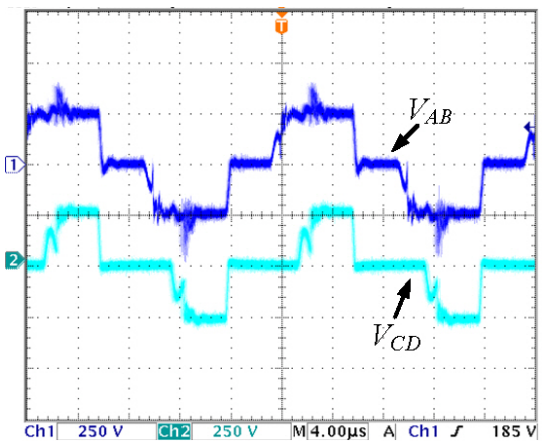

Fig. 10. Waveform of the primary voltages of the two transformers.

are driven by PWM_2; the switching of S2 is driven by PWM_4; the switching of S4 is driven by PWM_3; the switching of S8 is driven by PWM_5; and the switching of S6 is driven by PWM_6.

D. Experiment Results

Fig. 8 to Fig. 11 show the experiment results of the proposed control strategy. The input voltage is 500V. The output voltage is 20V. The rated load is 2Ω. The main factor, which causes the mismatch of the modules, is the turns-ratio of the transformers. In order to verify the effectiveness of the control strategy, it should be noted that the turns-ratios of the two HF transformers are intentionally selected to be different. The turns-ratio of the transformer in module #1 is 9:1, while that in module #2 is 4.5:1. Fig. 8 shows the input voltages during starting up. Due to the mismatch of the two transformers, the input voltages of the two modules are not shared equally. Finally, with the proposed control strategy, the input voltage is shared equally between the two modules under the steady state.

Fig. 9 and Fig. 10 show the PWM signals and the primary voltages of the power transformers under the steady state. The input voltages are in proportion to the turns-ratios of the individual modules for the ISOP converter, when the duty ratios of all the modules are the same [6]. Therefore, the duty ratios of all the modules are in proportion to the turns-ratios, when the input voltages achieve equal sharing. As can be seen in Fig. 9 and Fig. 10, the duty ratio of module #1 is two times larger than that of module #2, because the ratio of the turns-ratios for the two transformers is approximately 2 to 1. Moreover, as can be seen in Fig. 10, the amplitudes of the two waveforms are equal, which illustrates that the input voltages of the two modules are shared equally.

Fig. 11 shows the individual input voltages and the filter inductor currents corresponding to the step change load. Despites the transients, the total input voltage can be shared equally fairly well. The output current can be shared when the input voltage is shared for the ISOP converter [4].

IV. Conclusions

A control strategy for ISOP converters with power balance is proposed. The input voltage difference can be reconstructed by calculating the difference in the input current for neighboring modules, which simplifies the design and lowers the cost. The problem of electric isolation is avoided when measuring the input voltages. The control strategy is suitable for two modules and for multiple modules. The effectiveness of the novel control strategy is verified by means of a 200W prototype.

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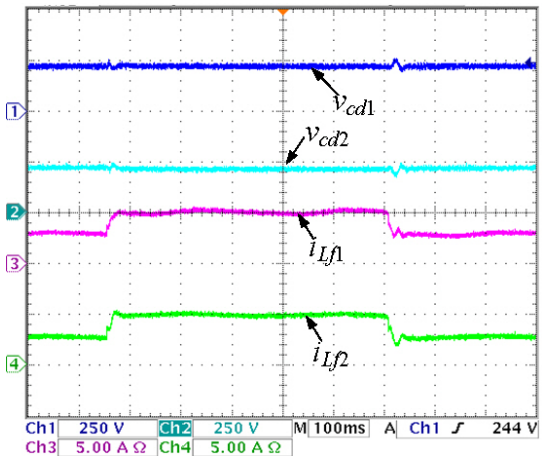

Fig. 11. Individual input voltages and output filter inductor currents of during the step change load.

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