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Direct Duty-ratio Modulated Fault-tolerant Strategy for Matrix Converter-fed Motor Drives

Yulong Li*, Nam-Sup Choi†, Byung-Moon Han**, and Eui-Cheol Nho***

* Division of Electro Electric Systems, Hyundai Heavy Industries Co., LTD., Gunsan, Korea
† Division of Electric., Electron. Communication & Computer Eng., Chonnam National University, Yeosu, Korea
** Dept. of Electrical Eng., Myongji University, Yongin, Korea
*** Dept. of Electrical Eng., Pukyong National University, Busan, Korea

Abstract

Direct duty-ratio PWM schemes for continuous fault tolerant operation of matrix converter-fed motor drives are presented. The proposed method features simple modular modulation structure based on per output phase concept, which requires no additional modification on the normal modulation schemes for fault-tolerant applications. Realizations of fault-tolerant strategy applied to different system configurations are also treated to enhance the system flexibility. The proposed method can be effectively applied to treat the motor open phase fault and converter switching device failure. Simulation and experimental results show the feasibility and validation of the proposed strategies.

Key Words: Fault-tolerant, Matrix converter, Motor drive, PWM

I. Introduction

Developments in modern power electronics technology significantly stimulate the industrial application of adjustable speed drives (ASDs). With the increasing requests for more stable and reliable solution of ASDs in industrial application, continuous fault-tolerant operation of ASDs are more and more studied and investigated. Nowadays, ASDs with the configuration of AC/DC/AC back-to-back converters are still popularly used in practical application. Fault-tolerant modulation schemes based on the AC/DC/AC back-to-back converters have been well treated. Early works have been reviewed in [1] and [2] to present the analysis, modeling and simulation of various inverter and machine faults. Then, a two-phase operation mode was proposed in [3] by connecting the motor stator winding neutral point to the dc voltage source. In [4], when a converter leg is lost, an utilization topology with a fourth converter leg connecting to machine neutral permits the fault-tolerant operation of a three-phase induction motor drive. In [5] and [6], the authors make very good comparison of different fault-tolerant strategies in order to perform comparison of the features, implementation costs and performance limitations.

Meanwhile, there have also been increasing interests to improve the features for the ASDs such as bidirectional power flow, compact size, no integration of large energy storage components and so on. In principle, the matrix converter can fulfill these requirements based on an all-silicon solution.

Matrix converter is a direct AC-AC converter which consists of an array of bidirectional switches to provide an AC load with desired AC voltages from AC input source voltages. The matrix converter can be applied to variable power conversion, AC drive and renewable power generation [7], [8]. Various methods to modulate the bidirectional switches of the matrix converter have been presented in many works. Examples are the Venturini method [9], space vector PWM method [10] and carrier based modulation method in [11].

Recently, the matrix converter has been penetrating considerable interests in AC/AC converting application. Then the similar fault-tolerant algorithms can be immigrated from AC/DC/AC converter to matrix converter. Kwak's study, including [12]-[14], dealt with the fault-tolerant matrix converter drive with the additional neutral connection approach and reconfigurable structure method, respectively. Also, the method of detecting fault conditions is investigated in [13]. However, the modulation strategies proposed in [12]-[14] are developed based on the Venturini method [9] and space vector PWM method [10]. The modulation methods needs to be modified a lot in order to perform the fault-tolerant control and thus are far from intuitive to understand and difficult to implement it. Other works [15], [16] are presented based on space vector PWM method and the carrier based modulation method.

Previous works dedicated to fault-tolerant operation of matrix converter-fed motor drives imply complex modulation

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Recommended for publication by Associate Editor Kyo-Beum Lee.
† Corresponding Author: nschoi@chonnam.ac.kr
Tel: +82-61-659-7311, Fax: +82-61-659-7319, Chonnam Nat'l University
* Division of Electro Electric Systems, Hyundai Heavy Industries Co., LTD., Korea
** Dept. of Electrical Eng., Myongji University, Korea
*** Dept. of Electrical Eng., Pukyong National University, Korea

scheme under faulted condition. These methods are also lack of generality and can't be simply applied to different system configurations.

This paper proposes a direct duty-ratio pulse width modulation (DDPWM) method [17], [18] to implement the fault-tolerant strategy for a three-phase matrix converter-fed motor drive. The DDPWM method features modular modulation structure for each output phase. Thus, nothing in the modulation strategy needs to be modified when the matrix converter transfers to fault operation, only the converter output commands have to be properly given. Therefore, the DDPWM can be very effectively and simply applied to realize the fault-tolerant control algorithm.

With help of DDPWM modulation technique, different system re-configuration under fault case will be investigated. At first, the configuration of additional connection between output and input neutral will be dealt with. Then the solution by adding a redundancy leg will be treated under both converter failure and motor winding failure. Simulation and experimental results are provided to show the validity and feasibility of the proposed method.

This paper is organized as follows. The basis of DDPWM method will be revised in Section II. Section III to V will present three different fault-tolerance system configurations of matrix converter, with simulation results. Then experimental results will be provided in Section VI. Finally, some conclusions are given in Section VII.

II. Review of DDPWM Method

The authors proposed DDPWM modulation method in [17], [18]. Fig. 1 shows the circuit configuration with the three-phase input voltages, input filter, a three-phase matrix converter and an inductive load. This is the normal configuration of the three-phase to three-phase AC-AC matrix converter. By properly switching the 3 by 3 bidirectional switches on and off, desired output with variable magnitude and variable frequency can be generated at the output terminals, where i_{oA}, i_{oB}, i_{oC} and v_{oA}, v_{oB}, v_{oC} are output currents and output voltages under normal operation.

A switching period T_s is divided into two time periods, T_1 and T_2. Also, *MX*, *MD* and *MN* denote the maximum, medium and minimum input voltage values, respectively. During T_1, the line-to-line voltage between *MX* and *MN*, which is the maximum line-to-line voltage among three line-to-line input voltages at the sampling instant, is used. During T_2, the second maximum line to line voltage, which is the larger one in *MX* to *MD* and *MD* to *MN*, is used. If *MX-MD* > *MD-MN*, *MX* to *MD* is used during T_2 and the resultant switching pattern is named switching pattern-I. Otherwise, *MD* to *MN* is used during T_2, namely switching pattern-II.

Switching pattern-I: Fig. 2 shows switching pattern-I for generating *A*-phase output voltage where a triangular carrier is compared with a duty ratio value, d_{A1}, resulting in output phase voltage changed like *MN*→*MX*→*MD*. As seen in Fig. 2, *MN*, *MX*, *MX* and *MD* appear at *A*-phase output terminal

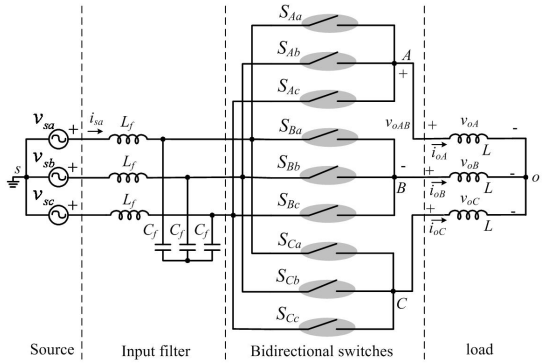

Fig. 1. System configuration with matrix converter.

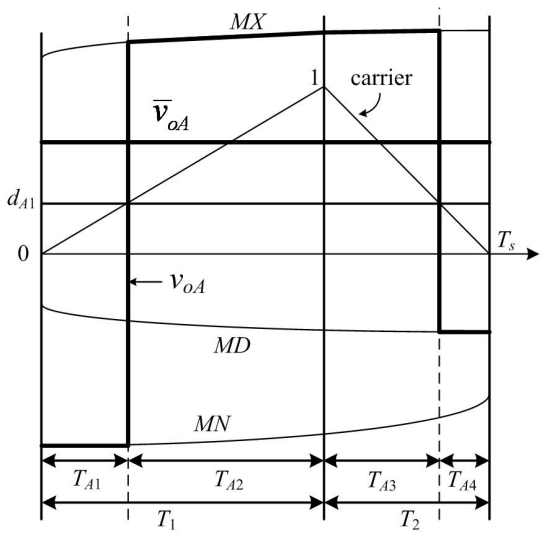

Fig. 2. Switching state in the case of switching pattern-I.

during T_{A1}, T_{A2}, T_{A3} and T_{A4} respectively. The four sub-intervals can be expressed as

$$\begin{aligned} T_{A1} &= d_{A1} n T_s \\ T_{A2} &= (1-d_{A1})\, n T_s \\ T_{A3} &= (1-d_{A1})\,(1-n)\, T_s \\ T_{A4} &= d_{A1}\,(1-n)\, T_s \end{aligned} \tag{1}$$

where d_{A1} is the *A*-phase duty ratio value when switching pattern-I is applied and n is defined by $n = T_1/T_s$ which involves the slope of the carrier.

Supposing that the input voltages are almost constant during switching cycles, the integration of output voltage v_{oA} over T_s can be written to be

$$\int_0^{T_s} v_{oA}\, dt \;\cong\; T_{A1}\cdot MN + (T_{A2}+T_{A3})\cdot MX + T_{A4}\cdot MD. \tag{2}$$

Then, it is found from (1) and (2) that the averaged value of v_{oA}, $\bar{v}_{oA}$, can be approximated by

$$\bar{v}_{oA} = \frac{1}{T_s}\int_0^{T_s} v_{oA} dt \cong d_{A1}\,(n\cdot MN - n\cdot MD + MD - MX) + MX. \tag{3}$$

By letting $\bar{v}_{oA}$ be equal to the *A*-phase output voltage command, v_{oA}^*, that is $\bar{v}_{oA} = v_{oA}^*$, then the duty ratio value, d_{A1}, for the present switching period can be calculated as

$$d_{A1} = \frac{MX - v_{oA}^*}{(MX-MD) + n\,(MD-MN)}. \tag{4}$$

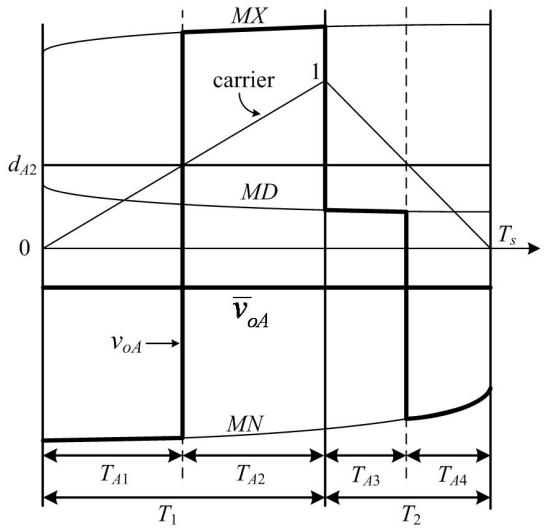

Fig. 3. Switching state in the case of switching pattern-II.

Switching pattern-II: In the same way, switching pattern-II can be analyzed. Fig. 3 shows the switching pattern-II for generating *A*-phase output voltage where a triangular carrier is compared with a duty ratio value, d_{A2}. The time intervals such as T_{A1}, T_{A2}, T_{A3} and T_{A4} are the same as in equation (1) and the output phase voltage is changed with the sequence of $MN \rightarrow MX \rightarrow MD \rightarrow MN$. In this case, the averaged value of v_{oA}, $\bar{v}_{oA}$, can be approximated by

$$\begin{aligned}\bar{v}_{oA} &= \frac{1}{T_s}\int_0^{T_s} v_{oA}\,dt \\ &\cong d_{A2}\cdot(MN - n\cdot MX - MD + n\cdot MD) + n\cdot MX - n\cdot MD + MD.\end{aligned} \tag{5}$$

Again, by letting $\bar{v}_{oA}$ be equal to the *A*-phase output voltage command, v^*_{oA}, the duty ratio value, d_{A2}, can be obtained as

$$d_{A2} = \frac{n(MX - MD) + (MD - v^*_{oA})}{n(MX - MD) + (MD - MN)}. \tag{6}$$

In summary, the duty ratio value d_A for *A*-phase at each switching cycle is determined by (7). The other two output phases can be treated in exactly the same way.

$$d_A = \begin{cases} \dfrac{MX - v^*_{oA}}{(MX - MD) + n(MD - MN)} & \text{if } (MX - MD) \geq (MD - MN) \\ \dfrac{n(MX - MD) + (MD - v^*_{oA})}{n(MX - MD) + (MD - MN)} & \text{if } (MX - MD) < (MD - MN). \end{cases} \tag{7}$$

Due to the per-phase modular structure, the DDPWM method has good applicability and flexibility. Therefore, this method can be easily applied to various fault-tolerant strategies. Only task for the fault-tolerant controller will be to properly assign the output commands under fault condition. Then without any changes in modulation method itself, the DDPWM is able to modulate desired output variables. This attractive feature greatly increases the system flexibility and generality. Large part of the works in [12]-[16] are focusing on developing new modulation strategies for the fault condition. Such solutions not only increase system complexity by assigning controller much more works, but also are lack of generality, which means new modulation schemes have to be found once the system configuration is changed.

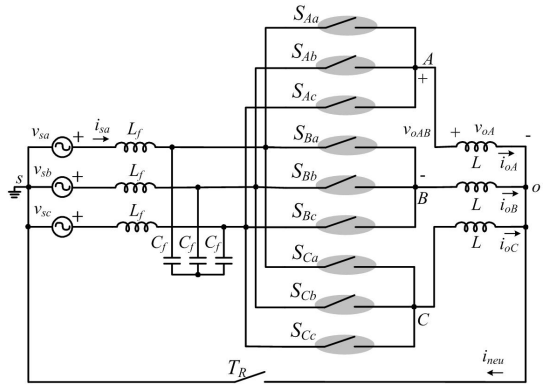

Fig. 4. Reconfiguration with neutral connection.

III. Re-configuration with Neutral Connection

A. Reconfigurable Structure with Neutral Connection

The system configuration in Fig. 1 can be modified to cope with fault situations as shown in Fig. 4. In Fig. 4, an additional connection is provided between the load neutral point and input voltage neutral by help of T_R. T_R should be active switch and capable of allowing bi-directional current flow, thus can be type of a TRIAC or a pair of commercial IGBT module. Under normal operation, T_R is off and the matrix converter will control the output voltage/current to drive the load [12].

This configuration will allow fault-tolerant operation when the system has an internal fault which means fault open at one of the matrix converter switches, or an external fault which means fault of motor open winding. Under such fault condition, the 3 bidirectional switches at the faulted phase will be forced off, leading to a single-phase open circuit at the faulted phase. Then other two healthy phases should be operating in such a way that the matrix converter can maintain the rotating flux in the motor load. Meanwhile, T_R will be turned on to conduct unbalanced load current to the input source neutral.

The modulation target under fault case will be to maintain the rotating flux by the two un-faulted phases. This is done by regulating these two phase currents with the magnitude increased by a factor of $\sqrt{3}$ and the phase shifted by 30? away from the axis of the faulted phase [4]-[6]. The principle can be illustrated by Fig. 5. Fig. 5(a) shows the system configuration when a *C*-phase fault happens. *C*-phase connected parts inside the converter and *C*-phase winding of the load will be isolated. At the same time, T_R will be on. After the event of fault condition detection, the control task is shown in Fig. 5(b) and Fig. 5(c) by the phasor diagram. Letting i_{oAf}, i_{oBf} and v_{oAf}, v_{oBf} are the vectors under fault operation, and φ is the angular difference between output current and voltage. Clearly, it can be obtained that in case of *C*-phase fault, the output voltage commands in normal operation and fault operation will be (8) and (9), respectively.

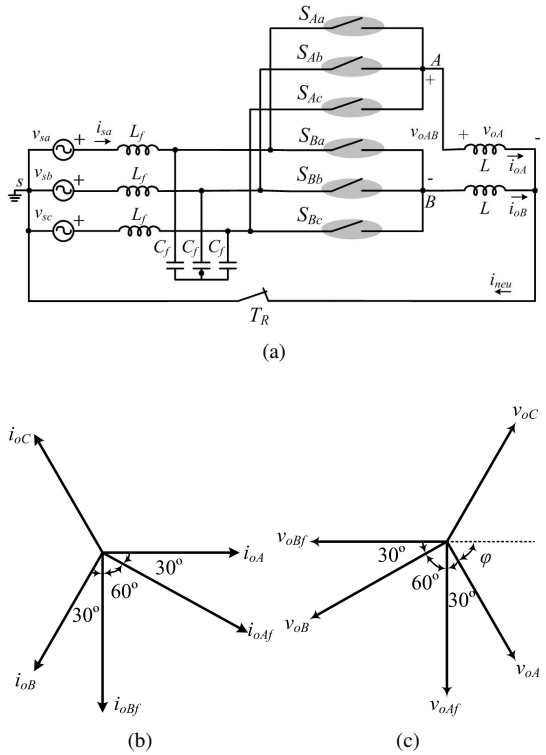

Fig. 5. (a) Operating circuit of Fig. 4 under *C*-phase fault. (b) Current phasor diagram in normal operation and under *C*-phase fault. (c) Voltage phasor diagram in normal operation and under *C*-phase fault.

$$\begin{aligned} v^*_{oA} &= V_o \sin(2\pi f_o t) \\ v^*_{oB} &= V_o \sin\left(2\pi f_o t - {}^{2\pi}/_{3}\right) \\ v^*_{oC} &= V_o \sin\left(2\pi f_o t + {}^{2\pi}/_{3}\right) \end{aligned} \tag{8}$$

$$\begin{aligned} v^*_{oAf} &= V_o \sin\left(2\pi f_o t - {}^{\pi}/_{6}\right) \\ v^*_{oBf} &= V_o \sin\left(2\pi f_o t - {}^{\pi}/_{2}\right) \\ v^*_{oCf} &= 0 \end{aligned} \tag{9}$$

where the superscript symbol '*' indicates that the variables are given as commands.

It can be directly figured out from the re-configuration in Fig. 4 that such system will require the possible access to the neutral points of the load and input voltage source. Otherwise, the additional neutral connection will not be possible. Such features put additional limitations on the system. For example, this solution will not fit for a delta winding motor, or a star winding motor without external access to the neutral point, or a delta connected transformer at the input side.

This configuration also limits the voltage transfer ratio q, which is defined as output voltage magnitude over input voltage magnitude. Under faulted case, the output neutral will be clamped to input neutral, making the normal harmonic injection modulation technique [9] for matrix converter unavailable. Then q will be limited to be 0.5. Considering that the magnitude of the un-faulted phase should be enlarged by $\sqrt{3}$ under fault operation, then q for normal operation will be $0.5/\sqrt{3}$, which will become a dramatic shortcoming of this solution. On the contrast, the reconfiguration in Fig. 4 is very simple and only requires one additional connecting device T_R, making this solution economically competitive.

TABLE I
SIMULATION PARAMETERS

R-L load	R=10Ω, L=10mH
Voltage transfer ratio	q=0.5
Input voltage (line-to-line RMS) V_{s-RMS}	220V
Output voltage (line-to-line RMS) V_{o-RMS}, normal operation	63.5V
Output voltage (line-to-line RMS) V_{of-RMS}, fault operation	110V
Input frequency f_s	60Hz
Output frequency f_o	30Hz

B. Simulation Results

By the parameters listed in Table I, the output voltage references under normal operation and fault condition can be easily found to be

$$\begin{aligned} v^*_{oA} &= 55 \cdot \sin(60\pi t) \\ v^*_{oB} &= 55 \cdot \sin\left(60\pi t - {}^{2\pi}/_{3}\right) \\ v^*_{oC} &= 55 \cdot \sin\left(60\pi t + {}^{2\pi}/_{3}\right) \end{aligned} \tag{10}$$

$$\begin{aligned} v^*_{oAf} &= 90 \cdot \sin\left(60\pi t - {}^{\pi}/_{6}\right) \\ v^*_{oBf} &= 90 \cdot \sin\left(60\pi t - {}^{\pi}/_{2}\right) \\ v^*_{oCf} &= 0. \end{aligned} \tag{11}$$

The simulation results are shown in Fig. 6. Fig. 6 shows the output line-to-line voltage v_{oAB}, *A*-, *B*-, *C*-phase output currents i_{oA}, i_{oB}, i_{oC}, and neutral connecting current i_n. Output voltage references are also given in Fig. 6. It can be seen from the simulation results that as soon as the *flag* signal triggers fault-tolerant operating mode, the output *A*- and *B*- phase are well modulated with the scheme shown in Fig. 5(b).

The output C-phase is open immediately and neutral connection starts to conduct the unbalance load currents. Therefore, it can be said that the proposed DDPWM method is able to well synthesize the output voltages under both normal operation and fault-tolerant operation.

IV. RE-CONFIGURATION AT CONVERTER OUTPUT TERMINALS

A. Reconfigurable structure with neutral connection at converter output terminal

The system re-configuration with neutral connection of input source can also be done in the way shown in Fig. 7. The system configuration requires three additional connecting devices between the converter output terminal and input voltage neutral, T_{RA}, T_{RB} and T_{RC} [13]. With help of these three auxiliary connecting devices, any of the three output phase can be connected to the input voltage neutral. In case that an open switch fault at the converter happens, all the switches tied to the faulted phase will be open and the corresponding connecting device T_R at that phase will be turned on to bypass the load current through the connection to input neutral.

An example is also given in Fig. 8 in the case of *C*-phase failure. With the case in Fig. 8, load terminal *C* is directly connected to input neutral, causing the terminal voltage clamped to zero. The voltage difference between normal operation and fault-tolerant operation will be $-V^*_{oc}$. Then by reflecting this $-V^*_{oc}$ to the other healthy phases, the three-phase load current

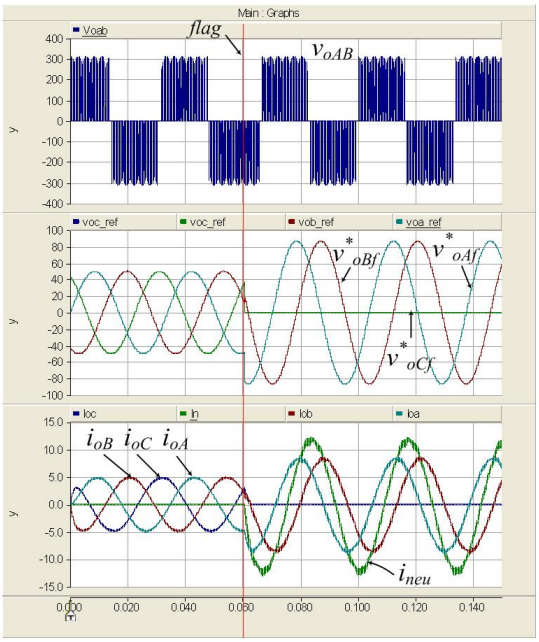

Fig. 6. Simulation results of Fig.5 operation.

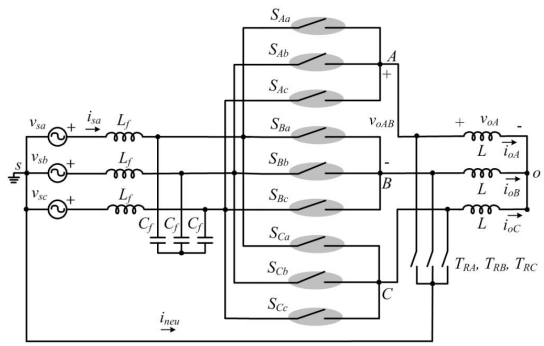

Fig. 7. Reconfiguration at converter output terminals.

will be maintained. Output A- and B-phase voltage references can be calculated to be

$$\begin{aligned} v^*_{oAf} &= V^*_{oA} + \left(-V^*_{oC}\right) \\ v^*_{oBf} &= V^*_{oB} + \left(-V^*_{oC}\right) \\ v^*_{oCf} &= 0. \end{aligned} \tag{12}$$

Eq. (12) shows the same effect as in Fig. 5(b) to regulate these two phase voltages with the magnitude increased by a factor of $\sqrt{3}$ and the phase shifted by 30? away from the axis of the faulted phase.

The system reconfiguration with additional neutral connection at converter output terminal can be compared with the solution by connecting the output and input neutrals. It can be directly figured out that there will be no need to access to the load neutral point, thus increasing the system adaptiveness. Meanwhile, the available voltage transfer ratio q can't be enlarged compared with the solution to connect the output and input neutrals. This is because the C-phase load terminal is equal to input neutral voltage. If introducing an offset voltage to the output neutral, this voltage is not cancelled between A- and C-phase, neither is the case between B- and C-phase. As a result, the induced offset voltage will cause distortion to the load currents.

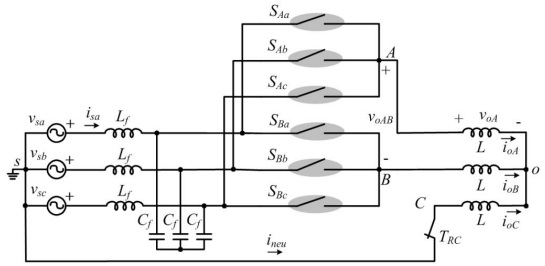

Fig. 8. Operating circuit of Fig. 7 under C-phase fault.

TABLE II
SIMULATION PARAMETERS

R-L load	R=10Ω, L=10mH
Voltage transfer ratio	q=0.5
Input voltage (line-to-line RMS) V_{s-RMS}	220V
Output voltage (line-to-line RMS) V_{o-RMS}, normal operation	63.5V
Output voltage (line-to-line RMS) V_{of-RMS}, fault operation	110V
Input frequency f_s	60Hz
Output frequency f_o	30Hz

The shortcomings of the re-configuring method described in this section will be requirement of more auxiliary connecting devices and access of input neutral point. Moreover, this method will not be suitable to deal with the open circuit fault from the load.

B. Simulation Results

A simulation by PSCAD/EMTDC of the reconfigured matrix converter in Fig. 8 is performed. The switching period T_s is 100 μs, and other simulation parameters are shown in Table II.

The output voltage references under normal operation and fault condition in (8) and (12) can be found to be

$$\begin{aligned} v^*_{oA} &= 55 \cdot \sin\left(60\pi t\right) \\ v^*_{oB} &= 55 \cdot \sin\left(60\pi t - {}^{2\pi}/_{3}\right) \\ v^*_{oC} &= 55 \cdot \sin\left(60\pi t + {}^{2\pi}/_{3}\right) \end{aligned} \tag{13}$$

$$\begin{aligned} v^*_{oAf} &= 90 \cdot \sin\left(60\pi t - {}^{\pi}/_{6}\right) \\ v^*_{oBf} &= 90 \cdot \sin\left(60\pi t - {}^{\pi}/_{2}\right) \\ v^*_{oCf} &= 0. \end{aligned} \tag{14}$$

The simulation results are shown in Fig. 9. Fig. 9 shows the output line-to-line voltage v_{oAB}, A-, B-, C-phase output currents i_{oA}, i_{oB}, i_{oC}. Output voltage references are also given in the figure. It can be seen from the simulation results that as soon as the *flag* signal triggers fault-tolerant operating mode, the output A- and B- phase are well modulated to maintain the three-phase balance load currents.

V. RE-CONFIGURATION WITH AN ABUNDANCE LEG

A. Reconfigurable structure with an abundance leg to output neutral

Both the system re-configurations with neutral connection of input source clearly imply the restrain on connectivity of neutral point of the input source. In order to overcome this problem, the system re-configuration in Fig. 10 shows the solution with an abundance output leg.

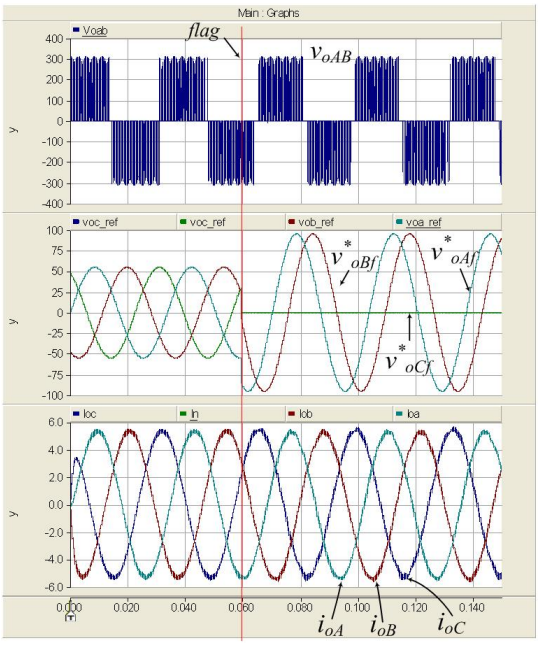

Fig. 9. Simulation results of Fig.8 operation.

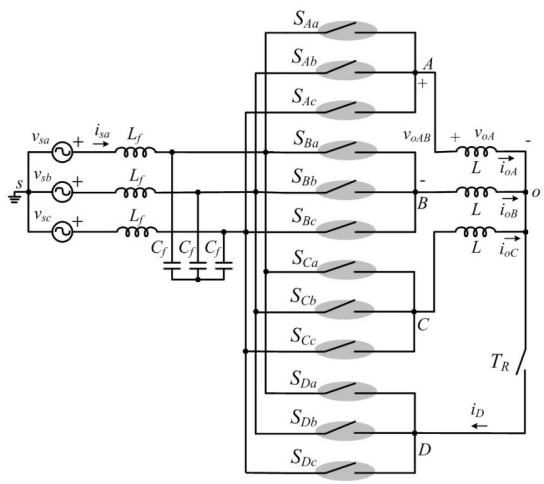

Fig. 10. Reconfiguration with an abundance leg to load neutral.

In case of an open switch fault happening inside the converter or an open winding fault occurring internal the load, the load neutral point can be connected to the fourth abundance leg to allow unbalanced current.

Compared with the configuration shown in Fig. 4, the reconfiguration in Fig. 10 also requires one auxiliary connecting device T_R. However, the abundance leg will cost another 3 bidirectional switches, making this solution relatively expensive. The advantages of the solution of Fig. 10 will be that load can be separated from source voltages without any direct neural connection even under fault-tolerant operation. As a result, there will be no need for the system to access input neutral point, making this system more flexible. Another important advantage of the configuration of an additional leg will be enlarged voltage conversion ratio by $\sqrt{3}$. This is because voltage potential of the load neutral point can be controlled by the converter. Then the method of introducing an offset voltage can be applied.

Determination of an inserted offset voltage to the output

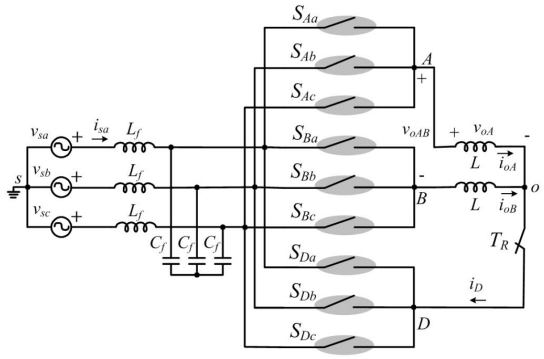

Fig. 11. Operating circuit of Fig. 10 under *C*-phase fault.

neutral has been well investigated in [9], [17]-[18]. The output voltage reference equation sets of (8) and (9) can be determined as (15) and (16), respectively.

$$\begin{aligned} v^*_{oA} &= V_o \sin(2\pi f_o t) + v_{off} \\ v^*_{oB} &= V_o \sin\left(2\pi f_o t - {}^{2\pi}/_{3}\right) + v_{off} \\ v^*_{oC} &= V_o \sin\left(2\pi f_o t + {}^{2\pi}/_{3}\right) + v_{off} \\ v^*_{oD} &= 0 \end{aligned} \tag{15}$$

$$\begin{aligned} v^*_{oAf} &= V_o \sin\left(2\pi f_o t - {}^{\pi}/_{6}\right) + v_{off} \\ v^*_{oBf} &= V_o \sin\left(2\pi f_o t - {}^{\pi}/_{2}\right) + v_{off} \\ v^*_{oCf} &= 0 \\ v^*_{oDf} &= v_{off} \end{aligned} \tag{16}$$

where v_{off} stands for the offset voltage and is expressed as

$$v_{off} = -\frac{\sqrt{6}}{12} V_{s-RMS} \sin(6\pi f_s t) + \frac{1}{6} V_o \sin(6\pi f_o t). \tag{17}$$

Fault-tolerance structure under *C*-phase open circuit is illustrated in Fig. 11. It can be directly found out that the converter system will change from the normal three-phase to three-phase configuration into a three-phase to two-phase three-leg topology. The control methodology will be the same as illustrated in Fig. 5(b). The two healthy phases are modulating voltages as determined by (16). Then the additional leg will conduct unbalanced load current. DDPWM is able to control such a two-phase three-leg matrix converter very effectively [18].

B. Simulation Results

Simulation results obtained by PSCAD/EMTDC for the reconfigured matrix converter in Fig. 11 are given in Fig. 12. The simulation parameters are shown in Table III. The simulation results in Fig. 12 show that the DDPWM method can effectively control the matrix converter of Fig. 11 in fault-tolerant operation with maximum voltage transfer ratio of 0.866.

VI. Experimental Works

A. Experimental Setup

To verify the feasibility of the proposed fault-tolerant methods, an experimental setup was built and the DDPWM controller was implemented by using TMS320VC33 DSP from Texas Instruments and Altera CPLD of EP1K100QC208-1.

TABLE III
SIMULATION PARAMETERS

R-L load	R=10Ω, L=10mH
Voltage transfer ratio	q=0.866
Input voltage (line-to-line RMS) V_{s-RMS}	220V
Output voltage (line-to-line RMS) V_{o-RMS}, normal operation	110V
Output voltage (line-to-line RMS) V_{of-RMS}, fault operation	190V
Input frequency f_s	60Hz
Output frequency f_o	30Hz

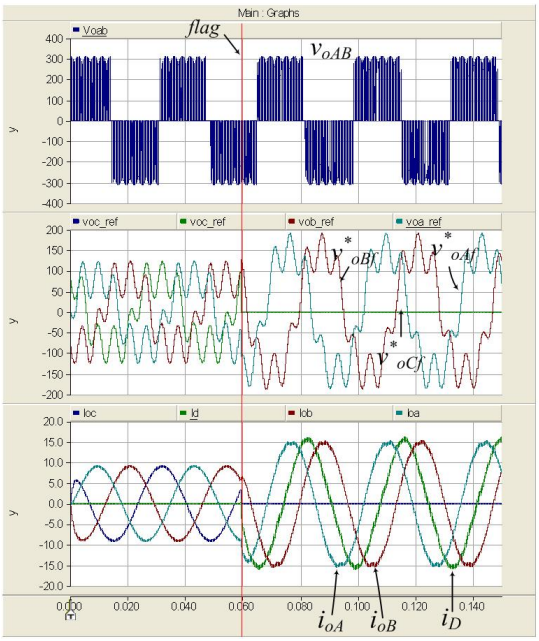

Fig. 12. Simulation results of Fig.11 when T_R is on.

The matrix converter parameters are given in Table IV. The experimental configuration is shown in Fig. 13. As seen in Fig. 13, two out of three input line-to-line voltages v_{sab} and v_{sbc} are sensed in order to calculate three input phase voltages v_{sa}, v_{sb} and v_{sc}. Sampled values of v_{sa}, v_{sb} and v_{sc} are then used to implement the required calculation.

B. Experimental Results

Fig. 15 shows the experimental result of the system reconfiguration illustrated in Section 3 (Fig. 6). The experimental conditions are made to be the same with Section 3B. In the same way, Fig. 16 gives the waveforms of the system reconfiguration illustrated in Section 4 (Fig. 8) under condition of Section 4B; Fig. 17 are the waveforms for the system reconfiguration described in Section 5 (Fig. 10) under condition of Section 5B.

The experimental results in Fig. 15 to Fig. 17 show very good accordance with the simulation results. They verify

TABLE IV
MATRIX CONVERTER HARDWARE PARAMETERS

Rated Input voltage (line-to-line RMS) V_{s-RMS}	220V,60Hz
Inductance of input filter L_f	100μH
Capacitance of input filter C_f	60μF
Rated voltage of IGBT	600V
Rated current of IGBT	200A
Switching frequency f_{sw}	10kHz

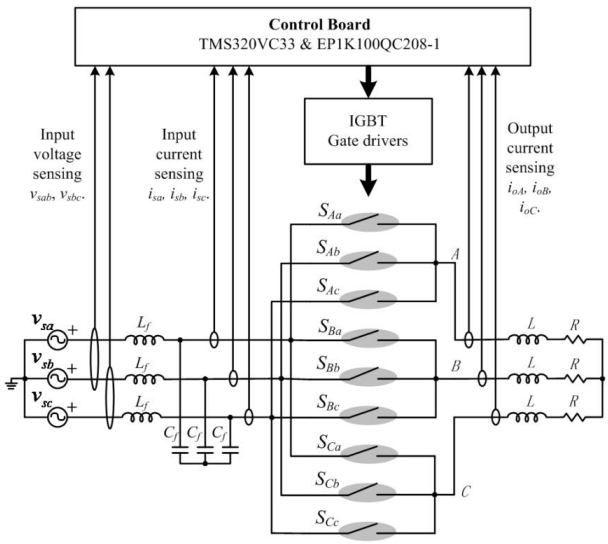

Fig. 13. Configuration of experimental setup.

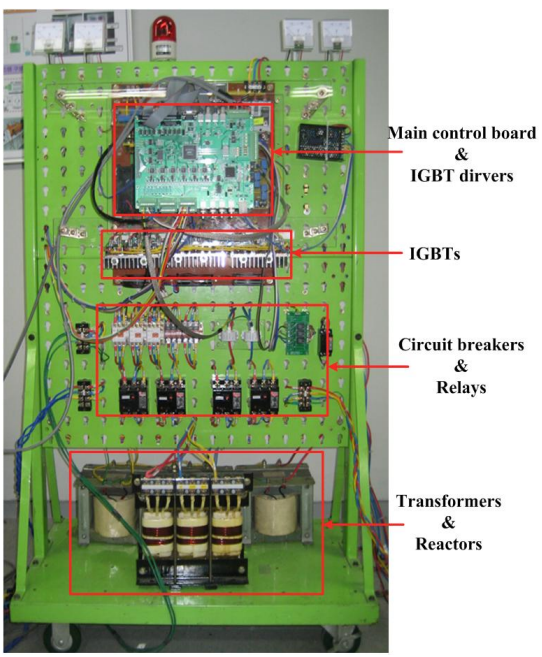

Fig. 14. Picture of experimental setup.

the correct and efficient operation of the proposed DDPWM based fault-tolerant modulation strategy in practical way. It can be seen that under different system reconfiguration, the fault current flows through the provided path to achieve more reliable and stable operation for matrix converter-fed drives.

It is found that, in actual experimental waveforms, there is a time delay between fault occurrence and starting conduction in T_R switch, which is not observed in simulation. This is because practical currents cannot be changed immediately due to large inductance at the output terminals even though the output command of fault conditions is activated.

Input phase locked loop (PLL) is also incorporated into DSP to obtain input voltage angle α_i and to determine the proper switching pattern. Three input phase currents i_{sa}, i_{sb}, i_{sc} are sensed only for protection purpose. Three output phase currents i_{oA}, i_{oB} and i_{oC} are sensed for both control and protection purpose. A picture of the experimental setup is also

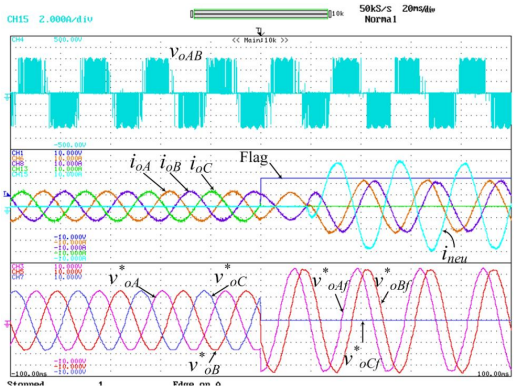

Fig. 15. Experimental results for system reconfiguration in Section 3 (Fig. 5) (v_{oAB}: 100V/div; i_{oA}: 5A/div; i_{oB}: 5A/div; i_{neu}: 5A/div; v^*_{oAf}:50V/div; v^*_{oBf}:50V/div; v^*_{oCf}:50V/div; time base : 20ms/div).

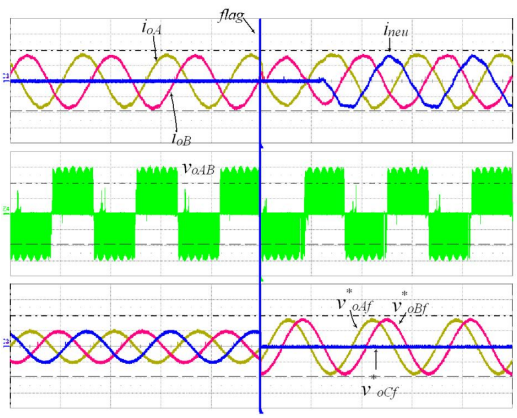

Fig. 16. Experimental results for system reconfiguration in Section 4 (Fig. 8) (v_{oAB}: 100V/div; i_{oA}: 5A/div; i_{oB}: 5A/div; i_{oC}: 5A/div; v^*_{oAf}:50V/div; v^*_{oBf}:50V/div; v^*_{oCf}:50V/div; time base : 20ms/div).

shown in Fig. 14.

VII. Conclusions

This paper applies the DDPWM methodology to fault-tolerant operation for the matrix converter-fed motor drives. By system re-constructed with additional connecting devices T_R or an abundance leg, totally three fault-tolerant configurations are investigated. Thanks to the per-phase modular characteristics of the DDPWM, the DDPWM scheme is able to modulate desired output variables for both normal operation and fault-tolerant operation, without any changes in modulation method itself. Therefore, control system complexity is greatly reduced and modulating task can be easily and effectively performed. A comparison for various kinds of fault-tolerant system re-configurations has also been performed on cost and voltage conversion ratio. The feasibility and validity of the DDPWM operation in different system re-configurations have been verified through simulation and experimental results.

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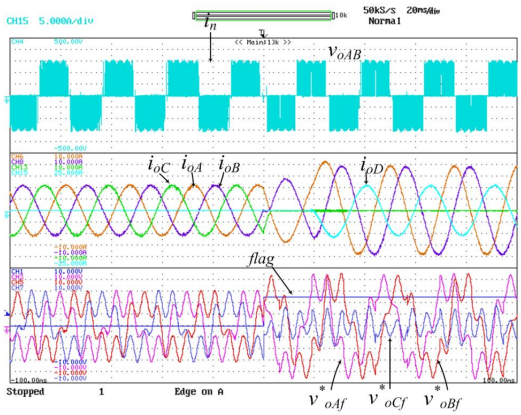

Fig. 17. Experimental results for system reconfiguration in Section 5 (Fig. 11) (v_{oAB}: 100V/div; i_{oA}: 4A/div; i_{oB}: 4A/div; i_{oC}: 4A/div; i_{oD}: 4A/div; v^*_{oAf}:50V/div; v^*_{oBf}:50V/div; v^*_{oCf}:50V/div; time base : 20ms/div).

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Yulong Li was born in China, in 1982. He received his B.S. degree in Communication Engineering from Beijing University of Petro-chemical Technology, China, in 2004, and his M.S. and Ph.D. degrees in Electrical Engineering from Chonnam National University, Yeosu, Korea in 2006 and 2009, respectively. Currently, he is with Hyundai Heavy Industries Co., LTD., Korea as a researcher. His research interests are in the areas of modeling and control of power electronics converters and renewable generations. He is also is a member of the Korean Institute of Power Electronics.

Nam-Sup Choi was born in Seoul, Korea, in 1963. He received his B.S. degree in Electrical Engineering from Korea University in 1987. He received his M.S. and Ph.D. degrees in Electrical Engineering from the Korea Advanced Institute of Science and Technology (KAIST), Taejeon, Korea in 1989 and 1994, respectively. He is currently a professor in the Division of Electrical, Electronic Communication and Computer Engineering, Chonnam National University, Yeosu, Korea. His research interests include the modeling and analysis of power conversion systems, matrix converters and multilevel converters for renewable energy systems and micro-grid applications.

Byung-Moon Han received his B.S. degree in Electrical Engineering from Seoul National University, Korea in 1976, and his M.S. and Ph.D. degrees from Arizona State University in 1988 and 1992, respectively. He was with the Westinghouse Electric Corporation as a senior research engineer in the Science & Technology Center. Currently he is a professor in the Department of Electrical Engineering at Myongji University, Korea. His research interests include power electronics applications for FACTS, custom power and distributed power generation.

Eui-Cheol Nho was born in Korea in 1960. He received his B.S. in Electrical Engineering from Seoul National University, Korea in 1984, and his M.S. and Ph.D. in Electrical and Electronic Engineering from KAIST, Korea, in 1986 and 1991, respectively.

He was with the Powertech Co., Ltd., Korea, as a chief of the R&D center from 1991 to 1995. Since 1995, he has been a member of the faculty in the department of Electrical Engineering, Pukyong National University. From 1997 to 1998, he served as a visiting scholar at the Department of Electrical and Computer Engineering, University of Wisconsin, Madison, USA. From 2005 to 2006, he also served as a visiting scholar at the Department of Electrical Engineering and Computer Science, University of California, Irvine, USA. His current research interests include high voltage PWM converter, soft-switching converter, energy storage system, hybrid generation system, and power line conditioners, etc